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Investigation of CMOS Based Integration Approach Using DAI Technique for Next Generation Wireless Networks

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Abstract
This research work investigates a CMOS based low noise amplifier (LNA) using differential active inductor with eight-shaped patch antenna for next generation wireless communication. The proposed work conceded into three different phases. The first phase proposes LNA architecture which includes multistage cascode amplifier with a gate inductor gain peaking technique. The ground approach for this architecture employs active inductor technique that includes two stages of differential amplifier. The proposed novel technique leads to give incremental in inductance by using of common mode feedback resistor and lowers the undesirable parasitic resistance effect. Additionally, this technique offers gain enhanced noise cancellation and achieves a frequency band of around 5.7 GHz. The proposed architecture includes single stage differential AI and enhances the bandwidth up to 6.8 GHz with peak gain of 21 dB at 7.8 GHz. The noise figure and stability factor are achieved which is reasonably good at 1 dB. The proposed architecture is design and optimized on advanced design RF simulator using 0.045 μm CMOS process technology. While in second phase, a narrow band eight-shaped patch antenna is designed which provides operating band range from 5.8 to 6.5 GHz with 6.2 GHz resonating frequency. Highest peak gain of 15 dB and maximum radiation power of 42.5 dBm is succeed by proposed antenna. The final phase provides integration strategy of LNA with antenna and achieves desired gain of nearly 21 dB with minimum NF of 1.2–1.5 dB in the same band.

Keywords Low noise amplifier (LNA) · Differential active inductor (DAI) · Patch antenna · Complementary metal oxide semiconductor (CMOS)

1 Introduction

Beyond 2018, next generation of wireless communication looking much attention for the innovations and the technologies. These would be including possible innovations in architectures, spectrum allocation and utilization in radio communications, networks, and services and applications. The CMOS based low noise amplifier with antenna integration

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approach could be beneficial for next generation transceivers in the wireless communication environment. The demand of communication is served by the availability of high quality receiver systems capable to offer the desired features of present day applications. Therefore, the designers have constraint to maintain the demanded parameters with some advancement in technology whenever designing a low noise amplifier. The basic components of an LNA comprises of the passive elements along with the much-needed active devices like CMOS. Inductors or bonding wires play a vital role in designing of an LNA by offering bandwidth extension and gain peaking. At the same time, they are required to be omitted from the circuits due to various obvious reasons which includes high noise, large chip area consumption, their bulky nature and they cannot be fabricated easily on the chip. The other most important factor because of which we try to avoid them is the parasitic effect or mutual inductance issue due to which the deviation in the desired frequency is quite evident. Thus, other than bandwidth extension there are various parameters of a receiver system which are also of the prime concern while crafting it. Beginning from the noise figure improvement a CMOS UWB LNA is reported in [1] where the thermal noise is sensed and canceled by feed forward arrangement but it results in instability and poor gain performance. The LNA reported in [2] uses inductor less capacitive peaking technique for gain enhancement and noise cancellation. The effect of parasitic capacitance along with the active capacitors deteriorates the bandwidth performance by introducing the poles. This parasitic capacitance effect can be compensated by offering the bandwidth extension by the incorporation of negative capacitance in the distributed amplifier suggested in [3]. But in this scheme no emphasis is given over noise cancelation. So, an LNA is designed that offers very low NF and avoids the use of bulky inductors. Apart from this, it offers area and cost–benefit just by employing multiple feedback in LNA [4]. An LNA suggested in [5] uses active inductor for gain enhancement. In addition to it, the noise cancellation and bandwidth enlargement are also attained here. The use of active inductors avoids passive, bulky, conventional spiral inductors that offer a large number of drawbacks including noise and area consumption. The active inductors can be used in diversified LNAs resulting in numerous paybacks. The LNA using active inductor with multiple feed-forward results into noise reduction, high gain but the limited band of 0.32–1 GHz [6]. The active inductor in conjunction with negative capacitor can improve the gain flatness in a multiband amplifier [7]. Another LNA using active inductor focuses on linearity of the amplifier along with the gain, NF and bandwidth. It uses active inductor based on a two-stage differential amplifier [8]. This work describes a new technique to implement a differential active inductor (DAI) where only one stage of differential amplifier is used. It offers a simplified and improved architecture by offering bandwidth of nearly 6.8 GHz within the band of 1.9–8.7 GHz. Also, the NF comes out to be only 1.29 dB while stability factor almost maintain at circuit level and max gain of nearly 21 dB is achieved. The paper is so organized that Sect. 2 deals with design consideration of LNA with simulation and measured approach. Section 3 focuses on antenna design and performance. Section 4 describes the integration approach of LNA with antenna and finally Sect. 5 gives conclusion.

2 Design and Consideration

The reported research has contributed greatly in the field of low noise amplifier for RF wireless communication. In the present work, novel idea is to develop an active inductor (AI) since the conventional coil hugely affects the performance of the system in adverse

manner. Fig. 1 shows conventional schematic of two stage CMOS based differential active inductor. The function of inductors is quite significant in the designing of amplifiers to extend the bandwidth by pushing the dominant poles to high frequency reach. Hence, they are widely used in gate inductive gain peaking techniques. The downsides of these components are many such that they make the system bulky, noisy and occupy large chip area along with parasitic effects. The active inductors are the solution to this problem where the active devices such as CMOS have been utilized to fulfill the requirements of inductors. Recently designed active inductors (AI) are based on gyrator–C structure that yields area efficient and high Q inductors [9–11]. The differential AI comprises of two differential amplifiers with common mode feedback resistors R_{CMFB}. Here the feedback resistor R_f is inserted to increase the inductance and decrease the parasitic capacitance [8]. The inductance and resistance of the conventional AI are given in Eqs. (1) and (2) respectively.

$$L = \frac{C_{gsM_3,M_4} + \left(C_{gsM_7,M_8} + 2C\right)\left(1 + \frac{R_f}{R_{CMFB} \left\| r_{0M_3M_4} \right\| r_{0M_1M_2}}\right)}{g_{mM_3,M_4} g_{mM_7,M_8}} \tag{1}$$

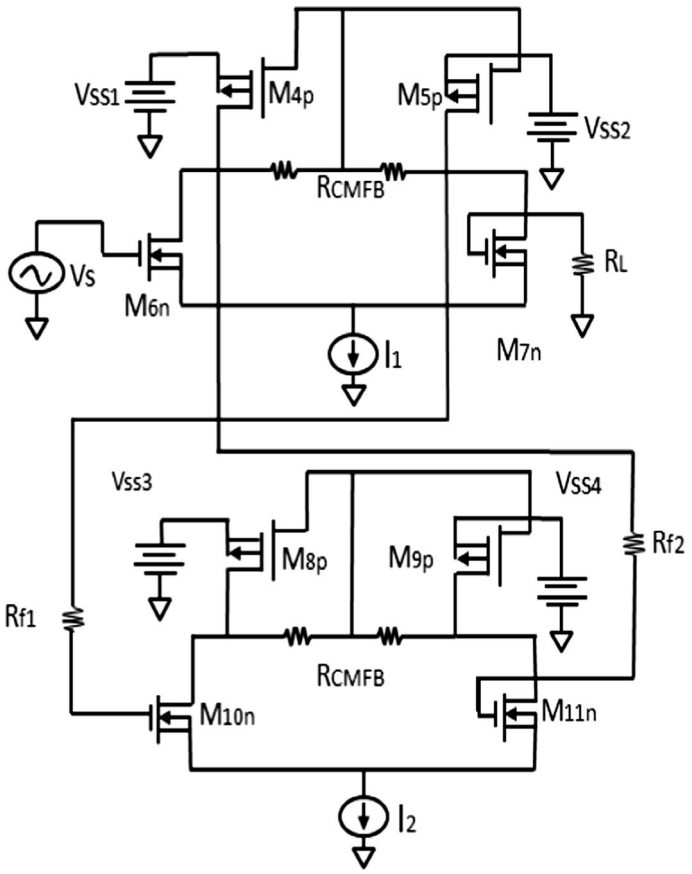


Fig. 1 Conventional structure of CMOS based active inductor

$$R = \frac{\frac{1}{R_{CMFB} \left\| r_{0M_3,M_4} \right\| r_{0M_1,M_2}} - \omega^2 \left(C_{gsM_7,M_8} + 2C\right) C_{gsM_3,M_4} R_f}{g_{mM_3,M_4} g_{mM_7,M_8}} \tag{2}$$

While for modified AI, inductance and resistance values can be evaluated by Eqs. (3) and (4) respectively.

$$L = \frac{C_{gsM_3,M_4} + \left(1 + \frac{R_f}{R_{CMFB} \left\| r_{0M_3M_4} \right\| r_{0M_1M_2}}\right)}{g_{mM_3,M_4}} \tag{3}$$

$$R = \frac{\frac{1}{R_{CMFB} \left\| r_{0M_3,M_4} \right\| r_{0M_1,M_2}} - \omega^2 C_{gsM_3,M_4} R_f}{g_{mM_3,M_4}} \tag{4}$$

Here C_{gs} is gate source capacitance of the MOS transistors, R_f is feedback resistance and r_o is output drain resistance of the device. The inductance and impedance of the AI are calculated on the basis of feedback resistance R_f.

It is well proven that the capacitive effect of MOS devices introduces poles that results into limited bandwidth. This issue is nullified by taking into account only one stage of proposed differential active inductor DAI which is shown in Fig. 2 such that the schematic would be not only simplified but its provides bandwidth extension also. Apart from that, power consumption is also reducing with minimized the noise effect. The impedance and inductance effect of DAI with respect to feedback resistance is shown in Fig. 3a, b respectively.

From the Fig. 3a, it is evident that the maximum value of L is achieved in the same band from 2 to 3 GHz with approximate values of 14 nH, 11 nH and 10 nH with respect to 0, 250 and 500 Ω. It is worth noting that as the frequency increased from 1 to 10 GHz, the inductance value decreases. Also as R_f tends to increase the flatness in the magnitude of L improves. The LNA with conventional active inductor is shown in Fig. 4. It comprises

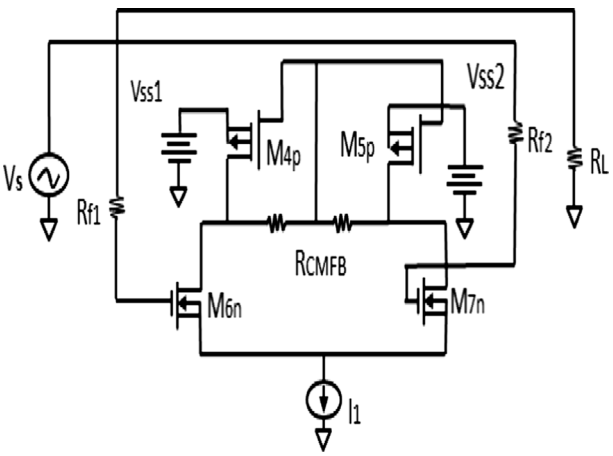


Fig. 2 Proposed schematic of active inductor (AI)

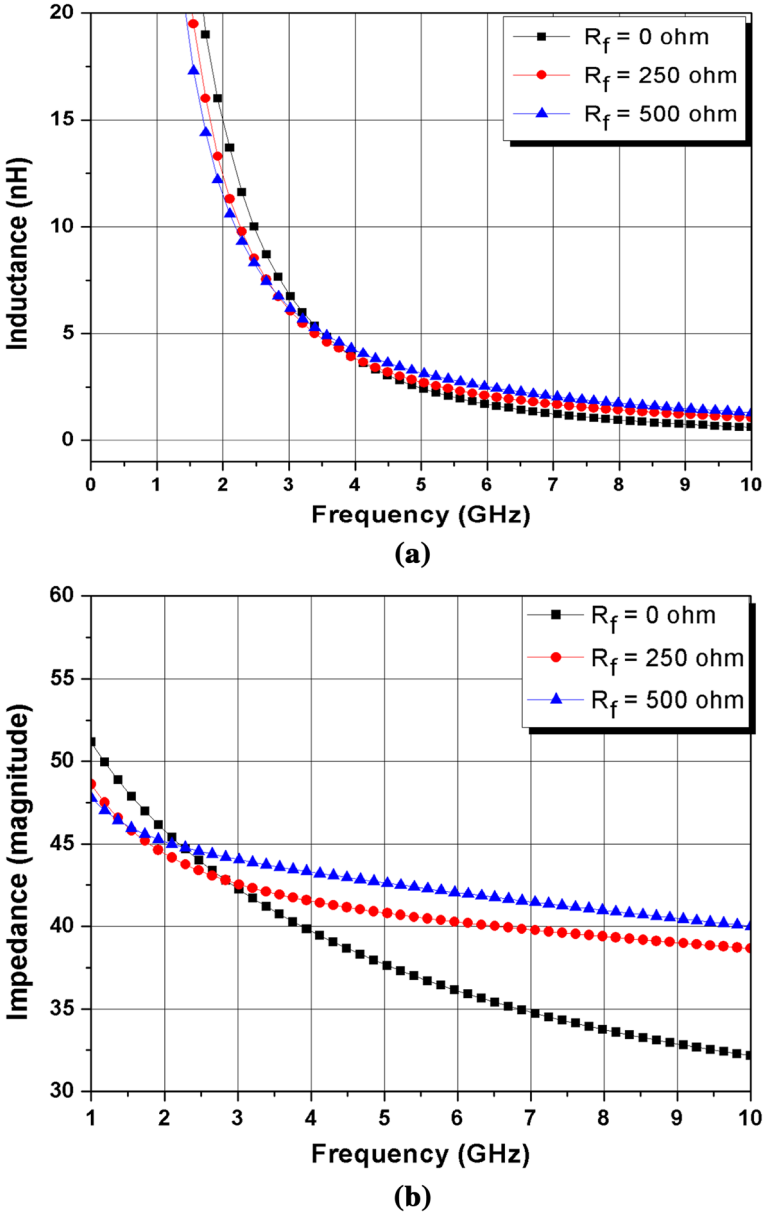


Fig. 3 Effect for proposed AI with variation of feedback resistance for. **a** Inductance and **b** impedance

of input matching stage using a cascode configuration of M1n and M1p. This architecture helps to nullify the noise effect due to high impedance and good reverse isolation features. In addition to this, it helps to improve frequency band by cancelling out miller effect which occurs at high frequencies resulting in roll-off of the gain. The limitation with the cascode stage is its gain flattening feature. So a shunt feedback resistor turns out to be an effective component for it. In addition to the input matching stage, another cascode stage of M_{2a}

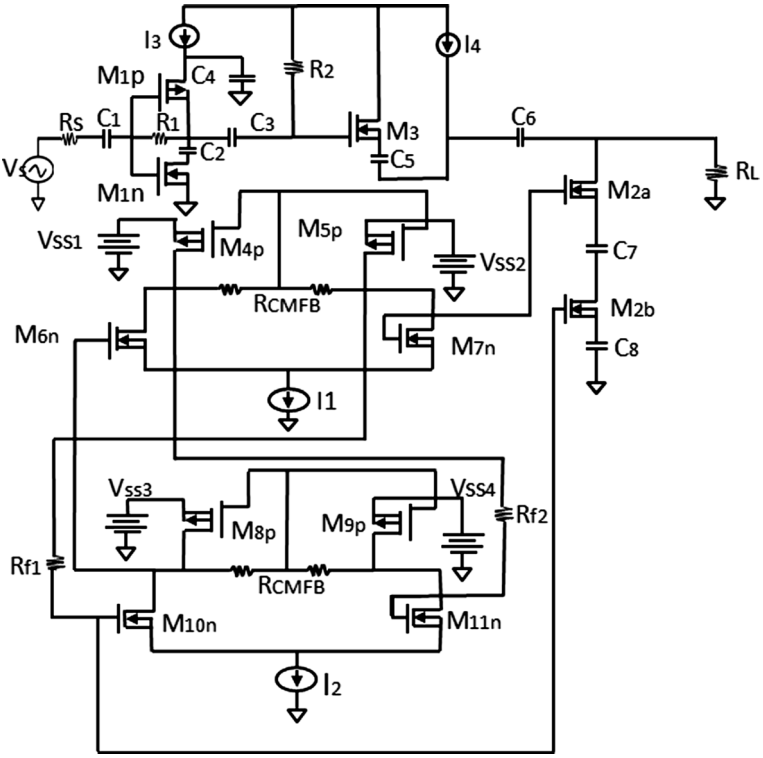


Fig. 4 Schematic of LNA with conventional AI

and M_{2b} is also used to cancel out the noise effect. The two stages are connected with the help of M_3 which acts as a source follower and also couples the two stages in order to have wideband operation at RF range. Thus the input matching and noise cancelling stage collectively offers high noise rejection with good gain flatness. The inductor is connected at the gate of M_{2a} whose function is essentially to compensate the dominant pole and provide bandwidth extension. However it raises the stability issue which is resolved by carefully designing the active inductor. Here the use of AI saves the chip area, reduces noise effect and offers high inductance value. In contrast to conventional architecture, the proposed one comprises less components where in only one stage of DAI is used along with the LNA mentioned here. The resultant proposed circuit is shown in Fig. 5. The performance comparison is shown here in terms of band of frequencies, forward gain, noise figure and stability factor in Fig. 7. Tables 1 and 2 are shown component values of CMOS LNA with AI and proposed AI. The microchip photograph of proposed LNA with AI is shown in Fig. 6. A silicon–copper metallization layer with thickness of 0.2 µm while metal–insulator–metal with oxide dielectric are used for passive components. The chip fabrication is done by using CMOS process of 0.045 µm with TSMC foundry kit. The area of chip fabrication is calculated as 0.125 * 0.212 mm^2 and less as compared to conventional ones.

It can be observed experimentally from Fig. 7a that the bandwidth extension is attained in the proposed DAI compared to the conventional configuration. It is evident from the graph that for conventional one it turns out to be 5.5 GHz ranging from 2.8 to 8.3 GHz

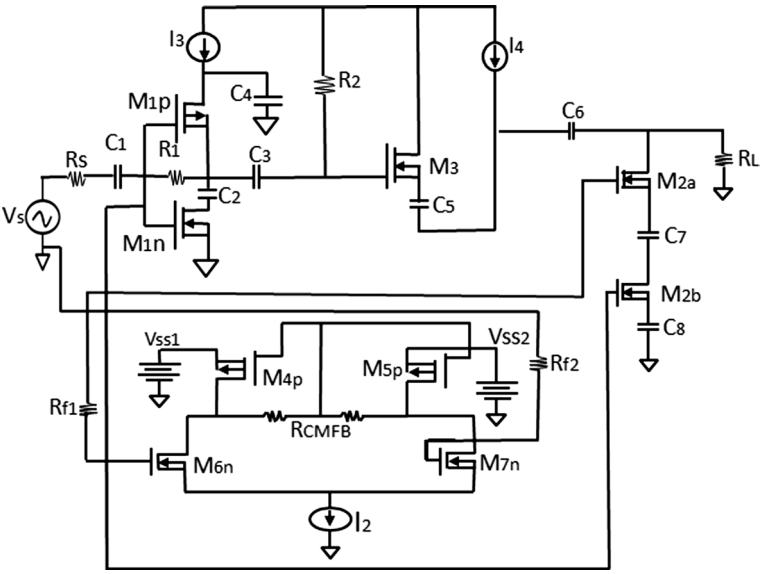


Fig. 5 Schematic circuit of LNA with proposed AI

Table 1 Component values of CMOS LNA

Component	Value	Component	Value
C_1	424 pF	I_1	0.8 mA
C_2	112 pF	I_2	6.5 mA
C_3	1.5 pF	M_{1n} (w/l)	0.001/0.045 µm
C_4	25.5 pF	M_{1p} (w/l)	60/0.045 µm
C_5	1.3 pF	M_{2a} (w/l)	0.005/0.045 µm
C_6	500 pF	M_{2b} (w/l)	0.001/0.045 µm
C_b	0.5 pF	M_3 (w/l)	825/0.045 µm
R_n	75 Ω	R_1	175 Ω

Table 2 Component values of CMOS AI

Component	Value	Component	Value
R_{CMFB}	21.5 Ω	M_{5p} (w/l)	60/0.045 µm
I_3	1 mA	M_{6n} (w/l)	100/0.045 µm
M_{4p} (w/l)	10/0.18 µm	M_{7n} (w/l)	100/0.045 µm

with minimum returns loss of − 11.4 dB at 4.8 GHz. For the proposed schematic, it gets improved by the factor of 1.3 GHz that is in the range of 1.9–8.7 GHz with the total band of 6.8 GHz with S_{11min} of − 11.8 dB at 4 GHz. As mentioned previously, the effect of noise is also minimized by cutting down one stage in the conventional DAI as each CMOS device contributes to a significant amount of noise in the schematic. The active inductor contributes to noise compared to conventional spiral inductors due to additional noise of the amplifier, but its impact on the overall noise performance is minimal which about 3%.

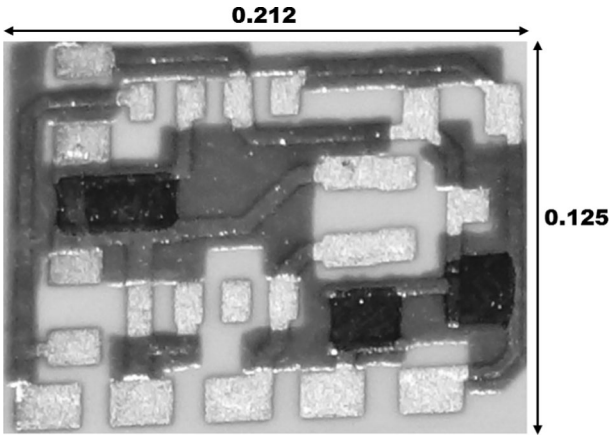


Fig. 6 Microchip photograph of proposed CMOS LNA

The deduction of one stage of DAI further minimizes it. Thus, the noise figure comparison is also done as shown in Fig. 7b. It is clear from the graph that the NF for the conventional configuration is nearly 2 dB throughout the frequency band while the performance gets elevated in the proposed DAI offering it to be less than 1 dB. As far as forward gain is concerned, it is shown in Fig. 7c. It depicts the forward gain in various forms. The conventional DAI gives it to be approximately 16 dB with a rapid rise in the range of 1–5 GHz with little flatter from 5 GHz onwards. The proposed DAI gives it to be smaller due to omission of one stage of DAI but the gain is much flatter for obvious reasons. So, its maximum value of 8 dB approximately. The integration of proposed DAI with LNA results into sufficiently high gain with much superior flatness in working band with slight sag in between 19 and 22 dB. The stability factor is also almost flat and nearly one for the complete bandwidth as shown in Fig. 7d. The performance comparison of proposed architecture with other reported papers is shown in Table 3.

3 Antenna Design and Performance

This section describes the design consideration of proposed antenna and its results. A narrow band printed slot dipole eight-shaped antenna is proposed here for next generation wireless communication. It is fabricated on FR-4 substrate with relative permittivity (ε_r) of 4.4 and thickness h = 1.6 mm. The antenna layout and its dimensions are shown in Fig. 8a. EM-simulator Ansoft HFSS.v.15 is used for design the proposed antenna. The total substrate size is chosen as 16×18 mm^2. The antenna structure is designed at 6 GHz and while it provides resonating frequency of 6.2 GHz. The two slots of same size of 5×1 mm^2 are cut inside the rectangular shape in the patch while one more slot cut that divides the structure in two parts having the dimension of 9.5×1.24 mm^2. A 50 Ω microstrip feed line is connected at the center of the patch whose dimension of 2×5 mm^2. The feeding line position and its length are optimized to maintain impedance matching. The fabricated antenna with measurement setup is shown in Fig. 8b. It can be observed from Fig. 8c that the simulated and the measured bands of the antenna are made good correlation with each other. It is a narrow band antenna operating at 6.2 GHz with a frequency band of 5.8–6.5 GHz. The peak gain as shown in Fig. 9a has a spike in the range of 5.8–6.6 GHz with the maximum

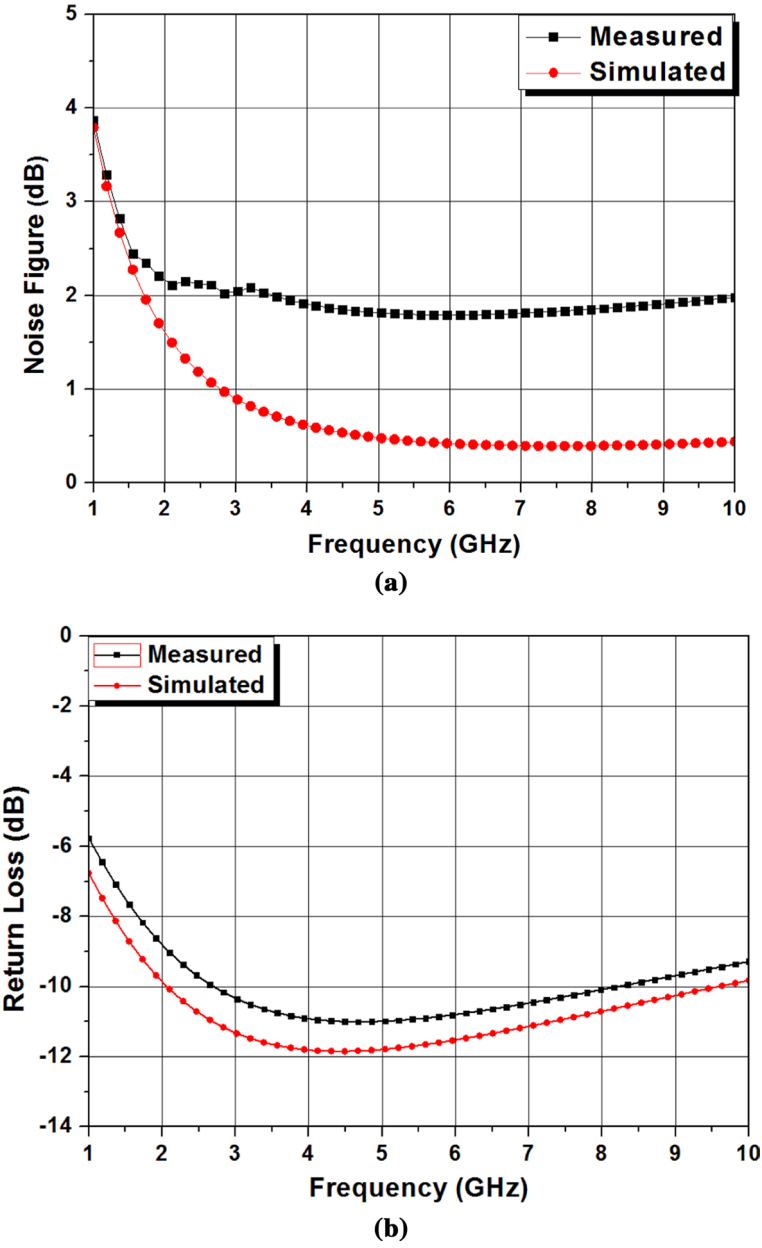
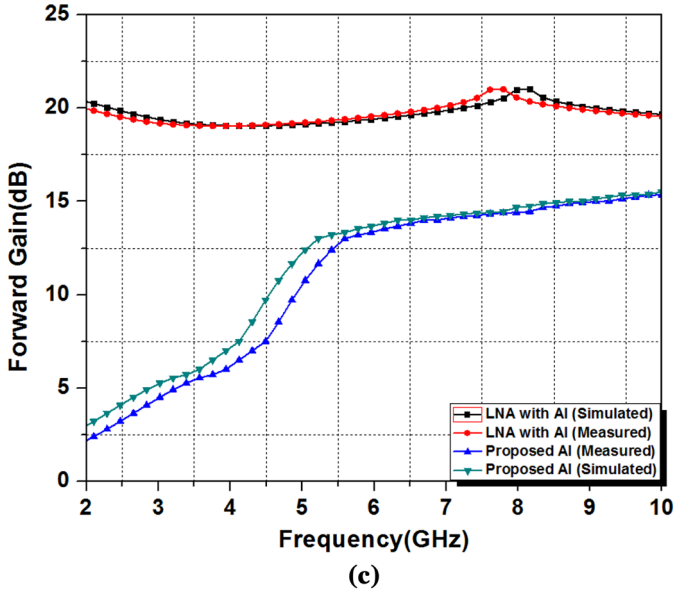


Fig. 7 Performance of LNA with measured data for **a** return loss, **b** noise figure, **c** maximum forward gain and **d** while stability factor with conventional one

magnitude of 14.46 dB. The radiated power is illustrated in Fig. 9b where it has two spikes, one is of 42.5 dBm in the desired band for $\Phi = 0°$ and $\theta = -180°$ while other is approximately 39 dBm in the band.



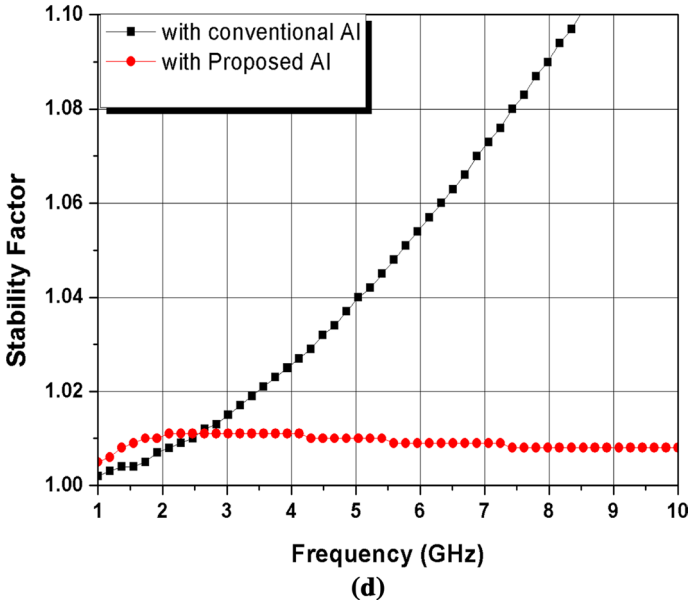


Fig. 7 (continued)

4 Integration Approach

The integration approach of antenna with LNA resulting into a complete receiver system for next generation wireless communication is presented in this section. As the designed antenna discussed above is not capable of offering sufficient gain, it is so integrated with proposed amplifier that the entire receiver system offers reasonably good amount of gain

Table 3 Performance comparison of proposed work with other reported ones

Design parameters	[2]	[5]	[7]	[8]	Current work
Technology (μm)	0.6	0.18	0.13	0.13	0.045
Frequency (GHz)	1.5	0.04–1.2	0.2–10.8	0.1–1.45	1.9–8.7
NF (dB)	3.5	2.1–3.4	4.1–6.2	2.5	0.6
Gain (dB)	22	16.4	21.5	16.9	21
Chip area (mm^2)	0.5 * 0.5	0.145 * 0.247	–	0.29 * 0.26	0.125 * 0.212

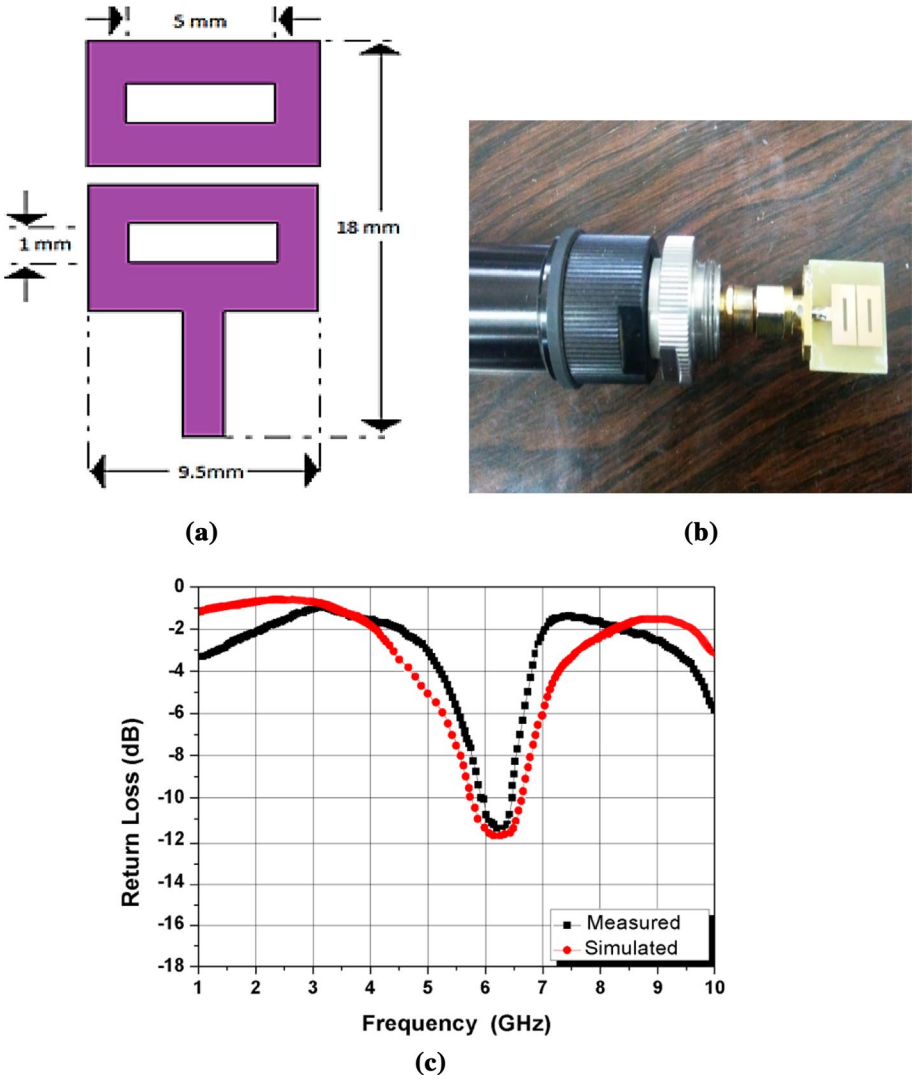


Fig. 8 Eight-shaped patch antenna with its **a** geometry, **b** fabricated picture and **c** measurement results

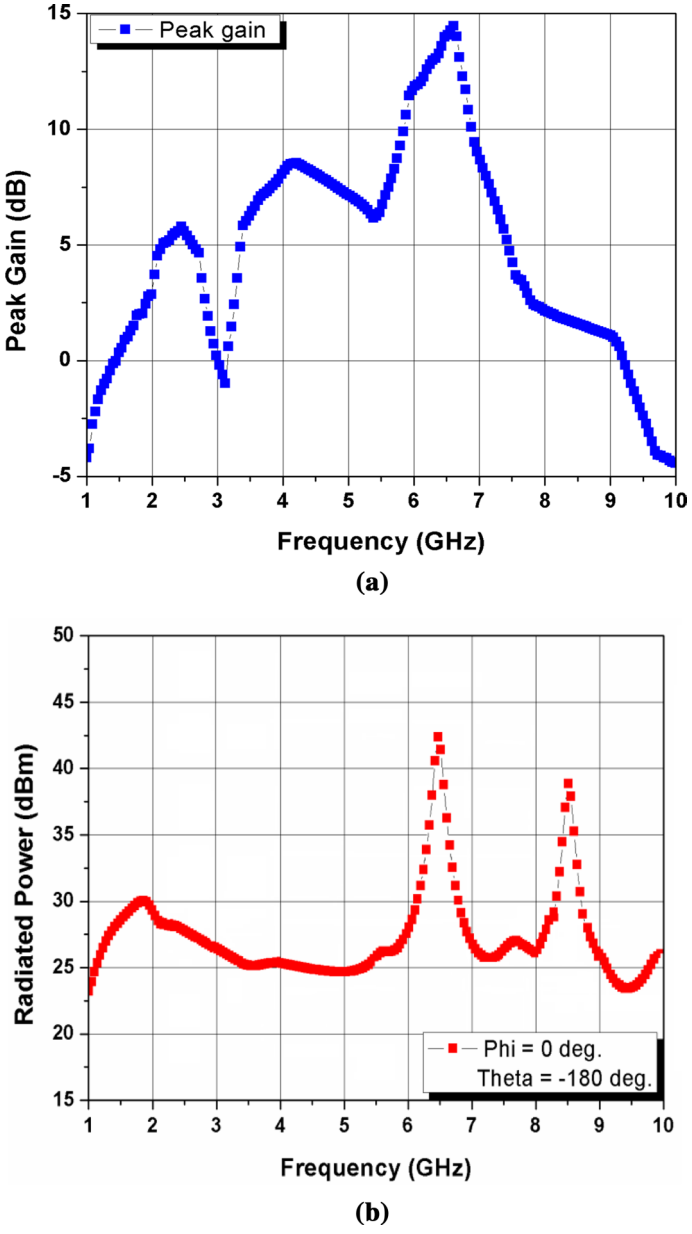


Fig. 9 Proposed antenna performance with its **a** peak gain and **b** radiated power

with the same bandwidth. The working principle is quite simple that the energy received by the antenna is coupled into the LNA which improves the amplification feature along with slight increment in noise figure. The proposed schematic of complete receiver system is shown in Fig. 10 and its performance is shown in Fig. 11. It is evident from the graph that the maximum gain is approximately 21 dB for the antenna band. The worth noting point

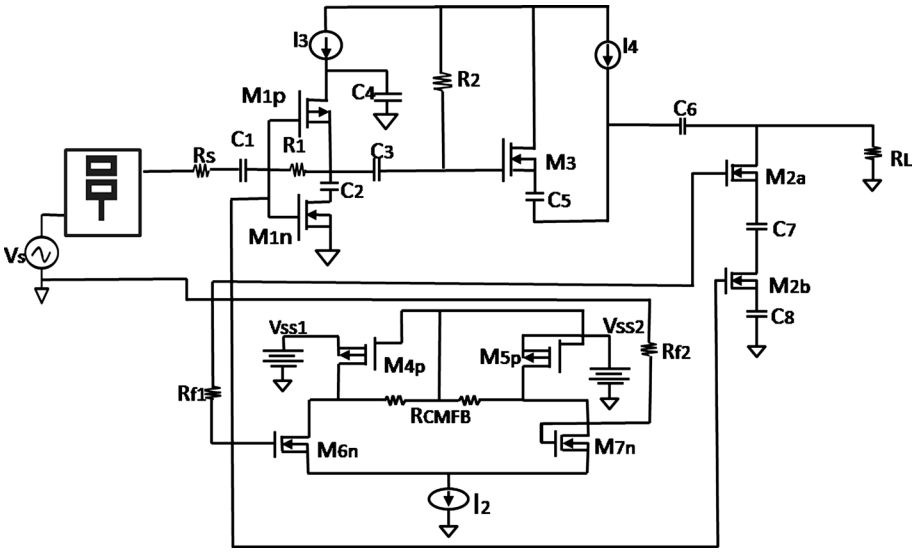


Fig. 10 Proposed schematic for Integration approach (LNA with antenna)

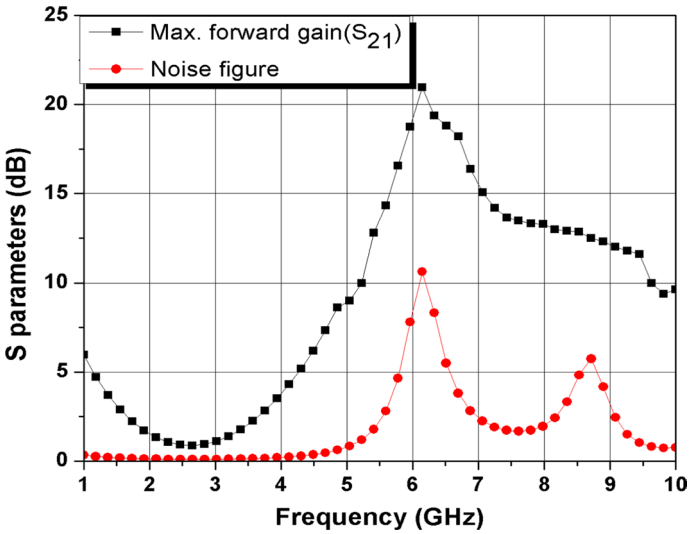


Fig. 11 Variation of noise and gain with respect to frequency

here is that out of a wide band amplifier the obtained output of the complete schematic is the expected antenna band. The noise performance is also shown here. It has increased for this band as it may arrive with antenna. The maximum NF obtained is 10.6 dB at 6.4 GHz.

5 Conclusion

The paper proposed CMOS based integration approach using single stage differential active inductor (DAI) for next generation wireless communication. The proposed architecture gave superior results as the band is obtained as 6.8 GHz with peak gain of 21 dB at 7.8 GHz while the noise figure and stability factor are nearly 1 dB. The DAI is designed on gate inductive gain peaking technique. A rectangular patch antenna is designed and fabricated and is coupled with the LNA to give a complete receiver system. The antenna is designed to operate for the band of 5.8–6.5 GHz. The overall maximum gain of the receiver system is 21 dB which is exactly equal to the gain offered by LNA only for antenna band. The measured results show that the proposed designs offer better outcome and could be operated for next generation wireless communication.

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References

1. Bruccoleri, F., Klumperink, E. A. M., & Nauta, B. (2004). Wide-band CMOS low-noise amplifier exploiting thermal noise canceling. *IEEE Journal of Solid-State Circuits, 39,* 275–282.
2. Li, Q., Member, I. E. E. E., & Zhang, Y. (2007). A 1.5-V 2–9.6-GHz inductor less low-noise amplifier in 0.13 µm CMOS. *IEEE Transactions on Microwave Theory and Techniques, 55,* 2015–2023.
3. Ghadiri, A., & Moez, K. (2010). Gain-enhanced distributed amplifier using negative capacitance. *IEEE Transactions on Circuits and Systems, 57,* 2834–2843.
4. Sobhy, E., Helmy, A., Entesari, S., & Sánchez-Sinencio, E. (2011). A 2.8-mW Sub-2-dB noise-figure inductorless wideband CMOS LNA employing multiple feedback. *IEEE Transactions on Microwave Theory and Techniques, 59,* 3154–3161.
5. Yu, Y.-H., Yang, Y.-S., & Chen, Y.-J. (2010). A compact wideband CMOS low noise amplifier with gain flatness enhancement. *IEEE Journal of Solid-State Circuits, 45,* 502–508.
6. Moezzi, M., & Sharif Bakhtiar, M. (2012). Wideband LNA using active inductor with multiple-feed-forward noise reduction paths. *IEEE Transactions on Microwave Theory and Techniques, 60,* 1069–1077.
7. Ghadiri, A., & Moez, K. (2014). Wideband active inductor and negative capacitance for broadband RF and microwave applications. *IEEE Transactions on Components, Packaging and Manufacturing Technology, 4,* 1808–1814.
8. Ma, L., Wang, Z.-G., Jian, X., & Amin, N. M. (2017). A high linearity wideband common-gate LNA with differential active inductor. *IEEE Transactions on Circuits and Systems II*. https://doi.org/10.1109/tcsii.2016.2572201.
9. Reja, M. M., Moez, K., & Filanovsky, I. (2010). An area-efficient multistage 3.0 to 8.5 GHz CMOS UWB LNA using tunable active inductors. *IEEE Transactions on Circuits Systems II, 57,* 587–591.
10. Abdalla, M., Eleftheriades, G. V., & Phang, K. (2006). A differential 0.13 µm CMOS active inductor for high-frequency phase shifters. In *Proceedings of IEEE international symposium on circuits systems (ISCAS)* (pp. 3341–3344).
11. Akbari-Dilmaghani, R., Payne, A., & Toumazou, C. (1998). A high Q RF CMOS differential active inductor. In *IEEE Proceedings ISCAS* (Vol. 3, pp. 157–160).

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