Journal of
Low Power Electronics
Vol. 14, 266–274, 2018

Low Voltage, Low Power G_m-C Filter for Low Frequency Applications

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(Received: 26 December 2017; Accepted: 13 March 2018)

This paper describes a low voltage, low power Transconductance-C (G_m-C) filter for low frequency applications. A tunable bulk-driven transconductor is proposed to realize the filter. The transconductance (G_m) is tunable from 8 nS to 90 nS, which is suitable for low frequency G_m-C filters. The transconductor consumes a power of 86 nW. To evaluate the performance of the proposed transconductor, a 2nd order Butterworth low pass filter (LPF) is designed. The cutoff frequency of the filter is tunable from 74 Hz to 820 Hz. The filter offers a dynamic range of 52 dB while consuming a power of 248 nW for a nominal cutoff frequency of 456 Hz. The circuit has been designed and simulated in UMC 180 nm technology with a supply voltage of 0.5 V.

Keywords: Bulk-Driven, Low-Voltage, Low-Power, Low-Frequency Filters.

1. INTRODUCTION

Continuous time (CT) filters are one of the important building blocks of analog pre-processing in wearable and implantable medical devices such as heart rate detectors, breathing detectors, cardiac-pacemakers, cochlear implants etc. They are used to limit the frequency band and to eliminate the out-of-band noise. As the signals involved in the above mentioned applications are of low frequency, typically 10 mHz to 10 kHz,[1] it is mandatory to design such filters with low cutoff frequency. The other major requirements of these filters are low power consumption, low noise and less area as these medical devices are portable and battery operated.

The popular topologies of CT filters are Active-RC and G_m-C structures. To design Active-RC filters with low cutoff frequency, large resistors and capacitors are required, which occupy a large area on the chip. Hence, simple Active-RC filters are not suitable for low frequencies. However, certain circuit techniques have been developed such as current steering,[2,3] Pseudo resistor based Active-RC filter,[4,5] R-2R ladder network[6,7] based filter etc., for low frequencies. But all these techniques have their own limitations as far as power, area, thermal noise, high sensitivity to changes in bias voltage etc., are concerned. In general, G_m-C filters are preferred over Active-RC filters for low frequencies.

In G_m-C filters, the cutoff frequency is determined by $G_m/(2\pi C)$. To get low cutoff frequency, either G_m should be low or capacitor should be large. But, large capacitors occupy more area on the chip. By using impedance scaler circuits[8,9] the capacitance value can be increased with less silicon area. But these circuits not only consume extra power but also produce extra noise. Therefore, a transconductor with small G_m is preferred for the realization of low frequency filters. Current division and current cancellation techniques to reduce G_m are reported in Refs. [9,10]. These techniques require more power and suffer from offset voltage. Floating-gate transistors[11,12] capacitively attenuate the input voltage and reduce the G_m. But, these transistors occupy more silicon area and need extra processing steps.

According to ITRS-2015 (International Technology Road map for Semiconductors), by about the year 2024, the power supply for digital circuits will be about 0.55 V. The main motive for this scaling of supply voltage is to reduce the dynamic power of digital logic circuits. Analog circuits have to work with these low supply voltages as they exist along with digital circuits in a typical System-on-chip (SoC). But the supply voltage scaling in analog circuits, results in the reduction of signal swing, and hence reduces dynamic range. As the threshold voltage (V_{th}) of the transistors is scaled at a slower rate than supply voltage, this problem is magnified. Thus, the existing analog circuits should be modified in order to have the same or even better performance under low voltage conditions.

In order to avoid above mentioned problems, bulk-driven transistors[13] can be used, where the signal is applied

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 1546-1998/2018/14/266/009 doi:10.1166/jolpe.2018.1558

to the bulk terminal rather than the gate terminal. This reduces the V_{th} of transistor and allows rail-to-rail input voltage swing even under low supply voltages such as 0.5 V. The bulk transconductance is typically 0.2–0.4 times the gate transconductance, which is the major requirement for the low frequency G_m-C filters. The G_m can be reduced further by current scaling circuits.[14] Therefore, a low voltage, low power transconductor with low G_m can be realized by using bulk-driven input transistors and current scaling circuits.

This paper proposes the design of fully differential tunable bulk-driven transconductor. As an application, a 2nd order Butterworth LPF is designed to demonstrate the performance of the transconductor. The rest of the paper is organized as follows. In Section 2, design of transconductor and its simulation results are discussed. Section 3 deals with design of the filter and its simulation results. Finally conclusions are drawn in Section 4.

2. TRANSCONDUCTOR DESIGN

Low power transconductor with small G_m is required for the realization of low frequency filters for biomedical applications. To allow full integration with digital circuits in deep sub-micron CMOS technologies, transconductor is required to operate under low supply voltage while maintaining sufficiently large dynamic range. Bulk-driven transistors[13] can be used to reduce the G_m as well as to allow rail-to-rail input voltage swing even under low supply voltages. The bulk transconductance (g_{mb}) is typically 0.2–0.4 times the gate transconductance (g_m). The gate-driven and bulk-driven transconductances in sub-threshold region are given by (1) and (2)[15] respectively.

$$g_m = \frac{I_D}{mV_T} \tag{1}$$

$$g_{mb} = (m-1)g_m \tag{2}$$

where, I_D is drain current of the transistor, $V_T = kT/q$, is volt-equivalent of temperature and m is sub-threshold slope factor. Typical value of m lies between 1.2 and 1.4.[15]

To reduce the G_m further, current scaling technique[14] is employed. In this paper, a low voltage, low power transconductor with low G_m is proposed by employing bulk-driven input transistors and current scaling technique.

2.1. Proposed Transconductor

Single ended circuit of the proposed transconductor is shown in Figure 1, where V_{in} and V_o represent input and output voltages respectively. V_{in} is given to the bulk terminal of the input transistor M_1. Here, the supply voltage (V_{DD}) is 0.5 V and input common-mode voltage is 0.25 V. This input common-mode voltage reduces V_{th} of the input transistor M_1 and allows more signal swing. I_{in} represents the current of transistor M_1 and I_o represents the output current. The transistor M_1 is biased by a constant current of

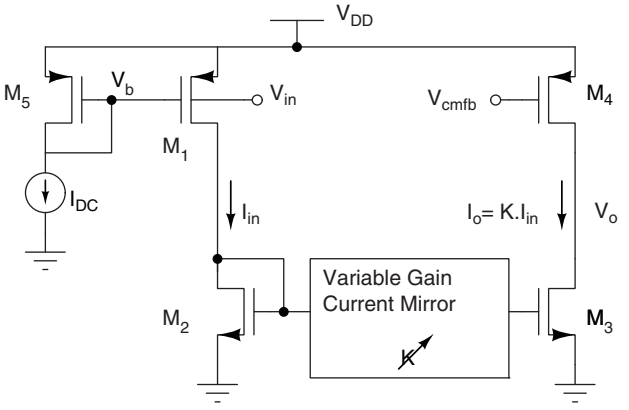


Fig. 1. Tunable single ended bulk-driven transconductor.

10 nA that is mirrored by constant current source I_{DC}. Bias current of 10 nA can be generated by using off-chip current sources such as Keithley or by using on-chip current generator circuits. M_2 mirrors the current I_{in} to M_3 through Variable Gain Current Mirror[14] with a current gain K.

The Variable Gain Current Mirror circuit is shown in Figure 2. The currents I_1 and I_2 are generated from a reference current source (not shown in figure). M_2, M_3, M_6 and M_7 are biased in the weak-inversion region and form translinear loop.[16] The relation among the gate-source voltages of M_2, M_3, M_6 and M_7 can be expressed as (3).

$$V_{GS2} + V_{SG6} = V_{SG7} + V_{GS3} \tag{3}$$

For an NMOS transistor operating in weak-inversion region, the drain current can be written as

$$I_{Dn} = A_n e^{B_n(V_{GSn}-V_{tn})}(1 - e^{-V_{DSn}/V_T}) \tag{4}$$

where,

$$A_n = \mu_n C_{ox}\frac{W}{L}(m_n - 1)V_T^2$$

$$B_n = \frac{1}{m_n V_T}$$

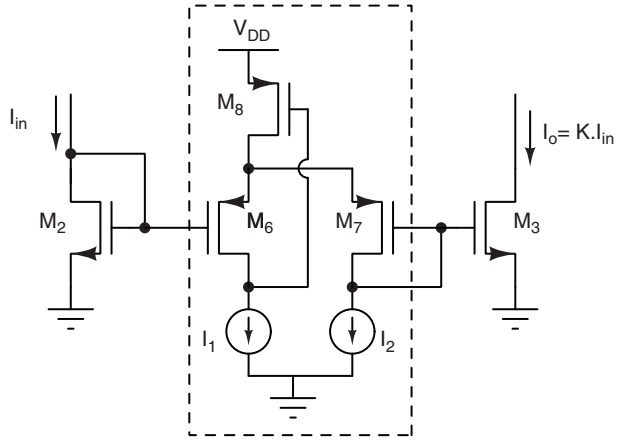


Fig. 2. Variable gain current mirror.

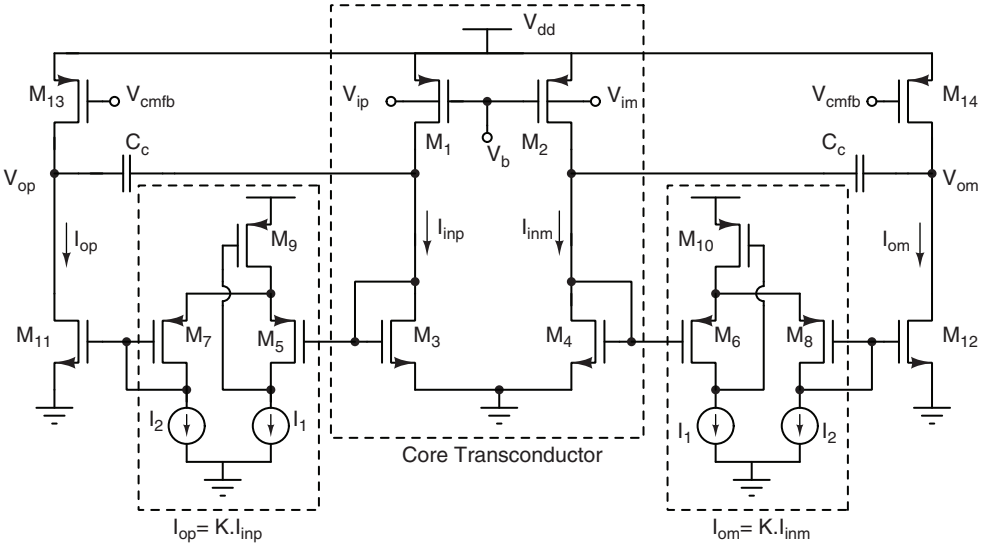


Fig. 3. Fully differential tunable bulk-driven transconductor.

m_n is sub-threshold slope factor of NMOS transistor and its value lies between 1.1 and 1.4. For $V_{DSn} \geq 4V_T$, the current I_{Dn} can be assumed to be independent of V_{DSn} i.e., $(1 - e^{-(-V_{DSn}/V_T)}) \approx 1$. Then (4) can be simplified to (5).

$$I_{Dn} \approx A_n e^{B_n(V_{GSn} - V_{tn})} \tag{5}$$

Similarly, the drain current for a PMOS can be written as (6)

$$I_{Dp} \approx A_p e^{B_p(V_{\mathrm{SGp}} - |V_{tp}|)} \tag{6}$$

From the Eqs. (5) and (6), V_{GSn} and V_{SGp} can be derived as (7) and (8) respectively.

$$V_{GSn} = \frac{1}{B_n} \ln\left(\frac{I_n}{A_n}\right) + V_{tn} \tag{7}$$

$$V_{\mathrm{SGp}} = \frac{1}{B_p} \ln\left(\frac{I_p}{A_p}\right) + |V_{tp}| \tag{8}$$

The transistors M_2, M_3 and M_6, M_7 in Figure 2 are matched. By substituting (7) and (8) in (3), the relationship among the currents I_{in}, I_{o}, I_1 and I_2 can be derived as (9)

$$I_{\mathrm{o}} = K \cdot I_{in} \tag{9}$$

where $K = (I_1/I_2)^{m_p/m_n}$ is the current gain.

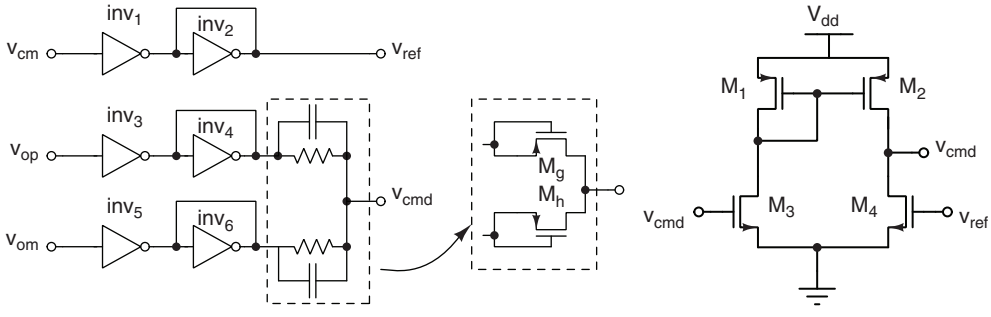
When $I_1 = I_2$, the current gain is 1 as $V_{\mathrm{SG6}} = V_{\mathrm{SG7}}$, $V_{\mathrm{GS2}} = V_{\mathrm{GS3}}$. When $I_1 > I_2$, the current gain is >1 as $V_{\mathrm{SG6}} > V_{\mathrm{SG7}}$, $V_{\mathrm{GS2}} < V_{\mathrm{GS3}}$. When $I_1 < I_2$, the reverse is true and the current gain is <1. Therefore the output current of the transconductor can be scaled by varying the currents I_1 or I_2, which in turn scales the effective transconductance of the circuit.

A fully differential version of the proposed transconductor is shown in Figure 3. The input transistors M_1 and M_2 are biased by using a current source of 10 nA (not shown in the figure). M_5–M_{10} and current sources I_1, I_2 form Variable Gain Current Mirror. All the transistors are operating in weak-inversion region. C_c is used as compensating capacitor to improve the phase margin.

The output differential current, i_{od} is given by (10).

$$i_{od} = K \cdot g_{mb} \cdot v_{id} \tag{10}$$

where $i_{od} = I_{op} - I_{om}$ is the output differential current, g_{mb} is the bulk-driven transconductance of the input transistor M_1 or M_2 and $v_{id} = V_{ip} - V_{im}$ is the input differential voltage.



(a) Common mode detector (b) Error amplifier

Fig. 4. CMFB circuit.[17]

The effective transconductance G_m is given by (11).

$$G_m = K \cdot g_{mb} \tag{11}$$

The voltage gain of the transconductor is given by (12).

$$A_v = K \cdot g_{mb} \cdot (r_{11} \parallel r_{13}) \tag{12}$$

where r_{11} and r_{13} are small signal output resistances of M_{11} and M_{13} respectively.

The transconductor uses a supply voltage of 0.5 V. The input common mode voltage (V_{cm}) is fixed at 0.25 V. Gates of M_{13} and M_{14} are biased with a common mode feedback voltage (V_{cmfb}) which sets the output common mode voltage to 0.25 V.

2.2. Common Mode Feedback Circuit

For a differential transconductor, a common mode feedback (CMFB) circuit is needed to maintain output common mode voltage of $V_{DD}/2$. A CMFB circuit proposed in Ref. [17] (Fig. 4) is used in this work. In Figure 4(a), inverters 3 to 6 along with transistors M_g and M_h form common mode detector. Inverters 3 and 5 sense the output voltages of the transconductor. Inverters 4 and 6 have their outputs shorted to inputs. This arrangement reduces the gain of sensing inverters, thus enhancing the linearity of the sensing inverters and entire CMFB circuit. Transistors M_g and M_h are connected such that they offer high resistance along with a capacitor. This arrangement gives the average (V_{cmd}) of the sensed output voltages of the transconductor. V_{ref} is generated from V_{cm} using the inverters 1 and 2. V_{cmd} is compared with the V_{ref} using a simple error amplifier shown in Figure 4(b). The error amplifier output voltage, V_{cmfb} is fed back to the transconductor to set the output common mode to V_{cm} (0.25 V). The total power consumption of the CMFB circuit is 40 nW.

2.3. Simulation Results

The transconductor is designed and simulated in UMC 180 nm technology using a power supply of 0.5 V. G_m of the transconductor can be tuned by varying the currents I_1 and I_2. This varies the current gain, K and hence G_m. The simulated G_m against the input differential voltage for different I_1 values is shown in Figure 5. G_m is tuned from 8 nS to 90 nS by fixing I_2 at 10 nA and varying I_1 from

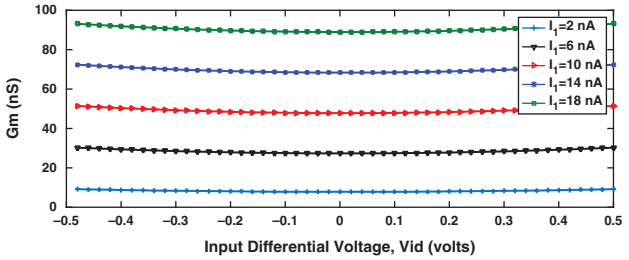


Fig. 5. G_m tuning.

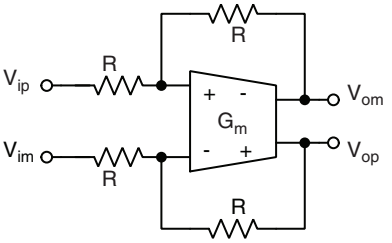


Fig. 6. Transconductor set up for linearity measurement.

2 nA to 18 nA in steps of 4 nA. The values of I_1 and I_2 can be digitally controlled by using current splitting circuits implemented as in Ref. [18]. It is observed that an equal increment in I_1, gives almost an equal increment in G_m.

The magnitude and phase response of the proposed transconductor are shown in Figure 7. The open loop DC gain is 28 dB and the unity-gain frequency is 3.7 kHz without adding any load capacitor. The phase margin is 83°.

To test the linearity, the transconductor is connected in unity feedback configuration with resistor, $R = 10$ KΩ as shown in Figure 6. A sinusoidal signal of frequency 100 Hz is applied to this circuit. The total harmonic distortion (THD) is found to be less than −40 dB for an input voltage of 1 V_{pp} differential. The integrated input referred noise from 40 Hz to 4 kHz is 47 μV_{RMS}. The dynamic range of the the transconductor is calculated to be 77 dB. Table I lists the parameters of the proposed transconductor.

A performance comparison of the proposed transconductor with other similar works found in the literature is given in Table II. The power consumption of the proposed transconductor including the CMFB circuit is as low as 86 nW. It can be seen that, performance of the proposed transconductor is better in terms of power and G_m tunability. Hence, it can be very efficiently used for the

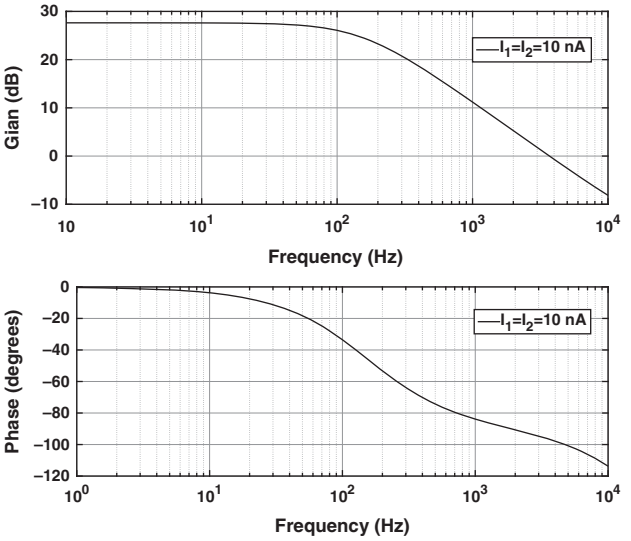


Fig. 7. Frequency response of the transconductor.

Table I. Parameters of the transconductor.

Parameter	Simulated values
Technology (μm)	0.18
Supply voltage (volts)	0.5
Transconductance (nS)	8–90
DC gain (dB)	28
UGB (kHz)	3.7
Phase margin (degrees)	83
$V_{\text{in-pp}}$ for 1% THD (volts)	1.0
Input referred noise from 40 Hz–4 kHz (μV)	47
Dynamic Range (dB)	77
Power (nW)	86[†]

Note: [†]At $I_1 = I_2 = 10$ nA, including CMFB circuit.

Table II. Comparison of the proposed transconductor with other similar works.

Parameters	[14]	[25]	[12]	[26]	This work
Technology (μm)	0.18	0.35	0.8	1.2	0.18
Supply voltage (volts)	0.8	0.8	1.5	1.35	0.5
DC gain (dB)	72.2	61	–	–	28
G_m (nS)	300–3000	66 n	0.46–82	16.6	8–90
UGB (kHz)	15 with $C_L = 20$ pF	0.195 with $C_L = 25$ pF	–	–	3.7
Phase margin (degrees)	90	81	–	–	83
Input referred noise (μV RMS)	–	80	110	17.29	47
$V_{\text{in-pp}}$ for 1% THD (volts)	1.6	0.1	1.2	0.24	1
Dynamic range (dB)	75	52.9	73	73.9	77
Power (μW)	8.3	0.040	≈1	1.35	0.086

design of low frequency filters with low supply voltage and low power.

2.3.1. G_m Variation with Process Corners and Temperature

Simulations are carried out to observe the effect of process corners (tt, ff, ss, fnsp and snfp) and temperature on G_m. The variation in G_m is found to be <1% across all the corners as given in Table III. As all transistors are operating in sub-threshold region, G_m is more sensitive to temperature compared to that when they are in strong-inversion saturation region. The variation in G_m is found to be ±6.3% for a temperature range of 0–70 °C. This variation in G_m can be compensated by using constant-G_m bias circuit. Table IV shows G_m values for different temperatures. It is observed that as the temperature increases, G_m decreases.

Table III. G_m variation with process corners.

Process corner	tt	ss	ff	fnsp	snfp
G_m (nS)	48	47.42	48.05	47.41	48.06

Table IV. G_m variation with temperature.

Temperature (°C)	0	27	50	70
G_m (nS)	50	48	46	44.6

3. FILTER DESIGN

A fully differential G_m-C, 2nd order LPF is shown in Figure 8.[19] Butterworth filter is chosen to get maximally flat response in the pass band. A 2nd order Butterworth LPF is designed and simulated to evaluate the performance of the proposed transconductor.

Transfer function of this 2nd order LPF can be derived as in (13).

$$H(s) = \frac{G_{m1}/G_{m4}}{(s^2 C_1 C_2/G_{m3}G_{m4}) + (sG_{m2}C_2/G_{m3}G_{m4}) + 1} \tag{13}$$

Transfer function of the 2nd order LPF prototype is given by (14)

$$H(s) = \frac{A_o}{(s^2/\omega_o^2) + (s/\omega_o Q) + 1} \tag{14}$$

By comparing (13) with (14), the expressions for DC gain (A_o), cutoff frequency (f_o) and Quality-factor (Q_o) are given by (15), (16) and (17) respectively.

$$A_o = \frac{G_{m1}}{G_{m4}} \tag{15}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{G_{m3}G_{m4}}{C_1 C_2}} \tag{16}$$

$$Q_o = \sqrt{\frac{C_1}{C_2}}\frac{\sqrt{G_{m3}G_{m4}}}{G_{m2}} \tag{17}$$

The expressions for DC gain, cutoff frequency and quality factor are modified to (18), (19) and (20) respectively if the input, output parasitic capacitances (C_i, C_o) and input, output conductances (g_i, g_o) of the transconductor are taken into account.

$$A'_O = \frac{G_{m1}G_{m3}}{(g_o + g_i)(G_{m2} + 2g_i + 3g_o) + G_{m3}G_{m4}} \tag{18}$$

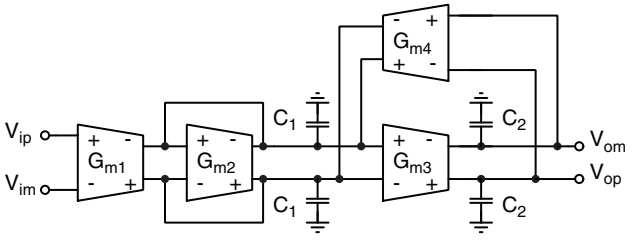


Fig. 8. 2nd order G_m-C LPF.

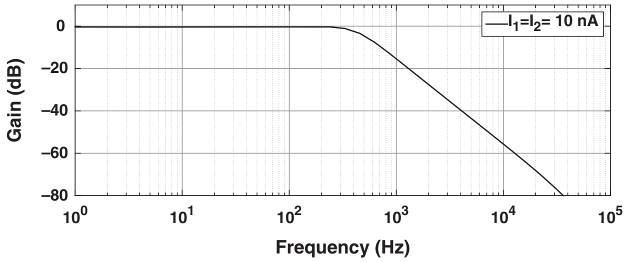


Fig. 9. Frequency response of the filter.

$$f'_o = \frac{1}{2\pi}\sqrt{\frac{(g_o+g_i)(G_{m2}+2g_i+3g_o)+G_{m3}G_{m4}}{C'_1C'_2}} \quad (19)$$

$$Q'_o = \sqrt{C'_1C'_2}\frac{\sqrt{(g_o+g_i)(G_{m2}+2g_i+3g_o)+G_{m3}G_{m4}}}{(3g_o+2g_i)C'_2+(g_o+g_i)C'_1+G_{m2}C'_2} \quad (20)$$

where, $C'_1 = C_1+3C_o+2C_i$ and $C'_2 = C_2+C_o+C_i$.

Hence, it can be seen that when the parasitic capacitances and input/output conductances are taken into account, actual frequency response deviates from the expected one. Simulations are carried out to estimate C_i, C_o, g_i and g_o. C_i and C_o are found to be 70 fF and 1.67 pF respectively. g_i and g_o are found to be 75 pS and 2 nS respectively.

For the 2nd order Butterwoth filter, quality factor is $1/\sqrt{2}$. In this design, all transconductances are taken to be equal. C_1 and C_2 are chosen to be 10 pF and 20 pF respectively to get the quality factor of $1/\sqrt{2}$.

Two CMFB circuits are used for this filter to maintain a common-mode voltage of 0.25 V at each node. As output nodes of G_{m1}, G_{m2} and G_{m4} blocks connected together, only one CMFB circuit is used for these blocks. One more CMFB circuit is used for G_{m3} block.

3.1. Simulation Results and Discussion

The cutoff frequency of the filter is 456 Hz for $I_1 = I_2 =$ 10 nA as shown in Figure 9. It is tuned from 74 Hz to 820 Hz by varying the current I_1 from 2 nA to 18 nA while keeping I_2 at 10 nA as shown in Figure 10. It can be tuned to the required value by controlling the currents I_1 and I_2 in the transconductor, so that it fits into the desired frequency range of different bio-potentials such as electromyogram (EMG), electroencephalogram (EEG), electrocardiogram (ECG) etc. Simulated values of DC gain and cutoff frequency very well match with the analytical expressions given in (18) and (19) respectively.

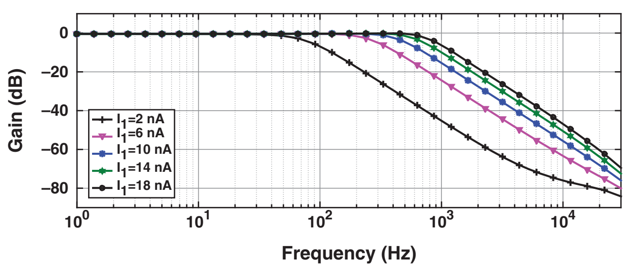


Fig. 10. Tuning of the filter cutoff frequency.

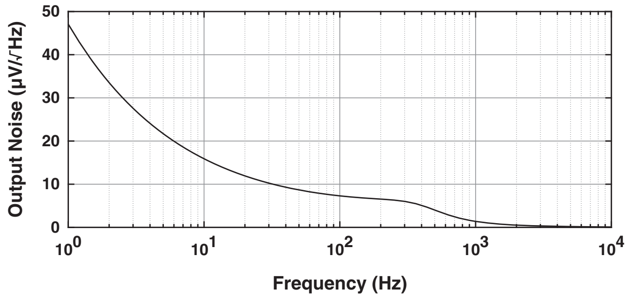


Fig. 11. Output noise of the filter.

Figure 11 shows output noise of the filter. At low frequencies it is dominated by flicker $(1/f)$ noise, around the cutoff frequency thermal noise dominates and it follows the filter response at higher frequencies. The 1/f corner frequency is approximately 30 Hz. The total input-referred noise integrated over the frequency range 5–500 Hz is 160 μV_{RMS}. A sinusoidal input signal of frequency 100 Hz is applied to measure the THD of the filter. THD of the output differential signal is found to be −40 dB for an input differential peak–peak voltage of 180 mV. Dynamic range of the filter is calculated to be 52 dB. Table V lists the parameters of the filter.

A performance comparison of the designed filter with other similar works found in the literature is listed in Table VI. Figure-of-Merit (FoM) in (21)[20] is used as performance measure. The lower the value of FoM, better is the performance of the filter. The filter designed using the proposed transconductor achieves an FoM of 0.78 pW/pole, which is better than FoM values quoted in Refs. [21–23]. In Ref. [11], floating-gate transistors are used to improve dynamic range and FoM, but these transistors occupy more silicon area and need extra processing steps. FoM value quoted in Ref. [24] is better than the FoM value of the proposed circuit. But the proposed circuit is better in terms of power when compared to that in Ref. [24].

$$\text{FoM} = \frac{\text{Power}}{\text{Order} \times \text{Dynamic Range}^2} \quad (21)$$

Table V. Parameters of 2nd order Butterwoth LPF.

Parameter	Simulated values
Cutoff frequency [Hz]	456
Power [nW]	248
$V_{in\text{-}pp}$@100 Hz for 1% THD [mV]	180
Input referred noise from 5–500 Hz [μV_{rms}]	160
Dynamic range [dB]	52
Cutoff frequency tuning range [Hz]	74–820

Table VI. Comparison of the designed filter with other similar works.

Parameters	[11]	[26]	[21]	[24]	[22]	[23]	This work
Technology	0.8 μm	1.2	0.35	0.18	0.35	0.13	0.18
Supply voltage (V)	1.25	±1.35	3.3	±0.9	3	0.9	0.5
Bandwidth (Hz)	100–2 K	0.3	1.5–15	1.5	1.95	25–225	74–820
Filter order	2	2	2	2	2	2	2
Filter topology	G_m-C	G_m-C	G_m-C	Opamp R–0.5R	G_m-C	G_m-C	G_m-C
$V_{\text{in-pp}}$ for 1% THD (mV)	1000	150 ($HD_3 = -45$ dB)	1000	300	762	7	180
Input referred noise (μV RMS)	178	15.6	318	114	791	17	160
Dynamic range (dB)	78–62	–	60	60	50.65	43.8	52
Power (μW)	2.5	8.18	165	0.936	6.31	0.8	0.248
FoM (pW/pole)	0.78	–	82.5	0.47	26	16.7	0.78

3.1.1. Performance Over Process Corners and V_{DD} Variations

Simulations are carried out across process corners (tt, ff, ss, fnsp and snfp) and ±10% V_{DD} variations (450 mV and 550 mV) and the effect of them on cutoff frequency of the filter are analyzed. Worst case deviation in cutoff frequency is observed in fnsp corner with $V_{\text{DD}} = 0.55$ V and in ss corner with $V_{\text{DD}} = 0.45$ V and are plotted in Figure 12. The observed variation in cutoff frequency is as low as ±2.4%.

3.1.2. Performance Over Temperature Variations

Figure 13 shows the normalized frequency response of the filter for a temperature variation in the range 0° to 70 °C. It can be seen that the deviation in cutoff of frequency the filter is ±8% up to 50 °C. These variations can be minimized by using constant-G_m bias circuit or automatic frequency tuning loop.

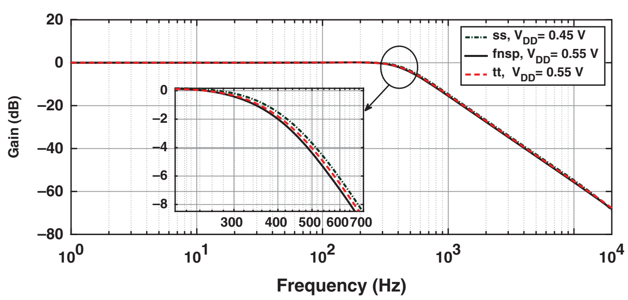


Fig. 12. Cutoff frequency variation (worst case) for various process corners and supply voltages.

It is observed that, when the temperature increases beyond 50 °C, the variation in cutoff frequency is more due to finite input impedance of the bulk-driven transconductor. To strengthen this argument, the variation in the bulk-leakage current of the input bulk-driven transistor is plotted in Figure 14 with respect to temperature. The leakage current is insignificant till about 50 °C. Beyond 50 °C, it increases drastically. At 70 °C, it is found to be 0.55 nA. Due to this leakage current, input impedance of the transconductor reduces and hence g_i increases. Till about 50 °C, input impedance is very high (g_i is low). At 70 °C, g_i is found to be 18.6 nS, which is comparable to G_m of 44.6 nS (Table IV). As G_m of the transconductor reduces with temperature (Table IV), cutoff frequency of the filter is expected to be reduced as it can be seen in (16). But, it is observed that the cutoff frequency increases by +17% at 70 °C. This can be justified by (19), which shows the effect of g_i on the cutoff frequency.

At 70°, DC-gain and Quality-factor are reduced to 0.5 (−6 dB) and 0.52 respectively. The reduction in DC-gain and Quality-factor are modeled by (18) and (20) respectively. However, the frequency response at 70 °C in Figure 13 is normalized to 0 dB for comparison purpose.

Hence, it can be inferred that at temperatures beyond 50 °C, the deviation in the frequency response is more. This can be attributed to the increased bulk-leakage current in the input bulk-driven transistors, which results

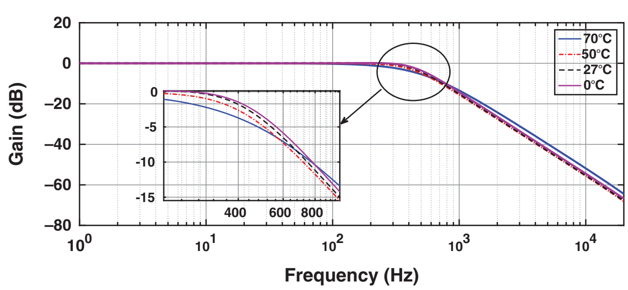


Fig. 13. Cutoff frequency variation for various temperatures.

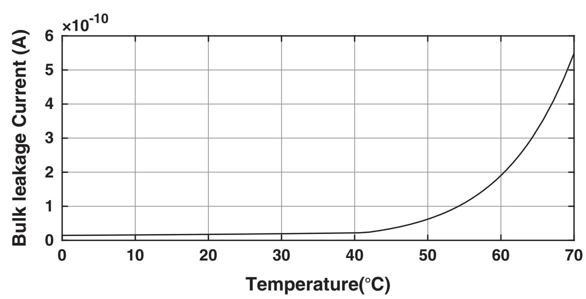


Fig. 14. Bulk leakage current of input transistor.

in decreased input impedance (increased g_i), there by affecting the cutoff frequency, quality factor and DC-gain. This can be overcome by decreasing the forward bias of bulk-source junction of input transistors, which can be done by increasing the power supply voltage and the drop across the tail current source of the transconductor. However, this can be achieved at the cost of power dissipation.

4. CONCLUSION

A fully differential low voltage, low power bulk-driven transconductor for low frequency G_m-C filters is presented. It offers 28 dB DC gain, 3.7 kHz unity gain frequency and 83° phase margin. The transconductor consumes a power of 86 nW with 0.5 V power supply. A 2nd order Butterwoth LPF with the cutoff frequency tunable from 74 Hz to 820 Hz is designed using the proposed transconductor. By adjusting the currents I_1 and I_2, the cutoff frequency can be tuned to fit into the desired frequency range of different bio-potentials. Filter has a dynamic range of 52 dB while consuming 248 nW of power for nominal cutoff frequency of 456 Hz. Filter is energy efficient with an FoM of 0.78 pW/pole. Filter is also simulated across process corners and V_{DD} variations and a deviation of only ±2.4% in the cutoff frequency is observed. Simulation results of the transconductor and filter very well match with the analytical expressions given in Sections 2.1 and 3.

Acknowledgment: The authors would like to thank Department of Information Technology, MCIT, Government of India, for the necessary tool support provided to carry out this work under SMDP, VLSI project.

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