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Minimization of Via-Induced Signal Reflection in On-Chip High Speed Interconnect Lines

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Abstract Vias are extensively used to connect different metal levels in a multilayered Integrated Circuits (IC). The impedance discontinuities at the junction of the interconnect and via results in signal reflections and create signal integrity problems. This is one of the important design issues in ICs operating at gigahertz (GHz) frequencies. In this paper, a method for the reduction of via-induced signal reflection in high-speed on-chip intermediate/global interconnect structures is proposed. Signal reflection minimization is achieved through impedance matching by the inclusion of an appropriate capacitive load at the interconnect–via junction. This method is demonstrated for a two-layer interconnect structure connected through a via. The proposed solution reduces the signal reflection to as low as −35 dB at the tuned frequency of 5 GHz and less than −10 dB in its vicinity (1 to 10 GHz). The operating frequency can be changed by tuning the matching capacitive load and hence this method can be extended to any high frequency operation by digitally tuning a bank of on-chip capacitors (without going through a new fabrication run). Further it is shown that the signal reflections are reduced considerably in a six-layer structure and hence this method can be extended to any multi-level interconnect structure.

Keywords Via · Signal reflection · Impedance matching · On-chip interconnect lines

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1 Introduction

It is a known conclusion that Moore's law still holds good even after 50 years of its inception and this trend is likely to continue for another 10 years. International Technology Roadmap for Semiconductors (ITRS) predicts that in 2015, a single IC will have more than 5 billion components with the technology node of 22 nm, 13 metal layers, on-chip performance of 10 GHz and the total interconnect length of 4000 m/cm^2 [9]. The GHz range signal propagation speed through the nano-sized devices and the interconnect structures creates signal integrity problems and is an important issue to be dealt with in today's modern VLSI design.

Impedance control over the transmission path (interconnect) is required to reduce the signal integrity problems when the signals are sent at high frequencies, typically more than 1 gigabits per second (Gbps). When the geometry of the transmission line is altered along the signal path, signal reflections are bound to occur due to impedance mismatch. Changes in the geometry of the transmission line are very common in ICs and they arise due to the inclusion of connectors, wire terminations, vias, etc. Vias are very commonly used structures to connect different metal interconnect layers and become the disruptors of impedance continuity [15, 21].

The impedance discontinuity at the junction of the on-chip intermediate/global interconnect and via results in signal reflections and contributes to the loss of signal. To increase the efficiency in the propagation of the signal, designers try to eliminate every impedance mismatch which is responsible for the introduction of skew, jitter, noise, etc. in the propagation of the signal along the high speed on-chip interconnect. Further, the improper connection of the vias between the two metal layers would create considerable voltage breakdown, signal attenuation, crosstalk, switching noise, etc. [3].

Via length is negligibly small compared to the signal wavelength at lower frequencies and hence it is either completely neglected or modeled as a combination of lumped circuit elements such as series inductors and shunt capacitors for ease of circuit analysis. When the operating frequency is in GHz range, the parasitics of via cannot be neglected and they need to be modeled as RLC structures for accurate analysis. Further, as the technology node decreases due to scaling, via resistance increases significantly [20] and it starts contributing to the signal integrity problems.

Studies on different types of vias, their properties and the impact on the propagation of signals are presented in [4, 13, 17, 19]. The capacitance of the via is extracted either from the solution of integro-differential equations [12] or from full-wave simulations [18]. Multiple via interconnect structures have been analyzed by decomposing the geometry into exterior and interior structures [8]. In addition to these, several papers describe the efficient modeling of multiple vias in high-speed interconnect circuits [16, 22].

Different techniques are reported in the literature to reduce the signal reflections in multilayered interconnect structures. In [14], it is demonstrated that the modification in the shape of the transmission line near the via reduces the signal reflections. A new type of via structure is used in [11] to reduce the signal reflection in multilayered interconnect structures. The design technique of employing an artificial neural network for constructing reflectionless via structures is proposed and validated in [7]. In [2], signal reflections are reduced by optimizing the via dimensions.

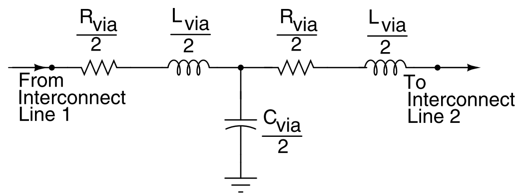

Fig. 1 Lumped RLC equivalent via model

In all these papers, the reduction in signal reflection is achieved through the modification of via structure and it is aimed at Printed Circuit Boards (PCBs). Further, in these cases the structure (geometry) of the vias once fabricated remains fixed and modification of via geometry is not feasible to suit newer frequencies of operation.

In this paper, the reduction of via-induced signal reflection in ICs is addressed by incorporating a simpler technique wherein an additional capacitance is included at the interconnect–via junction for impedance matching. This method does not require any modification to the technology-specified interconnect geometry. Via impedance is calculated from its equivalent circuit and the effect on the signal reflections at the junction of the metal interconnect line and the via is analyzed for two types of models: (i) two adjacent interconnect metal layers connected through a single via, and (ii) multi-level interconnects (layer 6 and layer 1) connected through five vias. Further, this method is amenable to frequency tunability by making use of a digitally switchable bank of capacitors in place of the single matching capacitor at the interconnect–via junction.

The rest of this paper is organized as follows. Introduction to the via structure is given in Sect. 2. In Sect. 3, expression is derived to find the value of the capacitive load to be included at the interconnect–via junction for impedance matching. Simulation results of the two-layer and six-layer interconnect models using the proposed method are given in Sect. 4. The conclusions are drawn in Sect. 5.

2 Modeling of the Via

Via is a small conductive cylindrical hole drilled from one layer to another layer that is used to make electrical connections between different interconnect levels in an IC. Via consists of structures like barrel, pad and anti-pad. The barrel is a conductive material that fills the hole to allow an electrical connection between the layers, the pad is used to connect the barrel to the component or trace and the-anti pad is a clearance hole between the pad and the metal on a layer to which no connection is required [6].

In Deep Submicron (DSM) regime, via effects are considerable and cannot be neglected. In [10], via resistance (R_{via}), via inductance (L_{via}) and via capacitance (C_{via}) are modeled as a function of physical dimensions and material characteristics of the via. A lumped *RLC* model represented in the form of **T** network as the equivalent of a via is shown in Fig. 1. Voltage drop between the interconnected nodes of the two metal layers is caused by R_{via}, L_{via} and the capacitive component C_{via} seen between the via and the ground. The expressions to estimate the resistance, inductance and

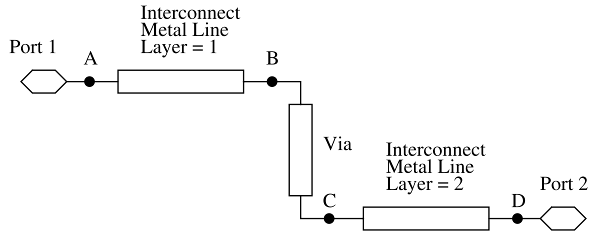

Fig. 2 Model of the two interconnect layers connected through a via

capacitance values of the via equivalent circuit are given in (1), (2) and (3) [10].

$$R_{\text{via}} = \frac{\rho h_{\text{via}}}{\pi r_{\text{via}}^2}, \tag{1}$$

$$L_{\text{via}} = \frac{\mu_0}{4\pi}\left[h_{\text{via}} \ln\left(\frac{2h_{\text{via}} + \sqrt{r_{\text{via}}^2 + (2h_{\text{via}})^2}}{r_{\text{via}}}\right) + \left(r_{\text{via}} - \sqrt{r_{\text{via}}^2 + (2h_{\text{via}})^2}\right)\right], \tag{2}$$

$$C_{\text{via}} = \frac{2\pi \varepsilon_r \varepsilon_0 h_{\text{via}}}{\ln((r_{\text{via}} + t_{\text{via}})/r_{\text{via}})}, \tag{3}$$

where ρ is the resistivity of the conducting material, r_{via}, h_{via}, and t_{via} represent the radius, length and dielectric thickness of the via, respectively. The permeability constant, or free space permeability, is represented by μ_0 and is a measure of the amount of resistance encountered when forming magnetic field in vacuum and has constant value of $4 \times \pi \times 10^{-7}$ H/m. The terms ε_r and ε_0 represent relative permittivity of the material and free space permittivity. Free space permittivity is defined as $\varepsilon_0 = 1/(\mu_0 c_0^2) = 8.852 \times 10^{-12}$ F/m where c_0 is the speed of light in vacuum ($=3 \times 10^8$ m/s).

3 Impedance Matching at Interconnect–Via Junction

Figure 2 shows the model of the two metal interconnect layers (L_1 and L_2) connected through a single via. When an electromagnetic wave propagates from interconnect line to via with differing characteristic impedance, two things happen: (i) a portion of the wave is reflected away from the impedance discontinuity back to the source, and (ii) a portion of the wave is transmitted through the via. The simultaneous existence of both the transmitted and reflected waves is a direct result of the boundary conditions that must be satisfied when solving Maxwell's equations at the interface between the two regions [6].

When the plane wave is propagating in the transverse electromagnetic (TEM) mode, the difference of the incident and reflected waves must equal to the transmitted wave, i.e.

$$v_t = v_i - v_r, \tag{4}$$

$$\frac{i_t}{Z_{\text{via}}} = \frac{i_i}{Z_0} - \frac{i_r}{Z_0}, \tag{5}$$

where v_i, v_r, v_t, i_i, i_r and i_t are the incident, reflected and transmitted voltage and current waves, respectively. Z_0 is the characteristic impedance of the transmission line and Z_{via} is the impedance of the via equivalent circuit.

Since the incident waves are known, (4) and (5) are solved simultaneously for the transmitted and reflected portions of the wave. The expressions for v_t and v_r are given by

$$v_t = v_i \frac{2Z_{\text{via}}}{Z_{\text{via}} + Z_0}, \tag{6}$$

$$v_r = v_i \frac{Z_{\text{via}} - Z_0}{Z_{\text{via}} + Z_0}. \tag{7}$$

The reflection coefficient (Γ) is a measure of how much of the signal is reflected back by the intersection between the two impedance regions and the transmission coefficient (ξ) tells how much of the wave is transmitted. From (6) and (7),

$$\Gamma = \frac{v_r}{v_i} = \frac{Z_{\text{via}} - Z_0}{Z_{\text{via}} + Z_0}, \tag{8}$$

$$\xi = \frac{v_t}{v_i} = \frac{2Z_{\text{via}}}{Z_{\text{via}} + Z_0}. \tag{9}$$

For implementation, interconnect metal lines are treated as microstrip lines and the characteristic impedance is calculated using (10) [5].

$$Z_0 = \sqrt{\frac{\varepsilon_0 \mu_0}{\varepsilon_{\text{eff}}}} \frac{1}{C_a}, \tag{10}$$

where

$$C_a = \begin{cases} \frac{2\pi\varepsilon_0}{\ln(8h/w_e + w_e/4h)}, & \frac{w_e}{h} \le 1, \\ \varepsilon_0\left[\frac{w_e}{h} + 1.393 + 0.667\ln\left(\frac{w_e}{h} + 1.444\right)\right], & \frac{w_e}{h} > 1, \end{cases} \tag{11}$$

$$\varepsilon_{\text{eff}} = \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{w_e}\right)^{-1/2}\right], \tag{12}$$

$$w_e = \begin{cases} w + 0.398t(1 + \ln\frac{4\pi w}{t}), & \frac{w}{h} \le \frac{1}{2\pi}, \\ w + 0.398t(1 + \ln\frac{2h}{t}), & \frac{w}{h} > \frac{1}{2\pi}. \end{cases} \tag{13}$$

In (10), C_a and ε_{eff} represent the distributed capacitance in an air-filled microstrip line and the effective dielectric constant of the microstrip. The terms C_a and ε_{eff} are defined as shown in (11) and (12). In (11) and (13), w, t, h and w_e represent width, thickness of the conductor, substrate thickness, and effective width that accounts for the extra capacitance caused by the finite thickness of the signal conductor, respectively. Electric field lines will be established between the edge of the conductor

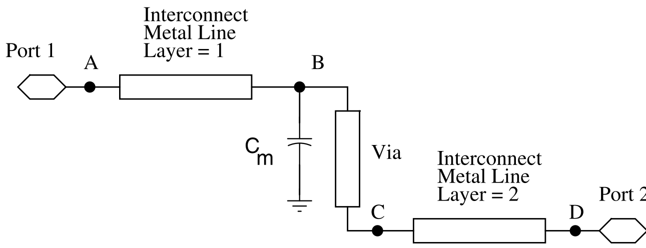

Fig. 3 Proposed method to reduce the signal reflection in the model of the two interconnect layers connected through a via

and the reference plane, thicker signal conductors exhibiting increased capacitance. Hence, the effective width w_e is slightly wider than the physical width w to account for the extra capacitance.

Figure 3 shows the proposed method used to reduce the signal reflection in the model of the two interconnect layers connected through a via. A matching capacitive load C_m is added at the interconnect–via junction. The input impedance Z_{in} seen from the right terminal of the first interconnect layer (point B in Fig. 2) is computed by replacing the via in Fig. 2 by its equivalent circuit given in Fig. 1. Thus, Z_{in} is given by

$$Z_{\text{in}} = \left(\frac{R_{\text{via}} + j\omega L_{\text{via}}}{2}\right) + \left[\frac{1}{j\omega C_{\text{via}}} \parallel \left(\frac{R_{\text{via}} + j\omega L_{\text{via}}}{2} + Z_{02} + \left(\frac{1}{j\omega C_L} \parallel Z_{t2}\right)\right)\right] \tag{14}$$

where Z_{02} is the characteristic impedance of the second interconnect layer, Z_{t1} and Z_{t2} are the terminating resistances used for S parameter analysis at the input and output side of the structure (4) and C_L is the load capacitance.

Simplifying (14),

$$Z_{\text{in}} = x + \frac{1}{j\omega C_{\text{via}} + \frac{1}{x + Z_{02} + \frac{Z_{t2}}{j\omega C_L Z_{t2} + 1}}}, \tag{15}$$

where

$$x = \frac{R_{\text{via}} + j\omega L_{\text{via}}}{2}.$$

The signal reflection is minimum when the characteristic impedance of the microstrip line matches with the via impedance. The values of R_{via}, L_{via} and C_{via} for 65-nm technology node are computed using (1) to (3) and are found to be equal to 3.5 Ω, 26.09 pH and 113.98 fF, respectively. For contemporary through silicon via architectures, the inductive voltage drop is found to exceed resistive voltage drop for frequencies above 3 GHz [10] and hence the via structure can be assumed to behave predominantly as an inductive load. In such a scenario, matching between the

Table 1 Interconnect layer thickness, width and spacing

Layer	Thickness (μm)	Width (μm)	Spacing (μm)
Metal 1	0.20	0.13	0.10
Metal 2	0.25	0.15	0.10
Metal 3	0.30	0.17	0.10
Metal 4	0.50	0.28	0.05
Metal 5	0.80	0.40	0.05
Metal 6	1.20	0.60	0.02

interconnect and the via can be easily achieved by connecting an appropriate matching capacitance between point B and ground as in Fig. 3. The equivalent new input impedance seen from point B in Fig. 3 is given by

$$Z_{\text{match}} = \left(\frac{1}{j\omega C_m} \parallel Z_{\text{in}}\right). \tag{16}$$

Substituting the expression for Z_{in} into (16) and simplifying, the expression for C_m is given by

$$C_m = \frac{1}{j\omega}\left[\frac{1}{Z_{\text{match}}} - \frac{1}{x + \frac{(a+jb)}{(c+jd+1)}}\right], \tag{17}$$

where

$$x = \frac{R_{\text{via}} + j\omega L_{\text{via}}}{2},$$

$$a = R_{\text{via}} - \omega^2 L_{\text{via}} C_{\text{via}} Z_{t2} + 2Z_{02} + 2Z_{t2},$$

$$b = R_{\text{via}} C_L Z_{t2} + L_{\text{via}} + 2Z_{02} C_L Z_{t2},$$

$$c = -\omega^2 C_{\text{via}} (R_{\text{via}} C_L Z_{t2} + L_{\text{via}} + 2Z_{02} C_L Z_{t2}),$$

$$d = \omega C_{\text{via}} (R_{\text{via}} - \omega^2 L_{\text{via}} C_L Z_{t2} + 2Z_{02} + 2Z_{t2}).$$

The value of C_m is adjusted for minimum signal reflection (maximum impedance matching) for a given operating frequency.

4 Simulation Results

Models of two- and six-layer interconnect structures are created using Advanced Digital System (ADS) software. S-parameter analysis is used to analyze the signal reflection at the input and output side of the created model. Interconnect parameters of 65-nm technology node are used in the simulations and are listed in Table 1 [1].

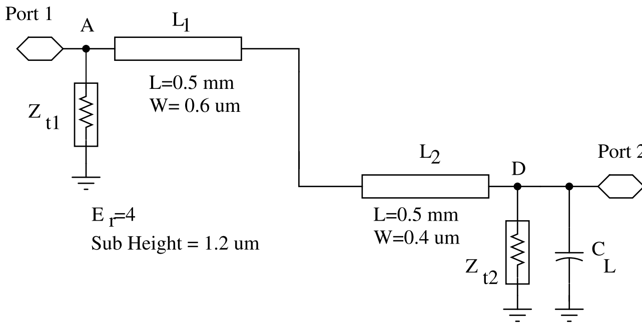

Fig. 4 Arrangement used to simulate the model of two directly connected interconnect layers

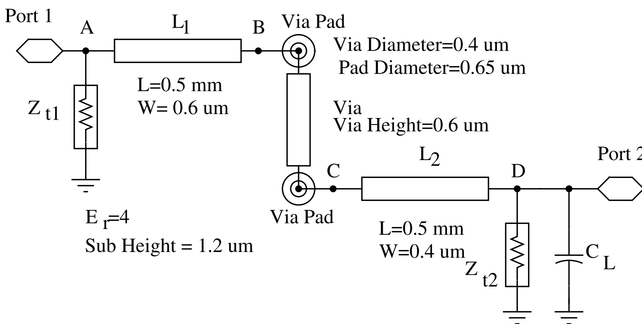

Fig. 5 Arrangement used to simulate the model of two interconnect layers are connected with a via

4.1 Signal Reflection Reduction in a Two-Layer Interconnect Structure

Figures 4 and 5 show the arrangements used to perform S-parameter analysis. In Fig. 5, the following via dimensions are considered: via diameter of 0.4 μm, pad diameter of 0.65 μm, via height of 0.4 μm and dielectric thickness 1 μm. A transmitter and a receiver are connected using such an interconnect. The receiver section is modeled as load capacitance (C_L). In the simulations, the considered values of the metal length, load capacitance C_L, terminating resistances Z_{t1} and Z_{t2} are 0.5 mm, 0.25 pF, 76 Ω and 88 Ω, respectively.

The effect of via on signal reflection can be seen by comparing the S-parameter analysis of two-layer interconnect structures—one in which the metal layers are directly connected as in Fig. 4 (not practical in real scenario) and the other through a via (as in Fig. 5). Figure 6 shows the signal reflection (parameter S_{11}) measured at point A in Figs. 4 and 5. From Fig. 6 it can be seen that up to a frequency of 10 GHz, there is a significant increase in the signal reflection in the structure employing via in comparison to the structure without a via. This is due to the impedance mismatch between the interconnect layer and the via.

An equivalent of the via lumped RLC model represented in the form of **T** network is shown in Fig. 1. Figure 7 shows the input signal reflection at point A in Fig. 5

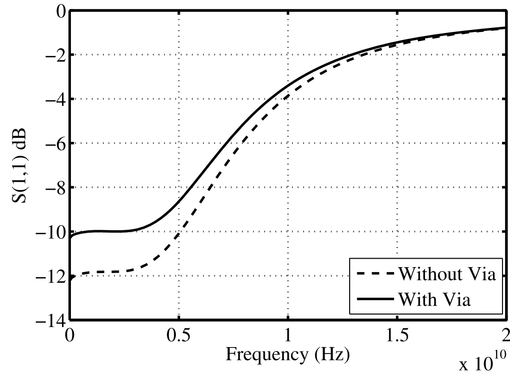

Fig. 6 Effect on the signal reflection in the model of two interconnect layers with and without via

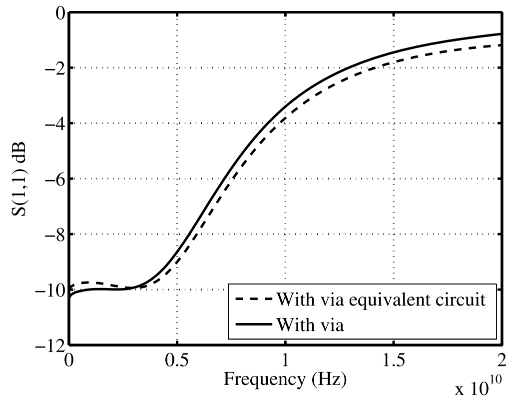

Fig. 7 Signal reflection in the two-layer interconnect model with via and its equivalent circuit

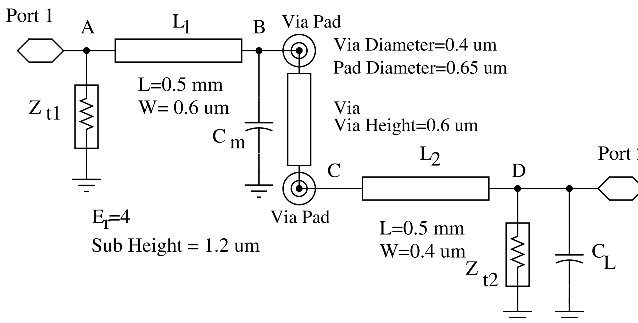

Fig. 8 Arrangement used to reduce the signal reflection in the two-layer interconnect model connected through a via

with via and its equivalent model. Results show that both the responses are closely matching. Hence the model shown in Fig. 1 can be used as the equivalent of the via.

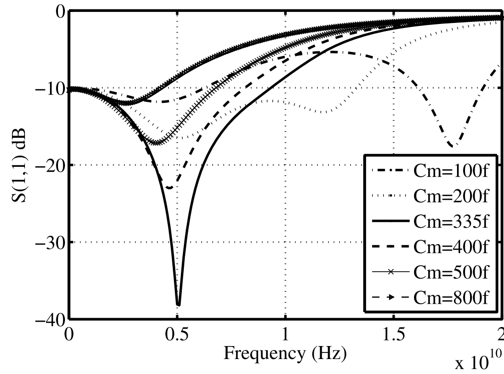

Fig. 9 Signal reflection for different matching capacitance values

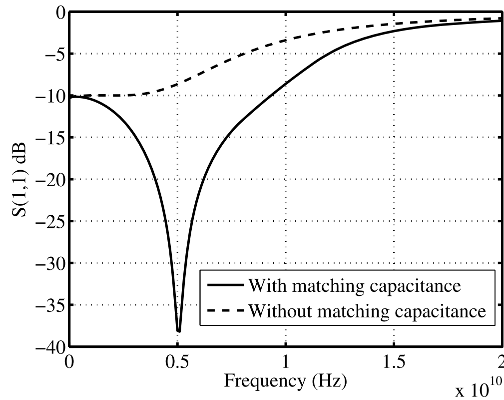

Fig. 10 Signal reflection with and without capacitance in the two-layer interconnect model

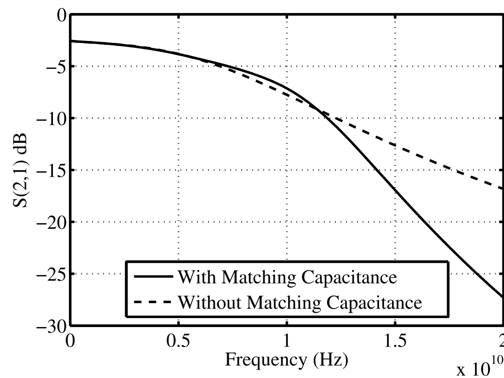

Fig. 11 Transmission loss with and without capacitance in the two-layer interconnect model

The arrangement to mitigate the signal reflection at the junction of the interconnect and the via is shown in Fig. 8. Figure 9 shows the signal reflections at the input side (point A in Fig. 8) for different capacitance (C_m) values.

It is observed that the minimum signal reflection point is dependent on the matching terminating resistances at the input (Z_{t1}) and output side (Z_{t2}) of the structure

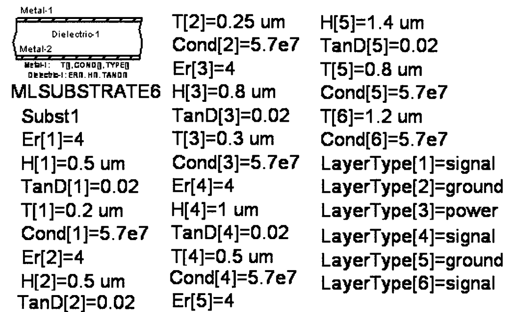

Fig. 12 ADS setup for the simulation of 6-layer structure

and the matching capacitance C_m. In this work, we are interested to have low signal reflections in the range 1–10 GHz. By keeping the minimum signal reflection point at 5 GHz with $Z_{t1} = 76\ \Omega$ and $Z_{t2} = 88\ \Omega$, the theoretical value (see (17)) of C_m is found to be 345 fF. From the simulations, the matching capacitance value is found to be 335 fF at 5 GHz (Fig. 9).

Figures 10 and 11 show the signal reflection (S_{11}) and transmission loss (S_{21}) at point A with and without matching capacitance (at point B in Fig. 8). From Fig. 10 it can be seen that there is a clear advantage in using a matching capacitance to reduce signal reflections.

4.2 Applying the Proposed Method to a Six-Layer Structure

Analysis of the proposed method is made for a six-layer interconnect structure in which the two interconnect metal lines are connected from layer 6 to layer 1 through five vias. The ADS setup for creating a six-layer structure is given in Fig. 12. The values of the relative dielectric constant of the substrate (ε_r[n]), height of substrate (H[n]), dielectric loss tangent (TanD[n]), metal thickness (T[n]), conductivity (Cond[n]) and type of the metal layer (LayerType[n]) are listed in Fig. 12.

Capacitances are added at the junctions of each interconnect layer and the via. The arrangement for the connection of two interconnect lines from layer 6 to layer 1 through vias is shown in Fig. 13. Vias are connected with suitable dimensions which are matching with the width of the corresponding interconnect layers.

Figures 14 and 15 show the signal reflection and the transmission loss (in this case, S_{31}) with and without capacitance in a six-layer structure. It can be seen that there is a significant improvement in signal reflection and transmission loss with the addition of the matching capacitances.

In multilayered structure, signal lines are surrounded by ground/power lines for the minimization of crosstalk. Hence the matching capacitances can be easily connected between the ground plane and the junction of the interconnect layer and the via. The matching capacitances (C_m) can be realized using MOS devices. Since the value of C_m is moderate, the area consumed by these capacitors is not very significant.

4.3 Scope for Frequency Tunability

The proposed method can be used to reduce the signal reflection at the junction of the metal interconnect layer and the via for different frequencies of operation. Figure 16

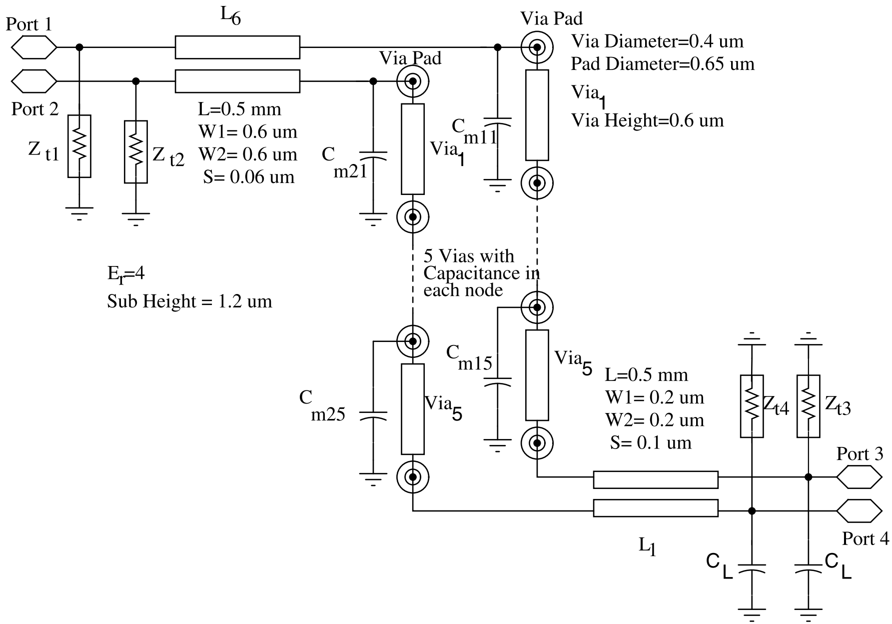

Fig. 13 Interconnect layer 6 is connected to layer 1 through five vias with capacitance in each junction

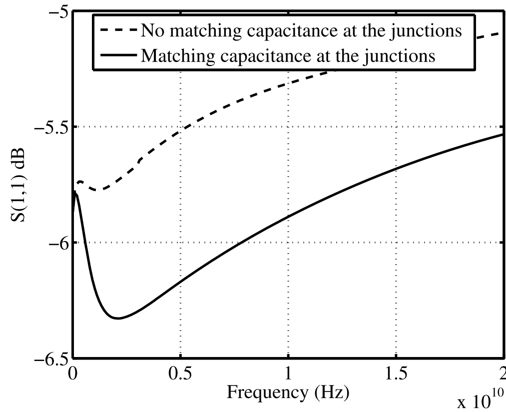

Fig. 14 Signal reflection with and without capacitance in a six-layer structure

shows the arrangement of the frequency-tunable signal reflection reduction for the model of two interconnect layers connected through a via. A bank of capacitors (C_{m1} to C_{mn}) are connected through digitally controlled switches (S_1 to S_n) in place of the matching capacitance at the junction of the metal layer and the via. Depending upon the frequency of operation, switches are digitally turned on so that the resulting capacitance value from the bank of capacitors is just right for the impedance matching. This method helps to reduce the signal reflection for a broad range of frequencies of operation. Switches as well as the capacitors can be realized using MOS devices and hence this method does not require any additional fabrication run to incorporate

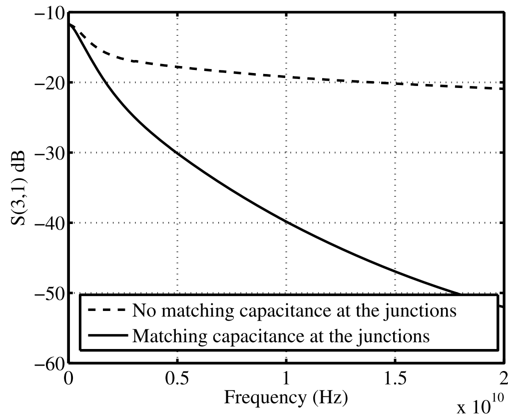

Fig. 15 Transmission loss with and without capacitance in a six-layer structure

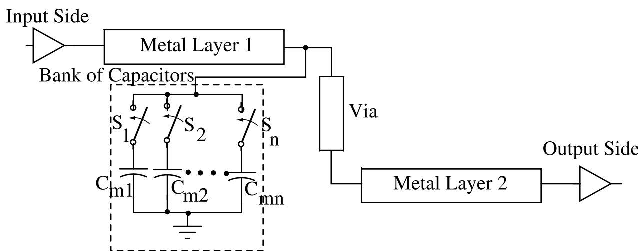

Fig. 16 Arrangement for the frequency-tunable signal reflection reduction

tuning. However, care must be taken to minimize the parasitic effect of the switches on signal transmission.

5 Conclusion

S-parameter analysis shows that when two metal interconnect layers are connected through a via, signal reflection takes place at high frequencies of operation due to impedance mismatch at the junction of the interconnect and the via. In this paper, a method is proposed to reduce the signal reflection by adding a matching capacitance at the interconnect–via junction. The matching capacitance value is analytically computed and is found to be in close agreement with the simulation results. In the two-layer interconnect model, signal reflections are reduced to less than −10 dB in the frequency range of 1 to 10 GHz and is below −35 dB at the tuned frequency of 5 GHz. The proposed method is applied to a six-layer interconnect structure and the signal reflection is found to reduce considerably. The above method can be extended to different operating frequencies by incorporating digitally tunable capacitive loading.

References

1. P. Bai, C. Auth, S. Balakrishnan, M. Bost, R. Brain, V. Chikarmane, R. Heussner, M. Hussein, J. Hwang, D. Ingerly et al., A 65 nm logic technology featuring 35 nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low k ILD and 0.57 μ^2 SRAM cell, in *IEEE International Electron Devices Meeting* (2005), pp. 657–660
2. R.W.Y. Chang, K.Y. See, E.K. Chua, Comprehensive analysis of the impact of via design on high-speed signal integrity, in *9th Electronics Packaging Technology Conference* (2007), pp. 262–266
3. H. Chen, Q. Li, L. Tsang, C.C. Huang, V. Jandhyala, Analysis of a large number of vias and differential signaling in multilayered structures. IEEE Trans. Adv. Packag. **51**(3), 818–829 (2003)
4. Q. Gu, Y.E. Yang, M.A. Tassoudji, Modeling and analysis of vias in multilayered integrated circuits. IEEE Trans. Microw. Theory Tech. **41**(2), 206–214 (2002)
5. S.H. Hall, H.L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs* (Wiley, New York, 2009)
6. S.H. Hall, G.W. Hall, J.A. McCall, *High Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices* (Wiley, New York, 2000)
7. K.T. Hsu, G.H. Shiue, C.M. Lin, T.W. Huang, R.B. Wu, Design of reflectionless vias using neural network-based approach. IEEE Trans. Adv. Packag. **31**(1), 211–218 (2008)
8. C.C. Huang, K.L. Lai, L. Tsang, X. Gu, C.J. Ong, Transmission and scattering on interconnects with via structures. Microw. Opt. Technol. Lett. **46**(5), 446–452 (2005)
9. Interconnect Technology 2007 Report, http://itrs.net/Interconnect.pdf
10. G. Katti, M. Stucchi, K. De Meyer, W. Dehaene, Electrical modeling and characterization of through silicon via for three-dimensional ICs. IEEE Trans. Electron Devices **57**(1), 256–262 (2009)
11. Y.W. Kim, J.H. Kim, H.W. Yang, O.K. Kwon, C. Ryu, B.Y. Min, A new via hole structure of MLB (multi-layered printed circuit board) for RF and high speed systems, in *Proceedings of the Electronic Components and Technology Conference* (2005), pp. 1378–1382
12. P. Kok, D. De Zutter, Capacitance of a circular symmetric model of a via hole including finite ground plane thickness. IEEE Trans. Microw. Theory Tech. **39**(7), 1229–1234 (2002)
13. P.A. Kok, D. De Zutter, Scalar magnetostatic potential approach to the prediction of the excess inductance of grounded vias and vias through a hole in a ground plane. IEEE Trans. Microw. Theory Tech. **42**(7), 1229–1237 (2002)
14. D.H. Kwon, J. Kim, K.H. Kim, S.C. Choi, J.H. Lim, J.H. Park, L. Choi, S.W. Hwang, S.H. Lee, Characterization and modeling of a new via structure in multilayered printed circuit boards. IEEE Trans. Compon. Packag. Technol. **26**(2), 483–489 (2003)
15. E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu, D. Morlion, Modeling complex via hole structures. IEEE Trans. Adv. Packag. **25**(2), 206–214 (2002)
16. E.X. Liu, E.P. Li, Z.Z. Oo, X. Wei, Y. Zhang, R. Vahldieck, Novel methods for modeling of multiple vias in multilayered parallel-plate structures. IEEE Trans. Microw. Theory Tech. **57**(7), 1724–1733 (2009)
17. S. Maeda, T. Kashiwa, I. Fukai, Full wave analysis of propagation characteristics of a through hole using the finite-difference time-domain method. IEEE Trans. Microw. Theory Tech. **39**(12), 2154–2159 (2002)
18. T. Onojima, T. Kashiwa, N. Yoshida, I. Fukai, Three-dimensional analysis of a through hole with radiation characteristics by the spatial network method. IEEE Trans. Microw. Theory Tech. **38**(6), 770–778 (2002)
19. J.P. Quine, H.F. Webster, H.H. Glascock, R.O. Carlson, Characterization of via connections in silicon circuit boards. IEEE Trans. Microw. Theory Tech. **36**(1), 21–27 (2002)
20. E. Sicard, S.D. Bendhia, *Basics of CMOS Cell Design* (McGraw-Hill, New York, 2007)
21. T. Wang, R.F. Harrington, J.R. Mautz, Quasi-static analysis of a microstrip via through a hole in a ground plane. IEEE Trans. Microw. Theory Tech. **36**(6), 1008–1013 (2002)
22. B. Wu, L. Tsang, Modeling multiple vias with arbitrary shape of antipads and pads in high speed interconnect circuits. IEEE Microw. Wirel. Compon. Lett. **19**(1), 12–14 (2009)