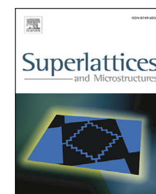
Superlattices and Microstructures 112 (2017) 654–664

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices



Optoelectronic properties of hybrid diodes based on vanadyl-phthalocyanine and zinc oxide

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A R T I C L E I N F O

Article history:
Received 17 August 2017
Received in revised form 27 September 2017
Accepted 19 October 2017
Available online 23 October 2017

Keywords:
Impedance spectroscopy
Cole-cole plot
Charge transport
Hybrid diode
Phthalocyanine
Mobility

A B S T R A C T

We report an investigation of the optoelectronic properties of a hybrid p-n diode device fabricated using ZnO film prepared by sol-gel technique on which a VOPc organic film is deposited by vacuum evaporation. The charge transport properties of devices having the configurations ITO/ZnO/Al and ITO/ZnO/VOPc/MoO_3/Al were investigated at different annealing temperatures (150 °C, 250 °C, 350 °C and 450 °C) by Impedance Spectroscopy (IS). The structural, morphological, optical and electrical properties were also studied at different annealing temperatures. The parameters related to the ITO/ZnO and ZnO/VOPc interfaces such as ideality factor (n), barrier height ($q\phi_B$) and rectification ratio (RR) of the diodes were determined from current density-voltage (J-V) characteristics. IS measurements suggest that the large photocurrent generated is due to the decrease in bulk resistance of the device on account of the generation of electron-hole pairs in the organic active layer when exposed to light. The RR and the photocurrent responsivity (R_{ph}) values obtained from the J-V characteristics compare well with those obtained from the IS measurements. It was observed that the absolute value of R_{ph} (470 mA/W) for the p-n diode with ZnO annealed at 350 °C is high compared to that of diodes with different ZnO annealing temperatures. These values also agree well with the values obtained for p-n diodes of other phthalocyanines. Our studies clearly demonstrate that a p-n diode with ZnO film annealed at 350 °C exhibits much better optoelectronic characteristics on account of increased grain size, improved charge injection due to the reduction of barrier height and hence higher (up to 5 orders) charge carrier mobility.

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1. Introduction

Organic-inorganic hybrid diodes have been of interest in optoelectronic applications in recent years. They are seen to play a prominent role in devices such as light emitting diodes, solar cells and photodiodes [1–4]. In such hybrid diodes, one can exploit the advantages of both organic and inorganic materials. Inorganic semiconductors, such as Zinc Oxide (ZnO) and Titanium oxide (TiO_2), are stable n-type semiconductors and have high electron mobility (5–6 $cm^2 V^{-1} s^{-1}$) compared to organic semiconductors (10^{-5} to 1 $cm^2 V^{-1} s^{-1}$) [5]. On the other hand, organic p-type semiconductors (phthalocyanines, pentacene, and P3HT) are known to have broad absorption spectra in the visible region which can lead to high efficiency in photodiodes and solar cells [6–8]. Moreover, these devices can be easily fabricated at low cost, even on flexible substrates [9].

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https://doi.org/10.1016/j.spmi.2017.10.023
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Hybrid interfaces of ZnO with organic semiconductors have been recently studied by several groups to explore their suitability in applications such as photodiodes [4,8,10–14].

Apart from planar interfaces with ZnO films, various nano structures of ZnO (particles, rods, tubes, wires, belts etc.) have been explored due to their potential applications in various miniaturized devices. Due to the ease of synthesis, high surface area and superior optoelectronic properties, ZnO nanoparticles have been widely exploited. Since a p-n junction is fundamentally important in all semiconductor devices, it is imperative to understand the role of quality of the junction on charge transport, in order to achieve high device performance. In devices involving ZnO/organic semiconductor interfaces, the effect of annealing of ZnO layer on the interface properties have not been explored much.

In this work, we have investigated the optoelectronic properties of hybrid diodes involving ZnO and Vanadyl-phthalocyanine (VOPc), a well-known metal phthalocyanine (MPc). MPcs possess relatively good electronic properties, are inexpensive and exhibit high environmental stability [15,16]. ZnO/MPc photodiodes have been well investigated [17–19]. Our specific choice of VOPc was based on the fact that it is a non-planar phthalocyanine molecule and is known to offer better performance in comparison to planar phthalocyanines [20–22]. Further, VOPc is commonly employed as a hole transport material [23]. To the best of our knowledge, photodiodes based on ZnO/VOPc combination has not been investigated so far. In an earlier work on hole transport through the VOPc thin films, we have shown that films deposited at low rates are better for optoelectronic applications [24]. Here, we first investigate the effect of ZnO film annealing at different temperatures on the charge transport properties of ITO/ZnO/Al electron only devices. Subsequently, we also report the fabrication and electrical characterization of p-n junctions with the configuration, ITO/ZnO/VOPc/MoO_3/Al, under dark and illuminated conditions. These investigations were carried out with the motivation of understanding charge carrier dynamics at ITO/ZnO and ZnO/VOPc interfaces and its effect on the charge transport.

1.1. Experimental details

The schematic of the proposed devices is shown in Fig. 1.

1.2. Preparation of ZnO thin films and fabrication of electron only devices

ZnO nano-particulate thin films were prepared by sol-gel spin coating technique similar to the method used in our previous study [25]. The precursor was prepared by dissolving 4 g of zinc acetate dehydrate [Zn $(CH3COO)_2 \cdot 2H_2O$] in 50 ml of 2-methoxy ethanol. This colloidal solution was stirred for 1 h on pre-heated hot plate (70 °C), and 1.2 ml of monoethanolamine (MEA; acts as a stabilizer) was added drop-wise for about 10 min and the mixture was stirred for about 2 h. The resulting clear solution was aged (48 h) at room temperature to form a gel. The aged sol-gel was spin coated on pre-cleaned and UV-Ozone treated (15 min) patterned ITO coated glass substrates at a spin rate of 500 rpm for first 30s and 1000 rpm for next 30s. The deposited film was baked at 120 °C for 10 min and the process is repeated three times to achieve desired thickness. These films were further annealed in air at either 150 °C, 250 °C, 350 °C or 450 °C for about 1 h. Thickness of the films was about 200 $\pm$ 10 nm as measured by spectral reflectometry technique.

For the fabrication of single layer devices, a 100 nm thick aluminium (Al) electrode layer was thermally evaporated on the pre-coated (and annealed) ZnO at a rate of 5–6 Å/s using a shadow mask.

1.3. Fabrication of hybrid p-n junction diode

VOPc (dye content > 85%) was procured from Alfa Aesar and was used without any further purification. A 100 nm thick VOPc layer was deposited on ZnO thin films by thermal evaporation at a base pressure of 8×10^{-6} mbar at a deposition rate of 0.1–0.2 Å/s. Subsequently, a thin layer of Molybdenum Oxide (MoO_3, 3 nm) was deposited at a rate of 0.1–0.2 Å/s to facilitate better hole injection. Finally, a 100 nm thick Al layer (electrode) was deposited as described earlier for the electron only devices.

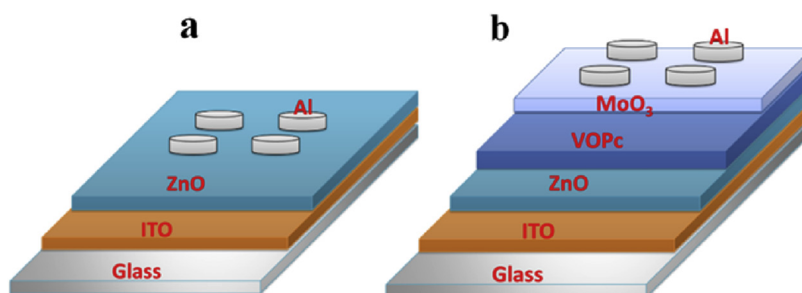

Fig. 1. (a) Schematic of electron only device and (b) schematic for hybrid diode.

To confirm the crystalline phase of ZnO, X-ray diffraction (XRD) studies were carried out (Rigaku MiniFlex 600) with Cu-K_{α} (1.5406 Å) radiation. Optical band gap of ZnO was determined from UV–Vis transmission spectra, obtained using Ocean Optics SD2000 spectrophotometer in the wavelength range 250–850 nm. Surface morphology of the ZnO films was obtained using FESEM. Current density-voltage (J-V) measurements were carried out in dark and under illumination, using a 20 mW/cm^2 (Mercury Halide lamp), with a programmable Keithley 2400SMU. Impedance spectroscopy studies were done using Agilent E4980a LCZ meter in the frequency range of 20 Hz to 1 MHz keeping the ac amplitude fixed at 100 mV. All the measurements were performed at room temperature and under ambient conditions without any encapsulation of the devices.

2. Results and discussion

ZnO films, prepared on glass substrates, were annealed at different temperatures. Their XRD patterns are shown in Fig. 2(a). The results confirm that, the samples are crystallized in hexagonal wurtzite structure [JCPDS 36-1451]. As the annealing temperature is increased, the XRD peaks become sharper, indicating better crystallinity of the synthesized samples. The predominant XRD peaks at $2\theta = 31°, 34°, 36°$ and $54°$ are assigned to (110), (002), (010) and (110) planes. The estimated nanoparticles/grain sizes in the thin films, calculated from Scherrer's formula, are presented in Table 1. The SEM images of the ZnO films annealed at different temperatures are shown in Fig. 2(b). It can be clearly seen that the ZnO nanoparticles (grain) size increases with the increase in annealing temperatures. The particles sizes obtained from the SEM images agree well with the values estimated from XRD spectra.

2.1. Electron only devices

Fig. 3(a) shows energy level diagram of the proposed devices with ZnO as an active layer. The valence band (VB)-conduction band (CB) energy levels of ZnO and the work function of ITO and Al have been taken from the literature [26–28]. The energy difference (ΔE_{FC}) between the work function of ITO and the CB of ZnO is less compared to the energy difference (ΔE_{FV}) between work function of ITO and the VB of ZnO. Hence, it is concluded that electron injection dominates at the ITO/ZnO junction.

The room temperature J-V characteristics of the devices fabricated using ZnO films annealed at different temperatures are shown in Fig. 3(b). Clearly, the devices annealed at 150 °C, 250 °C and 350 °C show rectification behaviour and the corresponding rectification ratios (RR) of the three devices, at a bias voltage of 1.5 V, are found to be 1.89, 2.77 and 5.53, respectively. It was also found that the device with ZnO film annealed at a temperature of 450 °C did not show any rectification. The characteristic diode equation under forward bias greater than a few millivolts is given by Refs. [19,29].

$$I = I_0\, exp\left(\frac{V}{nV_t}\right) \tag{1}$$

where $\boldsymbol{V_t}$ is the thermal energy at 300 K (~26 meV), $\boldsymbol{V}$ is the applied bias, $\boldsymbol{n}$ is the diode ideality factor. $\boldsymbol{I_0}$ is the reverse saturation current which can be expressed as [10].

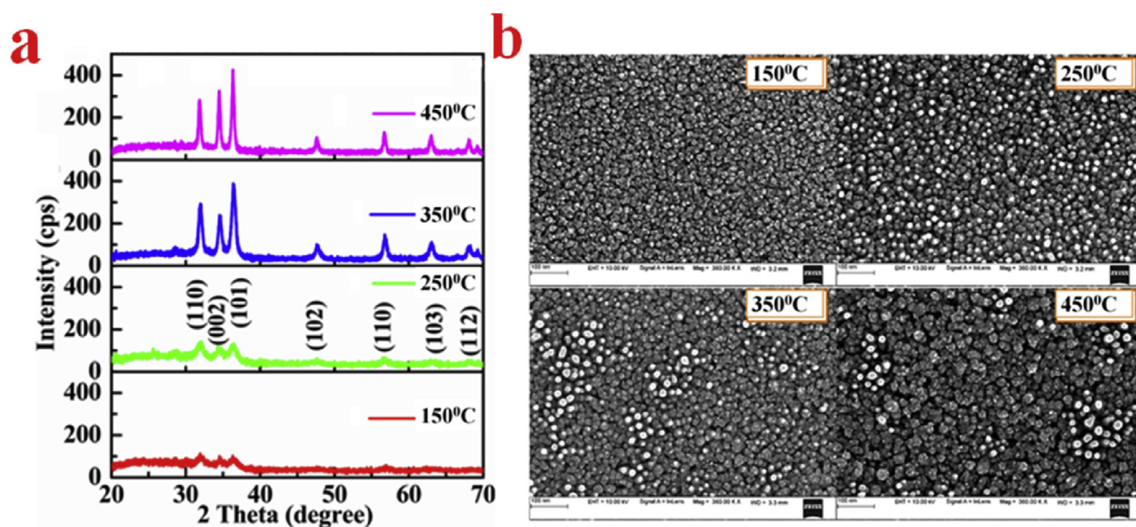

Fig. 2. (a) XRD pattern of ZnO films at different annealing temperatures and (b) SEM images, on 100 nm scale, of ZnO films on glass annealed at different temperatures.

Table 1
Estimated diode parameters form J-V, C-V and impedance characteristics for single layer electron-only devices.

Sample condition	Grain size (nm)		Ideality factor(n)	Reverse saturation current (I_0)	Barrier height (meV)	R.R @1.5 V	Mobility (cm^2/V-s)	DOS eV^{-1} cm^{-3}	Carrier density (cm^{-3})	V_{bi} (V)
	XRD	SEM								
150 °C	8	11	7.2	1.2×10^{-8}	550	1.89	3.22×10^{-10}	3.2×10^{17}	8.0×10^{17}	3.70
250 °C	11	15	6.7	9.0×10^{-8}	497	2.77	4.19×10^{-8}	4.2×10^{17}	1.3×10^{18}	3.55
350 °C	16	17	8.4	4.9×10^{-5}	333	5.53	4.16×10^{-5}	5.4×10^{17}	2.1×10^{19}	1.17
450 °C	25	21	–	–	–	–	–	–	–	–

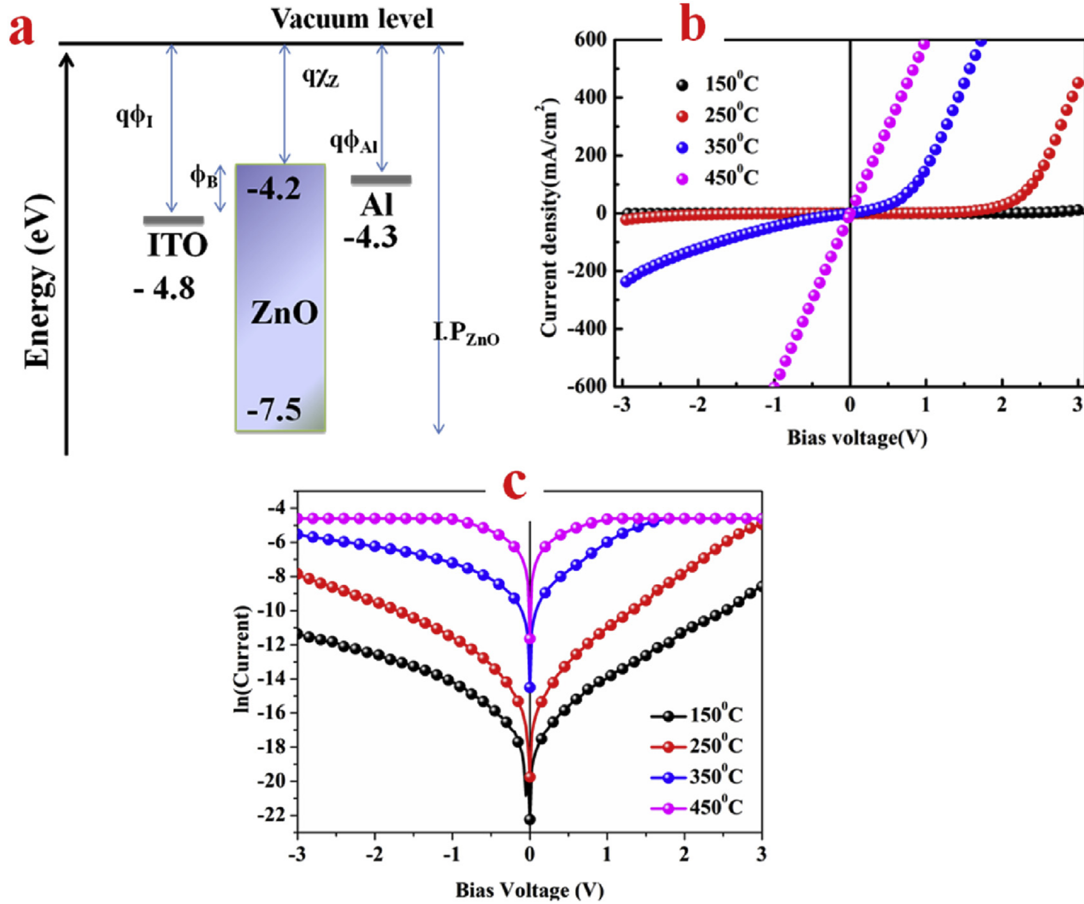

Fig. 3. (a) Energy level representation of the electron only devices with ITO/ZnO/Al configuration. Here, $q\phi_I$, $q\phi_{Al}$ and $q\chi_z$ represent the work functions of ITO, Al and the electron affinity of ZnO, respectively. IP_{ZnO} is the ionization potential of ZnO; (b) J-V characteristics of the single layer devices at different annealing temperatures; (c) I-V characteristics of the single layer devices.

$$I_0 = AA^* T^2 exp\left(\frac{q\phi_B}{kT}\right) \quad (2)$$

Here, A is the area of the device (1.6×10^{-2} cm^2), A* is the effective Richardson's constant (1.3×10^5 Am^{-2} K^{-2} for ITO contact) [29], ($q\phi_B$) is the barrier height in eV, k is the Boltzmann constant and T is absolute temperature in K.

The diode ideality factors and the reverse saturation currents of the devices with different ZnO annealing temperatures were obtained from *lnI-V* plots as shown in Fig. 3(c). The slope and intercept of the graphs in the linear region (0.1–0.8 V) yield the values of *n* and I_0, respectively. From Table 1, it is observed that the reverse saturation current increases by about three orders of magnitude, whereas the Schottky barrier height ($q\phi_B$) reduces from 550 meV to 330 meV as the annealing temperature of the ZnO increases from 150 °C to 350 °C. However, high value of ideality factors (>1) are observed for all the devices with different annealing temperatures, implying that the current conduction mechanism does not follows the

thermionic emission conduction mechanism alone and it is expected to result from multiple transport mechanisms. This suggests that the interface is not an ideal metal/semiconductor contact and that there must be some trapping states present at the interface which can act as localized carrier generation-recombination centres [30].

In general, the potential barrier height ($q\phi_B$) is related to the work function of the metal ($q\phi_M$) and the electron affinity of the semiconductor ($q\chi$) ($q\phi_B \approx (q\phi_M - q\chi)$) (Fig. 3(a)) [31]. In this study, the potential barrier height for the electron only devices reduces with increasing annealing temperatures (see Supplementary S1(b)). This may be ascribed to the dissimilarity in electron affinity of semiconductor nano particles depending upon their band structure and band gap energy [32]. Similar behaviour is also observed in earlier reports based on Kelvin probe and XPS measurements for sol-gel ZnO thin films [33–35]. We have also employed the impedance spectroscopy (IS) technique to investigate the behaviour of our devices and estimate the electron mobilities.

IS a non-destructive characterization tool to study the frequency dependent behaviour of the charge transport through the devices. It also yields information about the factors influencing charge transport such as the quality of the deposited electrodes, nature of electrode/semiconductor interface, defect density at the metal/semiconductor interface, defect density in the bulk of the semicondutor, charge injection and mobility. In order to investigate the influence of these factors, we have plotted the imaginary part of the impedance against the real part (known as cole-cole plot). Such plots are shown in Fig. 4(a) for the device with ZnO annealed at 350 °C, at different bias voltages. For a given bias, the results show only one semicircle in the measured frequency range (20 Hz to 1 kHz) indicating the predominance of single carrier life-time. The cole-cole plots shown in Fig. 4(a), can be modelled by the equivalent circuit shown in Fig. 4(b)and the impedance of the equivalent circuit may be written as

$$z(f) = Re[z(f)] - jIm[z(f)] = R_s + \frac{R_p}{1 + j\omega\tau} \tag{3}$$

where $\omega = 2\pi f$ is the angular frequency of ac signal, τ is the charge carrier relaxation time, R_s is the series resistance of the device which is a measure of the resistance of metal/semiconductor interface and R_P is the bulk resistance of a semiconductor. The estimated parameters from the equivalent model of the devices are plotted as a function of bias voltage in Fig. 4(c). The parallel resistance–voltage plots (Fig. 4(c)), show exponential behaviour, whereas, the value of constant phase element (CPE) ~1.8×10^{-8} F for 150 °C, 1.2×10^{-8} F for 250 °C and 1.6×10^{-8} F for 350 °C and is seen to be constant with applied bias. Further, the corresponding slopes obtained from the log (resistance)-voltage plots for different annealing temperatures (Fig. 4(d)) are 3.98 for 150 °C, 3.35 for 250 °C and 1.51 for 350 °C, respectively. This indicates that SCLC is the dominant mechanism in our devices having exponential trap distribution [36]. The decrease in slope values with increase in annealing temperatures

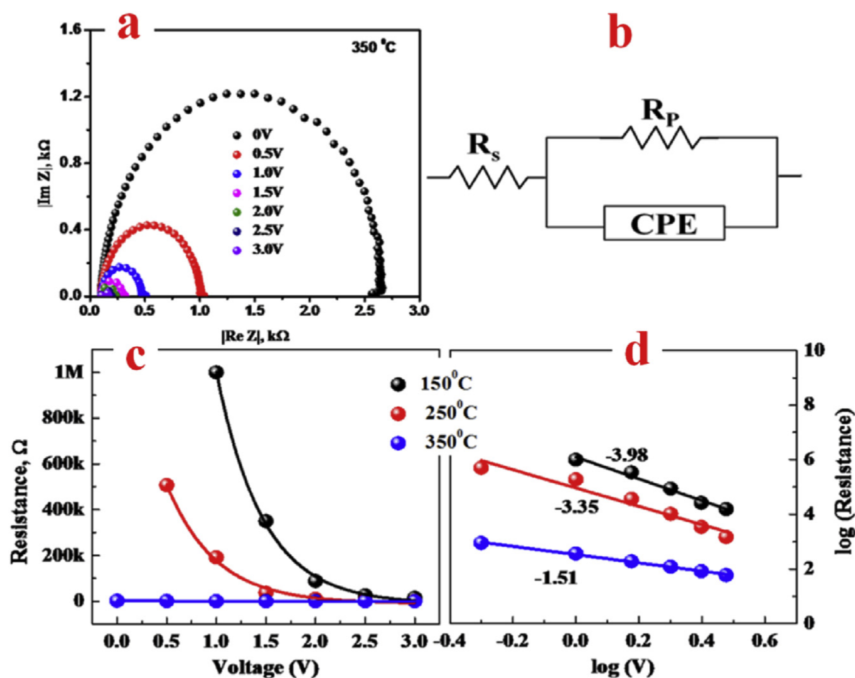

Fig. 4. (a) Frequency dependent Cole-Cole plots for ZnO annealed at 350 °C as a function of bias voltage, (b) equivalent circuit to fit impedance plots (c) resistance-voltage measurements for devices at different annealing temperatures and (d) parallel resistance voltage plots in logarithmic values to verify SCLC mechanism.

indicates reduction of trap density in the bulk of ZnO film. On the contrary, the device with ZnO annealed at 450 °C exhibits ohmic conduction.

For SCLC conduction mechanism with exponential trap distribution, the density of states (DOS) at the Fermi level is estimated using the following equation [37].

$$N(E_F) = \frac{2\varepsilon_r\varepsilon_0\Delta V}{qd^2\Delta E_F} \tag{4}$$

where ε_r is the dielectric constant of the ZnO (8.5) [38], ε_0 is the absolute permittivity, q is the electron charge, d is the thickness of the ZnO layer, ΔE_F is the shift in the quasi-Fermi level and $\Delta V = V_1 \sim V_2$, V_1 and V_2 two different voltages applied to the device. When the applied potential is increased from V_1 to V_2 (extremes of SCLC region), the quasi-Fermi level shift is given by the equation,

$$\Delta E_F = kTln\left(\frac{I_2V_1}{I_1V_2}\right) \tag{5}$$

where k is the Boltzmann constant, T is the absolute temperature and I_1, I_2 are current values measured at the voltages V_1 and V_2. From Table 1, it is noted that there is no significant change in the estimated values of effective DOS around the Fermi level which indicates that the trap density at the interface is same for all the samples. From the Capacitance–Voltage characteristics (Supplementary S2), it is found that the charge carrier density in the devices increases from 2.0×10^{19} cm^{-3} to 5.3×10^{19} cm^{-3} (about 2.5 fold) as the annealing temperature increases. This may be due to the changes in barrier height, facilitating high density of injected charge carriers into the device. The corresponding built in voltage values are tabulated in Table 1. ZnO annealed at 450 °C showed ohmic nature due to the intermixing of ITO and ZnO layers due to diffusion at the interface [39,40]. The observed values of the DOS at Fermi level for all the devices (10^{17} eV^{-1}cm^{-3}) are comparable with values reported earlier [30].

Fig. 5(a) depicts the Re [Z]-f characteristics as a function of applied dc bias for the device fabricated with ZnO annealed at 350 °C. At lower frequencies, it is seen that the magnitude of Re [Z] decreases progressively from 1000 kΩ to 15.3 kΩ with an increase in dc bias over a range of 1–3 V indicating that the device turns from high resistance state to the semiconducting

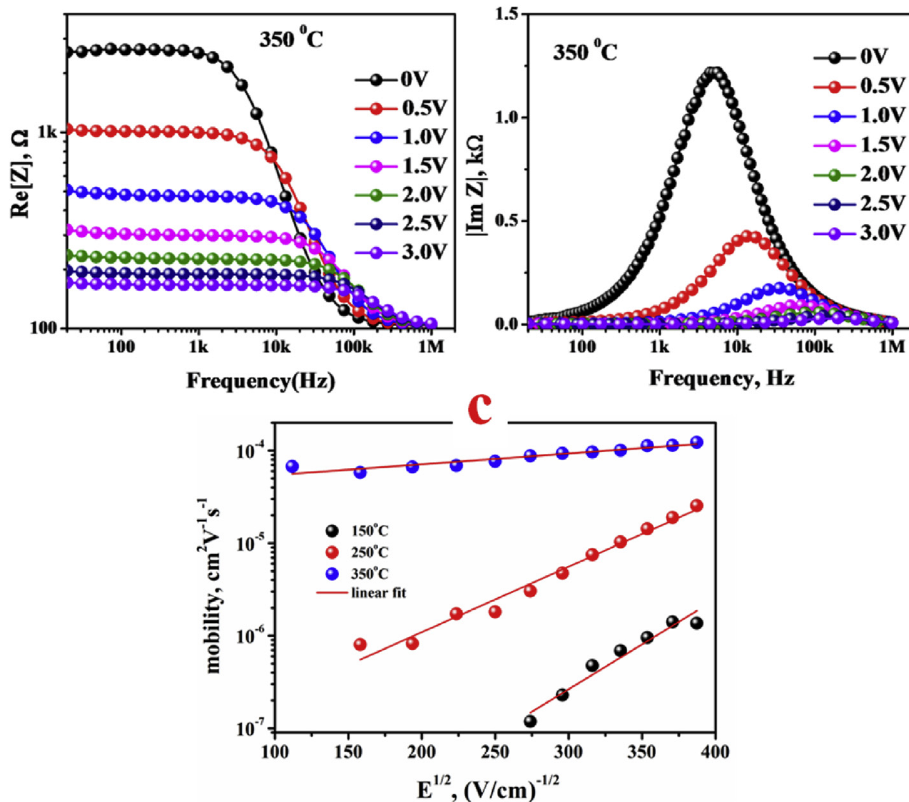

Fig. 5. (a) Re [Z]- *f* characteristics of the ZnO annealed at 350 °C, (b) Im [Z]- *f* characteristics of the ZnO annealed at 350 °C and (c) Poole-Frenkel mobilities for samples annealed at different temperatures.

state. This is due to the increase of charge carrier injection and better transport promoted by the applied bias resulting in the reduction of the bulk resistance of the device. However, at frequencies greater than 100 kHz, the Re [Z]-f plot for all dc biases converge. It can also be noticed from the plot that, the point at which Re [Z] gradually changes from being frequency independent to becoming frequency dependent shifts towards higher frequencies with increase in bias voltage. This may be attributed to increase in conductivity due to the release of space charge resulting from reduction in barrier height as the applied bias increases. It is also seen that the magnitude of the Re [Z] reduces with increase in annealing temperature of ZnO. This may be due to the reduction in ITO/ZnO potential barrier height with increasing annealing temperature; the barrier height is reduced from 550 meV to 333 meV (Table 1).

Fig. 5(b) shows the Im [Z]–f plots for different dc bias voltages. Generally, the frequency corresponding to the peak in Im [Z]-f plot is used to estimate the relaxation time (τ_r) and, thereby, the mobility of the charge carriers in the ZnO layer. The peak shifts to higher frequencies with increase in dc bias voltage with its magnitude progressively reducing. The charge carrier mobility (μ) of the annealed ZnO films are estimated using the relation [41,42].

$$\mu = \frac{d^2}{\tau_{dc} V_{dc}} \tag{6}$$

Here d is the thickness of the active layer, V_{dc} is the applied dc bias and $\tau_{dc} = K\tau_r$, K is numerical correction factor on account of dispersion transport [42]. τ_{dc} and τ_r are the average charge carrier transit time and charge carrier relaxation time, respectively. From the computer simulations, it is found that the value of $K = 0.46$ for the nondispersive transport and changes by ± 0.052 in case of dispersive transport. The simulated frequency dependent impedance plots are presented in Fig. S3 (Supplementary).

The Poole-Frenkel field-dependent mobility is given by the relation [43].

$$\mu(E) = \mu_0 \exp\left(\beta\sqrt{E}\right) \tag{7}$$

where $E = V/d$ is the applied electric field at a given voltage V. The field-independent mobility (μ_0) and the Poole–Frenkel (PF) coefficients (β) are obtained from the intercept and slope of the linear fit to the above equation (Fig. 5(c)). The charge carrier mobility values, thus obtained, are comparable with those obtained from sol-gel ZnO thin films reported by others [44]. From Table 1, it is evident that the electron mobility of the ZnO increases by up to 5 orders as the ZnO annealing temperature increases from 150 °C to 350 °C. This enhanced mobility at higher temperatures is attributed to the following reasons: (i) reduction of barrier height, which facilitates high electron injection from ITO to ZnO, and (ii) increase in the crystallinity of ZnO with annealing temperature which results in larger grain size and hence reduction in grain boundaries (which act as defects/traps). Higher charge injection due to the reduction of barrier height, lower defect density and improved crystallinity (increased grain size) makes the ZnO film annealed at 350 °C more suitable for optoelectronics applications.

3. VOPc/ZnO p-n junction diode

Fig. 6(a) shows the energy level diagram of the p-n junction diode with the configuration ITO/ZnO (annealed)/VOPc/MoO_3/Al. The energy levels of VOPc and MoO_3 have been taken from the literature [24,45]. In our earlier work, it was shown that VOPc thin films produced at low deposition rates (~0.1 A/s) exhibit high hole mobilities [24]. Therefore, we investigated the characteristics of the p-n junction formed by VOPc with ZnO. The room temperature J-V characteristics in dark, dark and illuminated conditions for the p-n junction with ZnO annealed at different temperatures are shown in Fig. 6(b) and (c), respectively. When a negative voltage is applied to ITO, the p-n junction gets forward biased, with ZnO being more negative than VOPc. Therefore, the current flows easily through the junction. When ITO is given positive bias, ZnO becomes more positive with respect to VOPc making the junction reverse biased, thereby limiting the current flow. Thus, all the diodes clearly exhibit rectification behaviour when not exposed to light. On fitting the experimental data of J-V curves at different ZnO anneal temperatures, it was observed that the ideality factors were rather high, ranging from 19 to 24 compared to that of an ideal diode ($n = 1$). This could be due to the following reasons (i) presence of imperfections/traps at ZnO/VOPc interface which may lead to different tunnelling assisted transport, and (ii) enhanced electron–hole recombination in the depletion region (ZnO/VOPc), thereby increasing the series resistance of the device.

Further, from Fig. 6(b), it can be seen that, the current through the device is higher if the ZnO film is annealed. As mentioned earlier, higher annealing temperatures increase the ZnO grain size (from 11 nm to 21 nm), which in turn leads to reduction in grain boundaries and also to lowering of the Schottky barrier height from 572 meV to 471 meV. This might be the reason for the high current through the devices having annealed ZnO films. When the p-n diode is subjected to illumination, the ideal diode equation is given by Ref. [45].

$$I_{total} = I_{dark} + I_{photo} = I_{sat}\left[exp\left(\frac{V}{nV_t}\right)\right] - I_{photo} \tag{8}$$

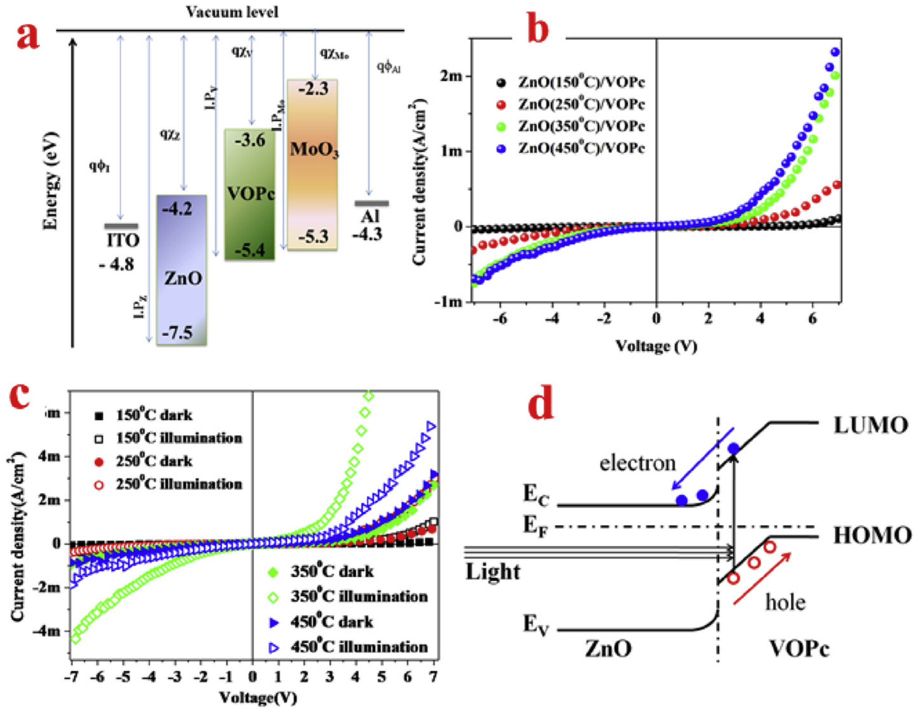

Fig. 6. (a) Energy level representation of the VOPc/ZnO diode in the configuration: ITO/ZnO/VOPc/MoO_3/Al; J-V characteristics of a VOPc/ZnO p-n junction in dark conditions; (c) J-V characteristics of a VOPc/ZnO p-n junction in dark and illumination conditions and (d) illustration of photocurrent generation mechanism in VOPc/ZnO p-n diode.

where I_{photo} is the photocurrent generated due to the illumination of the device. The mechanism which governs the charge transfer across the VOPc/ZnO interface is illustrated in Fig. 6(d). When the device is illuminated from ITO side, a large number of excitons are formed in VOPc layer due to absorption of photons. The optical transparency of all the ZnO films were greater than 85%, (see Fig. S1(a) in Supplimentary). The photogenerated excitons diffuse into the VOPc/ZnO interface. At the interface, the dissociation of excitons takes place rapidly due to the large LUMO offset between the ZnO and VOPc. Though the CB of ZnO is much lower (~0.9eV) than the LUMO of VOPc, the electrons are easily transferred to the ZnO layer and are collected by the ITO electrode. Simultaneously, the holes move easily through the VOPc layer, as it acts as an efficient hole transporter, and gets collected by the Al metal electrode.

The photocurrent responsivity (R_{ph}) is given by Ref. [46].

$$R_{ph} = \frac{I_{photo}}{P_{optical}} \tag{9}$$

where, $P_{optical}$ is the incident optical power. The estimated value of $'R_{ph}'$ at different annealed temperatures are presented in Table 2.

Table 2
Estimated p-n junction parameters from J-V characteristics.

ZnO annealing temperature	Measurement condition	Barrier height (meV)	RR@6 V	Photo responsibility (mA/W)	
				@ -6 V	@6 V
150 °C	Dark	562	0.5	6.2	13.0
	illumination		1.8		
250 °C	Dark	543	1.6	12.9	33.3
	illumination		7.7		
350 °C	Dark	490	2.4	131	470
	illumination		6.0		
450 °C	Dark	471	2.9	12.5	47.5
	illumination		3.3		

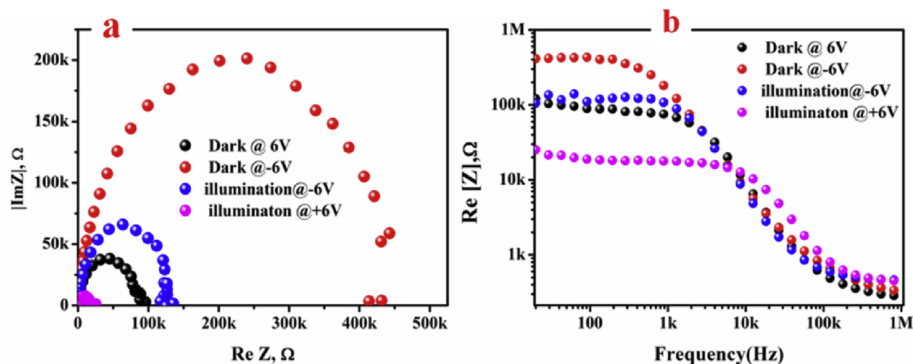

Fig. 7. (a) Cole-Cole plots for VOPc/ZnO interface (annealed at 350 °C) p-n junction in dark and illumination conditions for a given bias and (b) re [z] − *f* plots of a VOPc/ZnO (annealed at 350 °C) p-n junction.

It is observed from Fig. 6(b) that the dark current is more for the p-n diode with ZnO annealed at 450 °C. However, from Fig. 6(c), it can be observed that the photocurrent and, hence, the photocurrent responsibility (both at positive and negative bias voltages) is high for the device with ZnO annealed at 350 °C. It may be due to the lower electron-hole recombination at the interface and better charge collection in case of p-n junction with ZnO annealed at 350 °C. To further investigate the photoresponse of the device, IS measurements were also carried out for the p-n diode with ZnO annealed at 350 °C. Fig. 7(a) shows the Cole-Cole plots generated for the same device under dark and as well as illuminated conditions. Fig. 7(b) displays real part of the impedance versus frequency at a given bias. From 7(a) and (b), it can be noted that the difference between the Cole-Cole plots for a given condition (dark or illuminated) at a particular bias represents the rectification ratio. Also, the difference between the Cole-Cole plots for dark and illuminated conditions at a given bias (say at −6 V) is an indicative of the photo-response of the p-n junction.

The Cole-Cole plots for VOPc/ZnO interface at a given bias show a single semicircle for a given condition (dark or illuminated), which indicates the predominance of a single carrier life time. It can be seen that, at higher frequencies, the Cole-Cole plots are not perfect semicircles. To understand the nature of the Cole-Cole plots, we employed the equivalent circuit model for our devices, similar to the one shown in Fig. 4(b). In general, at a given bias, two semicircles are expected for a junction where two materials are involved. Since the bulk resistance (R_p) of ZnO in the electron only device configuration (Fig. 4(a)) is almost equal to the estimated series resistance (R_s) for the VOPc/ZnO interface (Fig. 7(a)), the semicircle corresponding to ZnO is not observed in the obtained Cole-Cole plots for VOPc/ZnO junction. It is also observed from Fig. 7(b) that the bulk resistance of the VOPc/ZnO p-n diode under illumination is, approximately, 5 times lower in forward bias and 2 times lower in reverse bias than that under dark condition at a bias of 6 V. The rectification ratios are found to be 3.42 and 8.1 in dark and illuminated conditions at 6 V, respectively. These rectification ratios agree well with the values obtained from the J-V characteristics.

4. Conclusions

In this paper, we have investigated four electron-only devices having the configuration: ITO/ZnO/Al by varying the annealing temperature of the active layer (ZnO). The improvement in the current density as well as the mobility of the devices, with the ZnO film annealed at 350 °C, is attributed to the increase in grain size, reduction of the Schottky barrier height and high carrier density. We infer that the electrical conduction in these devices is dominated by SCLC mechanism with exponential density of traps. The DOS at Fermi level is found to be ~10^{17} eV^{-1} cm^{-3} and is almost same for all the devices. The electron mobility values are obtained from the impedance measurements. A larger electron mobility of 1.91×10^{-5} cm^2 V^{-1} s^{-1} was achieved in the device with ZnO film annealed at 350 °C. In addition, we have also studied the organic-inorganic hybrid p-n diodes having the configuration: ITO/ZnO/VOPc/MoO_3/Al by varying the annealing temperature of ZnO (n-type layer). The interface parameters such as ideality factor (n), Schottky barrier height ($q\phi_B$) and rectification ratio (RR) of the devices were determined from J-V characteristics. It is realized that the devices with the ZnO film annealed at 350 °C show high photocurrent responsivity (470 mA/W). This suggests better exciton dissociation at the interface and thereby efficient charge collection at both the electrodes. Hence, ZnO films annealed at 350 °C are suitable for organic-inorganic hybrid optoelectronic device applications.

Acknowledgement

The Authors thank Department of Physics, National Institute of Technology Karnataka, Surathkal for various facilities. M.R.K acknowledges Mr. Raghavendra M.A.N.S (Department of Electronics and Communication Engineering, NITK) and M. VIjay (Department of Electrical and Electronics Engineering, NITK) for their help in computer simulations. Authors also thank

Ministry of Communications and Information Technology, Government of India, for financial support through a sponsored research project grant number 12(3)/2010-PDD.

Appendix A. Supplementary data

Supplementary data related to this article can be found at https://doi.org/10.1016/j.spmi.2017.10.023.

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