LOW POWER BALUN LNAs FOR NARROW-BAND AND UWB APPLICATIONS

Thesis

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DOCTOR OF PHILOSOPHY

by

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SEPTEMBER, 2019

DECLARATION

I hereby *declare* that the Research Thesis entitled **LOW POWER BALUN LNAs FOR NARROW-BAND AND UWB APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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Dedicated to

Amma, Nanna, Bujji and Kids...

Abstract

This research work concentrates on the Design and Implementation of single to differential (balun) Low Noise Amplifiers (LNAs) for narrow-band and ultra wide band (UWB) applications. The transceiver of wireless devices dominate the overall power consumption. Hence, low power designs are to be investigated for enhancement of the battery life. Improving the power efficiency of the front-end will dramatically increases the receiver performance. Furthermore many wireless receivers have indispensable passive/active balun for differential conversion of incoming single-ended antenna signal. The cynosure of proposed LNAs are low power, single to differential conversion and diminution of gain and phase error (i.e. less than 1 dB and 10° respectively) at the differential output.

A high selectivity, current-reuse balun LNA is proposed for low power wearable and implantable medical devices which are operated in the range of 401 to 406 MHz. An inductive degenerated common source (IDCS) topology has been used for optimum power, noise and impedance matching. The differential conversion of RF input has been achieved by stacking cascaded stage (stage-II) on top of the IDCS stage (stage-I). In addition, a second design of balun LNA is proposed for UWB applications in the frequency range of 3.1 to 10.6 GHz. The specifications of UWB are in contrast with the narrow-band design. The UWB radio technology introduces significant advantages for short-range communications systems. This technology requires a wide bandwidth, which allows Gigabit data rates over short distances. An exemplary common gate and common source topology (CG-CS) has been used for differential conversion of the input signal. A CG-CS stage exploits amalgamation of CG stage (for wide-band impedance matching) and CS to curtail signal imbalance, while simultaneously negating noise and distortion of the input matching transistor. The proposed balun exerts a differential stage on top of CG-CS stage. The improvement of bandwidth has been accomplished using staggered tuning on CG-CS and differential stages.

An Inductor-less balun LNA is also designed for multi-band applications in the range of 0.2 to 2 GHz. The proposed LNA incorporates noise can-

cellation and voltage shunt feedback techniques to achieve minimum noise characteristics and low power consumption respectively. In addition, transconductance scaling has been used to improve the noise performance. In this way, noise figure (NF) of LNA below 3 dB is achieved. An additional capacitor is used to correct the gain and phase imbalance at the output. The gain switching has been enabled with a step size of 4 dB for high linearity and power efficiency.

This research also concentrates on biasing circuits for LNAs to reduce the performance variations against process, supply voltage and temperature (PVT). A conventional biasing circuit leads to variations in the performance parameters of LNA. This is even worse when core transistor of LNA operates in the sub-threshold region. Compensation bias circuits have been designed to minimize the performance variations in LNA parameters. The proposed balun LNAs are implemented in UMC 0.18-μm CMOS technology. Finally, all the proposed designs are validated by rigorous Monte Carlo simulations.

Keywords: Low Noise Amplifier; Current re-use technique; Noise cancellation; Staggered tuning; Gain switching; MedRadio; UWB.

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Nomenclature

SYMBOL	MEANING
γ	Excess drain noise coefficient
δ	Excess gate noise coefficient
Q	Quality factor
K	Constant
T	Temperature
f	Frequency in Hz
ω	Angular frequency in radians per second
g_m	Transconductance
c	Noise correlation coefficient between gate and drain
f_t	Transition frequency
I/Q	In/Quadrature phase
k	Kilo
μ	Micro
$\overline{i_n^2}$	Noise current spectral density
C_{ox}	Gate-oxide capacitance
g_{d0}	Drain conductance for zero drain-source voltage
g_g	Frequency dependent gate conductance
α	Constant
θ	Phase in degrees
ϕ	Phase in radians
μ_n	Mobility of electrons

Abbreviations

ABBREVIATION	EXPANSION
BER	Bit Error Rate
BSF	Band Selection Filter
BW	Band Width
CCCS	Capacitively Cross-coupled Current Source
CCR	Complimentary Current Re-use
CG	Common Gate
CMOS	Complimentary Metal Oxide Semiconductor
CS	Common Source
CTAT	Complementary to Absolute Temperature
DC	Direct current
DCR	Direct Conversion Receiver
DQPSK	Differential Quadrature Phase Shift Keying
DTV	Digital television
EIRP	Effective Isotropic Radiated Power
FCC	Federal Communications Commission
FoM	Figure of Merit
FSPL	Free Space Path Loss
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
IDCS	Inductive Degenerated Common Source
IF	Intermediate Frequency
IIP	Input Intercept point
IM	Inter Modulation
IRF	Image Rejection Filter
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MedRadio	Medical Radio
Nf	Noise factor
NF	Noise Figure
OIP	Output Intercept Point
OTA	Operational Trans-conductance Amplifier
PCSNIM	Power Constrained Simultaneous Noise Impedance Matching
PPS	Power Phase Splitter
PVT	Process Voltage and Temperature
QFN	Quad Flat No-lead
RF	Radio Frequency
SAW	Surface Acoustic Wave
SD	Single to Differential
SNR	Signal-to-Noise Ratio
UHF	Ultra High Frequency
UMC	United Microelectronics Corporation
UWB	Ultra Wide Band
WLAN	Wireless Local Area Network

Chapter 1

INTRODUCTION

Communication system describes a communication exchange between two stations, transmitter and receiver. Prior to the data transmission over a wireless medium, transmitter shifts the baseband spectrum to the channel frequency assigned for transmission by modulating carrier signal. The receiver performs frequency down-conversion and demodulation to retrieve the original data. In the communication process, the role of receiver is listener, reader and it is as important as that of sender. The communication process would be complete and successful if the receiver provides satisfactory feedback on the received signal. The choice of receiver architecture is determined by parameters such as power dissipation, sensitivity, selectivity, noise figure, cost and number of external components.

In modern day technology, most of the wireless and mobile applications are using different radio receiver architectures to meet the demands. Some RF receivers have higher levels of performance and are not confined by area as much and where as some are simpler than others. Often, strong interference generated by users that do not belong to the standard of interest are presented close to the spectrum of desired signal. The interference from these can corrupt demodulation in receiver. Band-selection and channel selection filters are required to limit the effects of interferes. However, the front-end band selection filters suffer from a trade-off between selectivity and band loss. Further high selectivity filters are needed at higher frequencies (Razavi Behzad (1998)). Hence, to permit the channel selection filtering with reasonable quality factor (Q), the RF receiver must be devised with translating the desired channel to a much lower frequency. Different translation techniques have been around for many years.

1.1 Receiver architectures

In all types of radio receivers the first active block is low noise amplifier. Hence, the design of LNA dictates the overall performance of receivers. A brief study of receiver architectures must be needed to understand the importance of balun, low noise amplifier and the mixer. In general, these receiver architectures are classified as heterodyne and homodyne types.

1.1.1 Heterodyne receiver

In heterodyne architectures, the translation of incoming RF signal is performed by means of a mixer. The architecture of simple heterodyne receiver is shown in Figure 1.1.

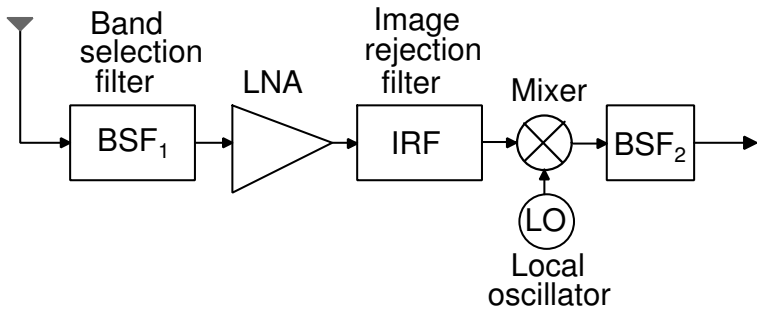


Figure 1.1: Architecture of a typical single-IF heterodyne receiver.

The band selection filter (BSF_1) of front-end selects the desired band and rejects the image as well. After the amplification from low noise amplifier (LNA), it passes through the filter for image rejection. Although the BSF suppresses image signal to some extent, it will be amplified by the LNA before mixing. So an image-reject filter is placed immediately before the mixer. The mixer then translates the desired band and interferes to the baseband. Further, band selection filter (BSF_2) suppresses the interferes to the lower level. In the design of heterodyne receiver, intermediate frequency (IF) is a critical parameter, because its selection involves a fundamental trade-off between image rejection, sensitivity and selectivity. A higher IF frequency eases the rejection of image since the image appears further away from desired band. Similarly, a lower IF leads to a larger adjacent channel rejection since the quality factor of a filter determined by the ratio of center frequency to bandwidth.

The choice of IF depends on trade-off among the spacing between desired band and image, the amount of image noise and the loss of image incurred by rejection filter. The image can be minimized either by increasing the IF or using high-Q filter. If the IF frequency is too high, then Q of image rejection filter (IRF) can be relaxed. This leads to much tighter requirements from band selection filter. In other case, the lower IF frequency demands for high-Q image filter to suppress image effectively. Further, the noise and interfere leakage will reduce the sensitivity of the receiver. The impact of IF selection on the receiver performance is shown in Figure 1.2.

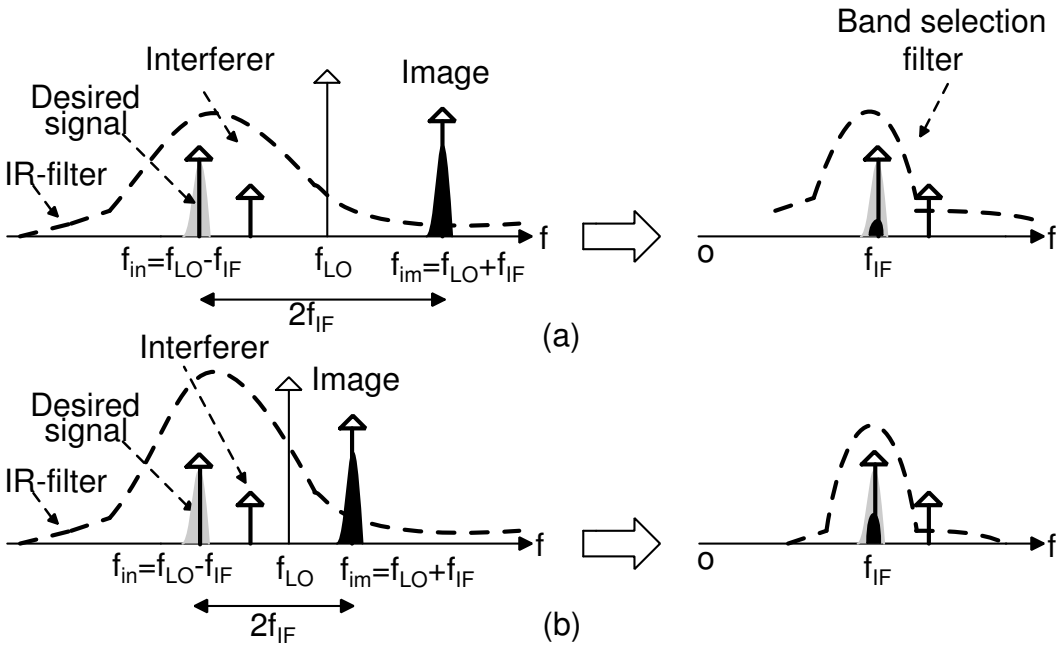


Figure 1.2: Trade-off between image rejection and channel selection (a) High IF (b) Low IF.

However, the single IF receiver architecture shown in Figure 1.1 has the following issues: (i) high-Q requirement of band selection filter (ii) trade off between image rejection and channel selection. These issues can be relaxed by using multiple down-conversion architecture as shown in Figure 1.3.

The first mixer (RF mixer) translates the desired band and interferes to the first intermediate frequency (IF). The second mixer (IF mixer) and BSF_3 suppresses the interferes to the lower level. In heterodyne receiver the choice of IF enhances the selectivity of the receiver. Further, the stability is more since the double translation process provides better isolation between the blocks. Though it has several advantages, the

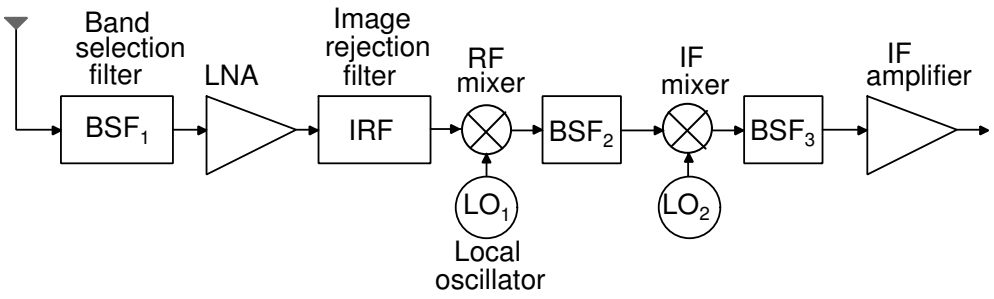


Figure 1.3: Architecture of super heterodyne receiver.

integration complexity, high power dissipation, and external components requirement are the bottlenecks. Moreover, it is not adaptable to use in different wireless standards and modes. Finally, the image filter between LNA and mixer is indispensable because image bands are also down converted by IF mixer and places in the desired band as shown in Figure 1.4. In order to reduce power consumption and addition of external components, a direct conversion (zero-IF) and low-IF architectures have increasingly gained popularity in recent designs of wireless communications systems.

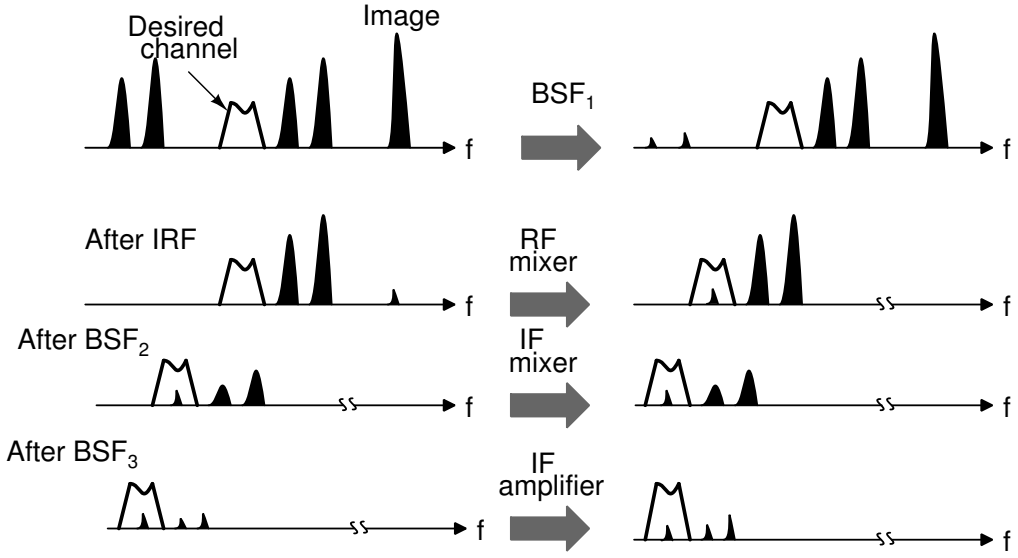


Figure 1.4: Importance of band selection and image rejection filters in multiple down conversion receiver.

1.1.2 Homodyne receiver

A homodyne receiver is also known as direct conversion or zero IF receiver. The architecture of homodyne and low-IF receiver is similar except that homodyne receiver down-converts RF signal frequencies directly to baseband frequencies. Therefore the direct conversion receiver emerges as an alternate to heterodyne architecture. The receiver architecture is shown in Figure 1.5.

The following aspects of zero-IF receiver makes it superior with respect to super heterodyne receiver: (i) absence of high-Q off-chip band selection filters since band selection is done by low pass filter (LPF) and it can be implemented with on-chip components (ii) as the frequency of IF is zero, the problem of image is avoided (i.e., no image rejection filter) (iii) simple to handle because of less number of mixing spurs.

However, in spite of its advantages and simplicity, the homodyne receiver does have some other performance issues that impede its widespread adoption (Lee (2004)). The main disadvantage is LO leakage as shown in Figure 1.6.

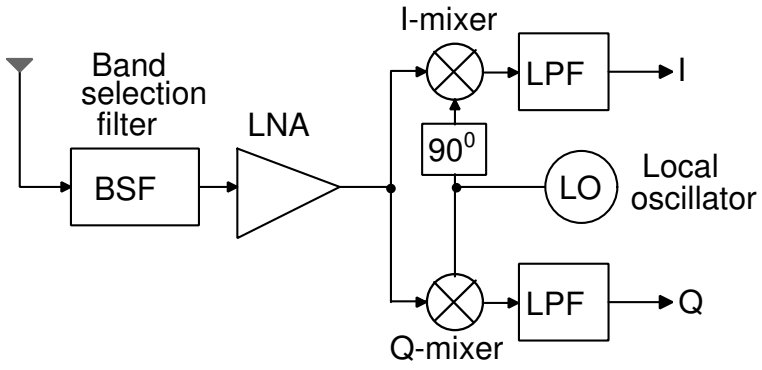


Figure 1.5: Architecture of direct conversion receiver.

A direct conversion receiver emits a fraction of LO power through the device and pad capacitance. The LO emission is undesirable and it reduces the sensitivity of other receivers operating in the same band. Even in heterodyne architecture, LO leakage will occur but it can be suppressed by front-end band selection filter. The LO leakage gives raise to large DC offset in the band of interest and makes the processing of baseband signal difficult. Furthermore, third-order distortion of active devices in the chain results in compression and intermodulation. As a result, a fraction of lower beat interferer component appears in the baseband. The effect of even-order

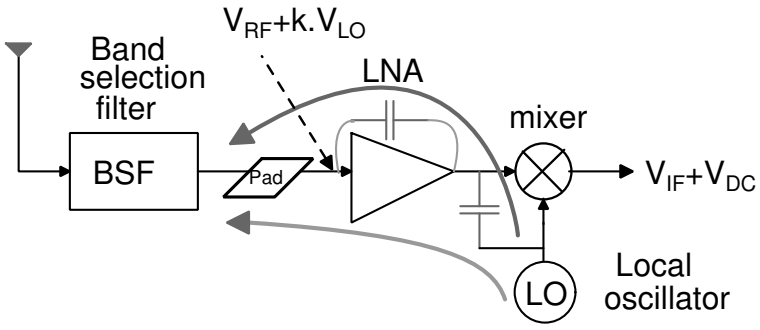


Figure 1.6: LO leakage and DC offset in direct conversion receiver.

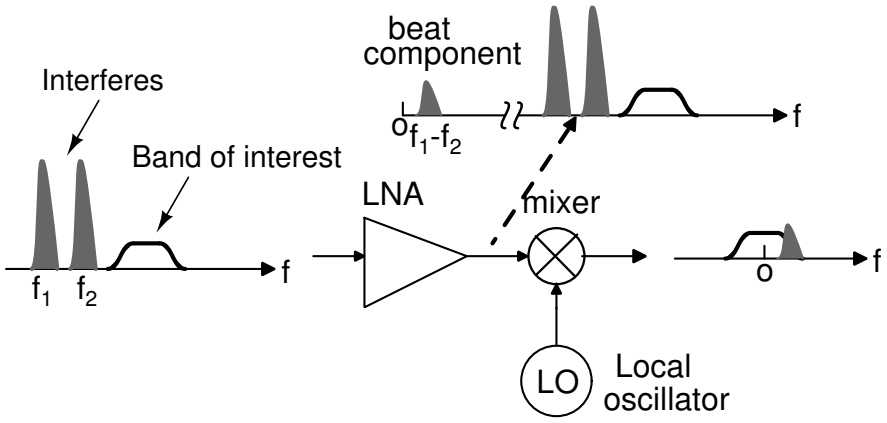


Figure 1.7: Effect of even order distortion on homodyne receiver.

distortion on the down conversion of baseband signal is shown in Figure 1.7 with two strong interferes at f_1 and f_2. Another serious problem of homodyne receiver is the I/Q mismatch. Due to the quadrature mixing requirement, either the RF signal or the LO output has to be shifted by 90°. Since shifting the RF signal generally causes severe noise-power-gain trade-offs and poor SNR performance (because of gain and phase error between I/Q signals).

1.2 Issues in narrow-band wireless RF front-end

Several architectures have been considered to realize low power receivers for narrow-band applications. It is shown that, the direct conversion architecture is inappropriate for the implementation of a system with channel bandwidths less than 100-150 kHz

(Cha *et al.* (2011)). The baseband can be severely corrupted by the presence of flicker noise and dc offset. If the channel bandwidth is more than 300 kHz, a direct conversion receiver can be used at the cost of high power consumption and complicate design (Ba *et al.* (2015)). A low-IF architecture would be better for narrow-band systems to reduce the design complexity. Therefore, the RF signal is down converted to a low IF of 500-600 kHz. Block diagram of a traditional narrow-band RF front-end is shown in Figure 1.8. It comprises of band selection filter, LNA, mixer, indispensable image filter and balun.

Most of the narrow-band front-ends suffer from the following common issues irrespective of receiver architecture: (i) at some point over the front-end chain, an incoming single-ended antenna signal needs to be converted into differential signal (ii) requirement of high-Q external channel selection filter (iii) gain and phase error at the output of balun (Martins *et al.* (2011)). Finally, the performance parameters are sensitive to process, voltage and temperature (PVT) variations.

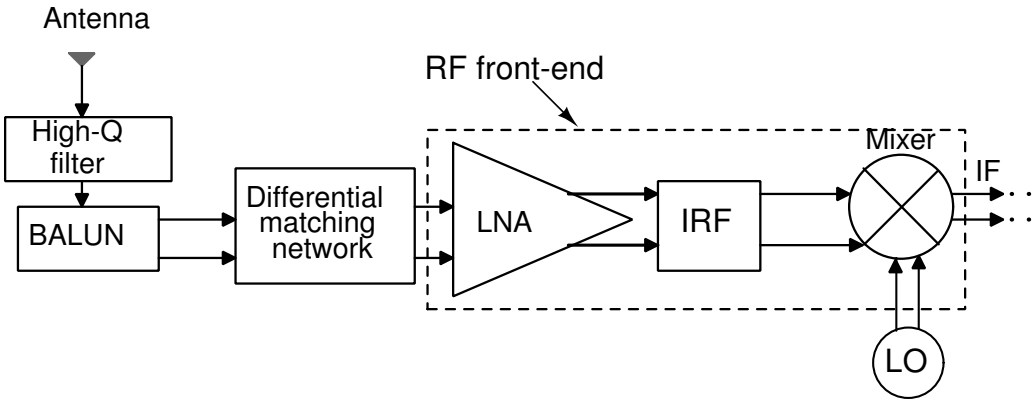


Figure 1.8: Block diagram of the traditional narrow-band front-end.

In all receiver front-ends, the first amplifying block is a low noise amplifier and it decides most of the front-end performance parameters such as sensitivity, gain, noise figure, linearity and power consumption. Many narrow-band techniques have been implemented for LNA. As we have targeted Medical Radio communication band as an example of narrow-band, the figure of merit (FoM) comparison of recently reported LNAs is shown in Figure 1.9. The FoM reported in Amer *et al.* (2007), is considered for comparison to select most relevant parameters of LNA. The mathematical expression

for FoM is given by (1.1).

$$FoM = \frac{Gain[abs] \times IIP_3[mW] \times f[GHz]}{P_{DC}[mW] \times (NF-1)[abs]} \tag{1.1}$$

where, f is the center frequency in GHz. Considerable research has been done on narrow-band LNAs, but it is heavily biased towards either single-ended or differential with inevitable balun. Though most of the techniques have sufficient FoM, still there are some restraints exists among them. Nevertheless the FoM of Cha *et al.* (2011) is better, the additional requirement of balun and headroom are the bottlenecks. So, a single to differential LNA would be the better option to overcome most of the issues occurring in traditional narrow-band receiver. The main design challenges in balun LNA are: (i) requirement of optimum power, noise and impedance matching (ii) need for single to differential conversion of incoming antenna signal (iii) need for minimum gain and phase error at the output and (iv) bias compensation against PVT variations.

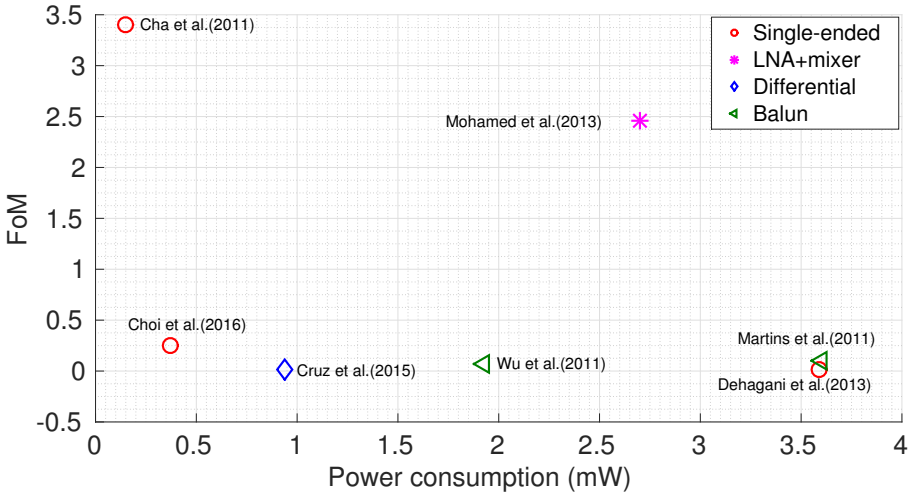


Figure 1.9: FoM comparison of recently reported LNAs for Medical Radio communication.

1.3 Issues in wide-band wireless RF front-end

The wide-band systems have been used for high data rate wireless applications. Direct conversion receiver (DCR) architectures are commonly used in wide-band systems as

shown in Figure 1.10. It comprises of balun, LNA, and mixer with filter. As DCR architecture suffers from LO leakage and DC offset, hence differential conversion of incoming signal must be entailed before the mixer stage. As per the Friis equation, if we place balun before the active block, its noise figure kills the entire receiver performance. So, placing a balun after the LNA would be better option. In either cases, there is requirement of lossy and bulky balun. The common challenges in wide-band front-end are :(i) low noise, gain flatness and low power consumption (ii) bandwidth extension and (iii) additional balun and its imbalance at differential output.

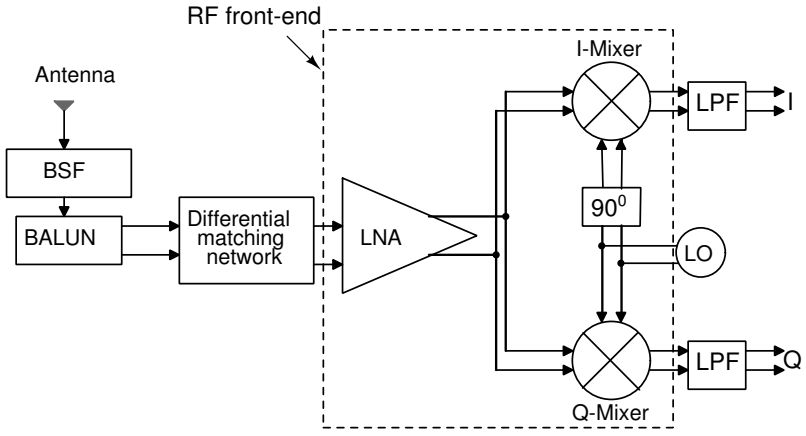


Figure 1.10: Block diagram of the traditional wide-band receiver.

Many techniques have been matured in the literature for wide-band LNAs. As we have focused on the design of LNA for ultra wide-band technology, a FoM comparison of recently published work has been given in Figure 1.11.

The FOM is included with gain, band-width (BW), noise figure and power consumption to meet wide-band low power system specifications (Linten *et al.* (2005)).

$$FoM = \frac{Gain[abs] \times BW[GHz]}{(NF-1)[abs] \times (P_{DC}(mW)/10^{-3})} \tag{1.2}$$

Most of the reported LNAs are cascade of minimum two stages to attain wide-band. Nevertheless recently reported LNAs showing better performance, the power consumption is not less than 8 mW.

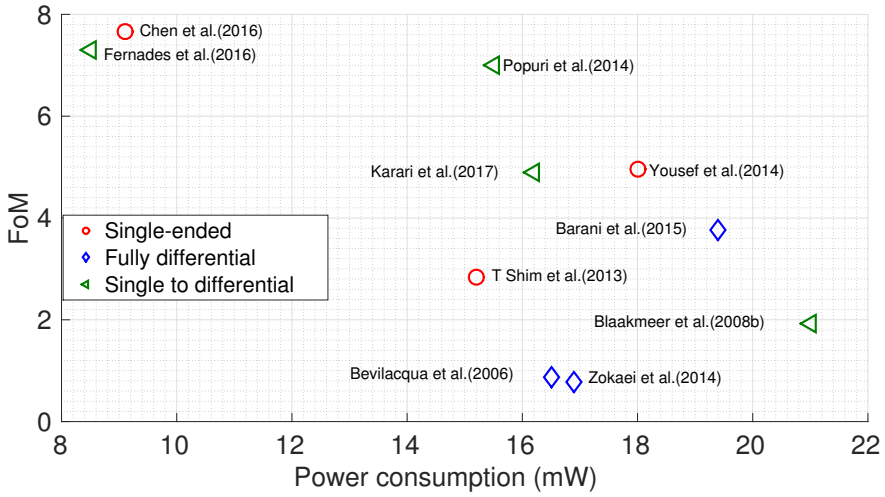


Figure 1.11: FoM comparison of recently reported LNAs for UWB applications.

1.4 Issues in multi-band wireless RF front-end

Nowadays, the design of high-end wireless devices focus on wide-band to cover minimum of 5 to 10 standards over different frequency bands. Many countries are using ultra high frequency (UHF) band for ISM applications (260 to 470 MHz), high quality digital signal for digital TV (DTV) applications (470 to 890 MHz) and GPS & B_2 systems for GNSS receivers (Wu *et al.* (2011), ATScomm (2004)). This trend will become popular in the future and creates many new design challenges with low area, power and single chip RF front-end. One of the main advantage of wide-band system is its re-usability and low cost. The performance of multi-standard receiver architecture depends on the design of low noise amplifier. The traditional block diagram of multi-standard receiver is shown in Figure 1.12. In this receiver chain, redundant LNAs increases the cost and area. Further, an inevitable balun is needed in each parallel path (Martins *et al.* (2011)). The parallel connections with narrow band LNAs have the disadvantage of large die area and lack of reconfigurability. Nevertheless, tunable LNA with active inductor covers the desired band, the poor noise performance beneath its advantage as given in Slimane *et al.* (2012).

In multi-standard systems, few common difficulties are: (i) the presence of intermodulation degrades the sensitivity and signal to noise ratio (SNR) (Meghdadi *et al.* (2017)) (ii) The strong input level, which may degrade the linearity of subsequent stages. These difficulties can be avoided using high dynamic range LNA. It is shown

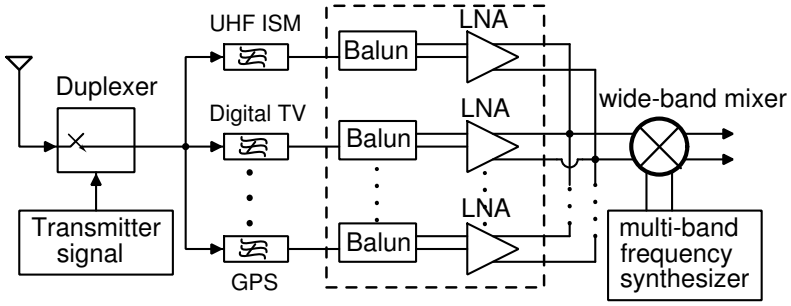


Figure 1.12: Block diagram of traditional front-end for multi-standard receiver.

that the gain switching of LNA is an effective method to improve the dynamic range and linearity (Jeong *et al.* (2008)). The input power level of targeted applications varies from –30 dBm to –80 dBm. So, gain switching becomes necessary to provide sufficient headroom for succeeding blocks in the receiver. Furthermore, most of the proposed designs are sensitive to PVT variations. This demands for additional bias compensation circuit which effects overall LNA performance. An inductor-less balun LNA is the suitable choice to subjugate above mentioned issues and meet the requirements of low area and power.

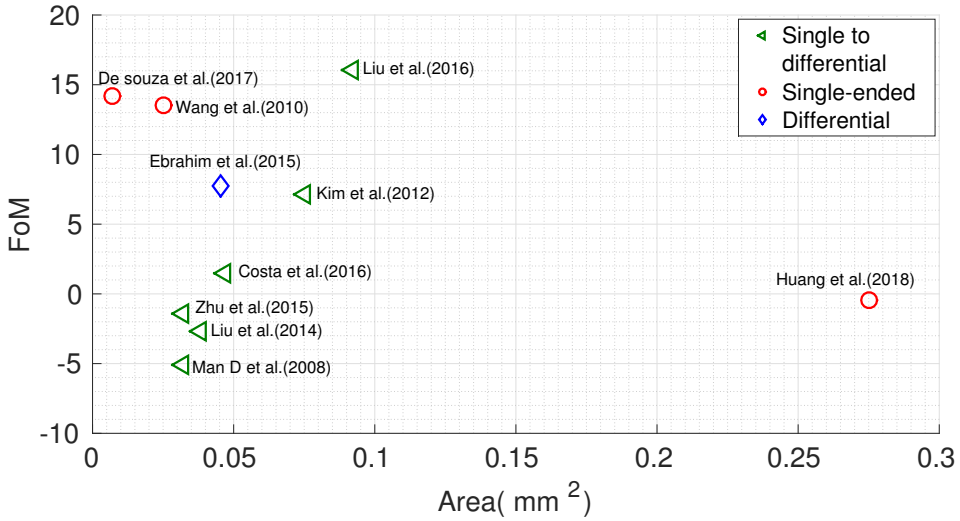


Figure 1.13: FoM comparison of recently reported LNAs.

A wide-band LNA with operating frequency of 0.2 to 2 GHz would be better choice to meet the demand of high-end devices. Furthermore, to reduce the chip area and integration complexity of target applications, an inductor-less wide-band LNA is preferred over its parallel connections of single-end counter part (Liu *et al.* (2014)).

Figure 1.13 shows the comparison of FoM versus core area of multi-band LNA. The figure of merit (FoM) reported in Pan *et al.* (2017) is used for the comparison to select most relevant parameters of LNA. The FoM is given by (1.3).

$$FoM = 20log_{10}\left(\frac{G_{max}[abs] \times BW[GHz]}{P_{DC}[mW] \times (NF[abs] - 1)}\right) \tag{1.3}$$

where G_{max} is the maximum voltage gain in linear units, BW is the bandwidth in GHz, P_{DC} is the static power dissipation in mW and NF is the noise figure in linear units. Though some of the designs have better FoM and low area, they suffer from high power consumption and requirement of additional balun inherently reduces the ratio of FoM to area.

1.5 Gap analysis

- In literature, considerable research has been conducted on a range of LNA designs, however the research is heavily biased towards the single-ended LNAs that is focused mainly on telecommunication applications.
- There are some anxious designs on fully differential LNA, in which the noise figure of additional balun hits the entire receiver performance.
- Despite its advantage single to differential (SD) (or) balun LNA design for both biomedical implants and UWB applications has not been experienced the same attention. So there exists a need to develop SD LNAs using power and noise optimization techniques at minimum gain and phase imbalance at the differential output.
- Conventional biasing topologies leads to large performance deviations under unavoidable PVT variations.
- Multi-standard high-end devices are using redundant narrow-band LNAs (expensive and area consuming) to cover the wide-band.

1.6 Motivation

In all types of receivers, low noise amplifier is the first active signal processing block and decides the important parameters of the receiver. Most of the proposed RF front-ends are using additional device (i.e., balun) to avoid (i) LO feed though and (ii) even order distortion. However, the additional balun consumes power, area and leads to signal imbalance at the output. In addition, the trade-off between image rejection and channel selection makes the design (i.e, narrow-band front-end) more complicate and power hungry. On the other hand, the design of UWB front-end demands for gain flatness at low power consumption.

In a typical wireless sensor node, transceiver consumes 50% of its overall power. Improving the power efficiency of the wireless transceiver will dramatically increase the battery life. Moreover, irrespective of bandwidth of the channel/ type of the receiver, most of the proposed LNAs are sensitive to PVT. Nowadays, there is a commercial demand for low-cost and low power medical radio and UWB portable devices. The design of low power single to differential LNA is significant for high performance RF front-ends. So, RF designers are urged to develop new methodologies that allow the design of such products.

1.7 Objectives

- To design new/improved architectures of balun LNA to avoid the use of bulky and lossy off-chip balun.
- To design bias compensation circuit that adapts and generates appropriate bias voltage / constant g_m to minimize variations in LNA parameters.
- To implement inductor-less multi-band LNA for high-end devices.
- To implement Integrated Circuits for proposed techniques.
- To validate the design by rigorous Monte Carlo simulations for PVT variations.

1.8 Organization and contribution of the thesis

The cynosure of this thesis is to implement new/alternative single to differential LNAs for narrow-band, ultra wide-band (UWB) and multi-band applications. Based on the technological background and motivation, the main interest lies in developing integrated circuits for LNA with optimum power, noise and impedance matching. In addition to this, LNA should result minimum gain and phase error to improve SNR performance.

Chapter 2, presents a background and description of performance metrics, used to assess RF design like noise figure, input intercept point, S-parameters and dynamic range. Furthermore, a brief discussion and comparison about the traditional LNA topologies is given.

Chapter 3, describes proposed approaches of balun LNA for Medical Radio communication. Primarily, a brief introduction about MedRadio communication and link budget estimation of RF front-end is given. Second, an overview of existing methods of LNA is presented. Last, a detailed discussion and analysis of both design-I and design-II is provided. In design-I power phase splitter is stacked on top of subthreshold inductive common source stage. The design-II is proposed to improve the noise performance of design-I by using additional ac coupling capacitor.

Chapter 4, starts with a brief introduction of UWB technology and target specifications of LNA. A low power noise cancellation balun low noise amplifier is proposed for ultra wide-band applications. Bandwidth extension has been achieved by stacking differential amplifier on top of the CG-CS stage with low power and minimum imbalance between the output signals. The complete analysis, post-layout simulation results and comparison with existing techniques has been devised.

Chapter 5, proposes an inductor-less balun LNA for multi-band applications. First, analysis of link budget and a review of existing techniques of multi-band LNA are explained. Second, the operation and performance of the proposed LNA is introduced with an analysis of gain, noise figure and phase error. The proposed LNA incorporates noise cancellation and voltage shunt feedback techniques to achieve minimum noise characteristics and low power consumption. In addition, the transconductance of CS stage is scaled to improve the noise performance. In this way, noise figure of LNA below 3 dB is achieved.

Chapter 6, focuses on design of bias compensation circuit to minimize performance parameters of LNA against PVT variations. A bias circuit comprises of negative feedback and charge pump to minimize performance parameter variations in sub-threshold LNA. A beta multiplier is designed to minimize parameter variations in wide-band LNA against unavoidable voltage-temperature (VT) variations.

Finally, conclude this thesis in Chapter 7, throwing highlights on possible future works and describing the pros and cons of the methods proposed and contributed as a part of this work. All the methods proposed are numerically verified and results are compared and analyzed in each chapters for the respective methods.

Chapter 2

PERFORMANCE METRICS OF LNA

2.1 Introduction

In the design of a complete wireless radio receiver, the assessment of low noise amplifier and other blocks are essentials to get a complete understanding about the performance of each individual block. The success of receiver design is measured in multiple dimensions: receiver sensitivity, selectivity, and proclivity to reception errors. The primary goal of RF design engineer is to optimize the front-end performance with a special focus on the first amplifying device. High-end receivers demand LNA with sufficient sensitivity to discern the residual signal from the surrounding noise and interference in order to reliably extract the embedded information. In the design of LNA, some characteristics are under the designers control and directly affect receiver sensitivity: noise figure, gain, bandwidth, linearity, and dynamic range. Controlling these characteristics, however, requires an understanding of the active device, impedance matching, details of fabrication and assembly to create an amplifier that achieves optimal performance with the fewest trade-offs.

Figure 2.1 shows the set of variables that affect LNA performance at the device and board design levels (Das (2013)). It is up to the designer to mitigate the impact of environmental variables, while finding the most appropriate trade-off between competing characteristics to optimize receiver sensitivity, selectivity, and maintaining information integrity. The device level trade-off depends on process technology, transistor geometry and package parasitics. All these parameters significantly affect

noise performance and should be considered while implementing the LNA. In practice, implementation of high performance LNA is difficult because of trade-off between the parameters as shown in Figure 2.2 (Nga (2012)).

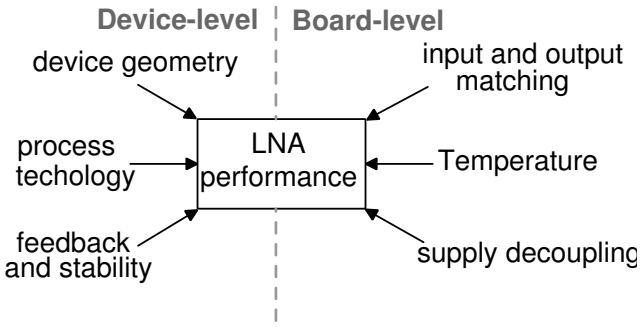


Figure 2.1: LNA performance variables at device and board level.

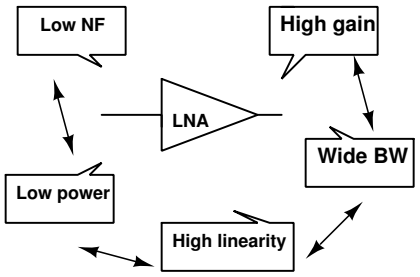


Figure 2.2: LNA design trade-off.

Table 2.1: Comparison of different LNA topologies.

Parameter	Common Source (CS)	Common Gate (CG)	Cascode
Gain	moderate	low	high
NF	best	better	good
Sensitivity to PVT	more	less	less
Reverse isolation	low	good	best
Bandwidth	low	very-wide	wide

Familiar LNA topologies have been considered for comparison with most relevant parameters. The common source topology is more attractive to design narrow-band systems. The cascode connection of same topology improves the stability and linearity. On the other hand, lower input impedance of a common gate topology makes

it attractive for the design of wide-band systems. The comparison of all the three configurations is given in Table 2.1.

2.2 Noise

In communication systems, any signal other than the desired signal is called noise and will reduce the sensitivity of the overall system. Different sources of noise with different noise generation mechanisms exist. The dominant sources of noise in integrated circuits are shot noise, flicker noise and thermal noise. Shot noise is mainly caused due to the hopping of electric charges over a potential barrier and is specific to nonlinear devices such as diodes and transistors. In MOS devices, the only source of shot noise is the DC gate leakage current and hence it is not considered as a major problem (Lee (2004)). This is in contrast with bipolar transistors in which base and collector shot noise may significantly degrade the performance of the overall receiver. Flicker noise (also known as pink noise), occurs due to the trapping of charges in the defects and impurities of the channel region in MOS devices. As a general rule, larger MOS devices experience less flicker noise. The spectral density of this noise is given by (Lee (2004)),

$$\overline{i_{fn}^2} = \frac{K.g_m^2}{fWLC_{ox}^2} \tag{2.1}$$

where K is a device-specific constant, g_m is the transconductance of the MOS device, f is the operating frequency, C_{ox} is the gate-oxide capacitance per unit area and W and L are the width and length of the MOS device respectively.

2.2.1 Thermal noise

Thermal noise is the noise caused by the agitation of carriers in a conductor and its spectral density is given by the following quantity, known as available noise power (Lee (2004)).

$$P_{NA} = kT \triangle f \tag{2.2}$$

where k is the Boltzmann constant ($1.38 \times 10^{-23} J/K$), T is the absolute temperature in Kelvins, and $\triangle f$ is the bandwidth of the noise measured in Hz. The value of P_{NA} for $1\,Hz$ of noise bandwidth at room temperature (290 K) is –174 dBm and is often called the noise floor of the system. The noise floor is an important quantity in

determining the sensitivity of the receiver (Razavi Behzad (1998)).

2.2.2 Dominant sources of noise in MOS devices

MOS device act like a transconductor in the saturation region and a resistor in the triode region. So, one can expect thermal noise associated with the carriers in the channel similar to the noise of carriers in a conductor. Van der Ziel Aldert (1986) had derived the expression for the drain current noise of MOS devices (also known as channel thermal noise), which is given as

$$\overline{i_{nd}^2} = 4kT\gamma g_{do} \triangle f \tag{2.3}$$

where g_{d0} is the drain conductance for zero drain-source voltage, γ is a technology-dependent parameter and has a value of around 2/3 for long-channel devices in saturation (in short channel devices γ is larger and its value is 3 for 180 nm technology) (Molavi (2005)). A careful examination of noise characteristics in a MOS device reveals that channel thermal noise does not fully take into account of all the noise associated with a MOS device (Shahani *et al.* (1997)). The extra noise can be modeled by introducing a frequency-dependent gate conductance:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2.4}$$

and an equivalent gate current noise is given as

$$\overline{i_{ng}^2} = 4kT\delta g_g \triangle f \tag{2.5}$$

where δ is the gate noise coefficient and is also a technology-dependent parameter. Its value is 4/3 for long channel and 6 for 180 nm technology. The gate current noise is partially correlated with the channel thermal noise and their correlation coefficient is given as:

$$c = \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \cdot \sqrt{\overline{i_{nd}^2}}} \tag{2.6}$$

where c is a complex number and its value is theoretically computed to be around –0.395 j for long channel devices as given in Van der Ziel Aldert (1986) and it is –0.55 j for 180 nm technology. Another source of noise in MOS devices that may contribute to

the total noise of LNA is noise generated by the distributed resistance of poly-silicon gate (Lee (2004)). The value of this resistance is given as:

$$R_g = \frac{R_\square W}{3n^2 L} \tag{2.7}$$

where $R_\square$ is the sheet resistivity of the gate terminal, n is the number of gate fingers, W and L are width and length of the MOS device. Different sources of noise in a MOS device are shown in Figure 2.3 (Molavi (2005)).

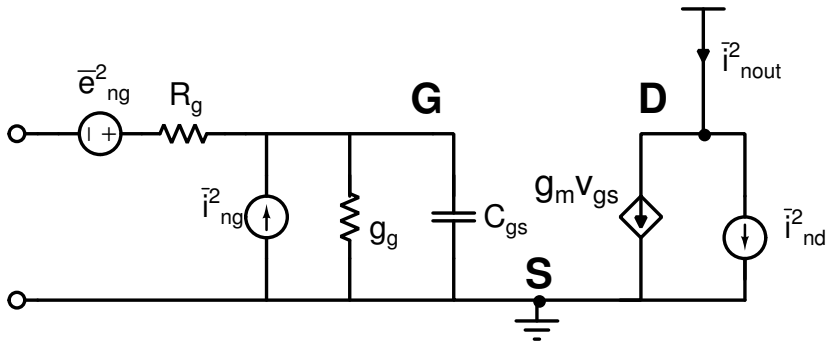


Figure 2.3: Dominant sources of noise in a MOS transistor.

2.3 Effect of gate noise on inductive source degeneration CS topology

Prior to any discussion of LNA noise factor, it is worthwhile to discuss the noise contribution of prevailing LNA topologies and briefly point out the importance of each topology.

The direct input termination of CS amplifier is shown in Figure 2.4a. This topology is more appropriate for broad-band matching than narrow-band, but the resistive termination and voltage degradation are the bottlenecks. The noise factor of this topology at the low frequency can be written as (Razavi Behzad (1998))

$$Nf = 2 + 4\frac{\gamma}{\alpha}\frac{1}{g_m R} \tag{2.8}$$

where α is $\frac{g_m}{g_{d0}}$. The noise factor of this topology is very high and is not acceptable for traditional front-end. Moreover, it is sensitive to transistor parasitics. On the other

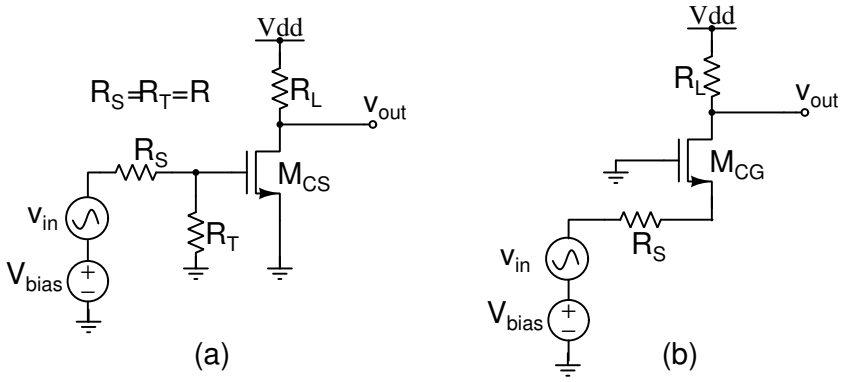


Figure 2.4: (a) Common source topology (b) Common gate topology.

side, common gate topology is shown in Figure 2.4b and the noise factor is analytically expressed as

$$\begin{aligned} Nf &= 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_S} \\ \Rightarrow Nf &= 1 + \frac{\gamma}{\alpha} \ (\because \frac{1}{g_m} = R_S) \end{aligned} \tag{2.9}$$

This topology offers impedance matching without using a resistor. The noise factor of CG topology is better than resistive terminated CS, but degrades at higher frequencies. However, this may be acceptable for wide-band amplifiers and can be improved for narrow-band using inductors. The inductive degenerated CS topology is shown in Figure 2.5. It offers good impedance matching without using physical resistor. The total drain noise current can be expressed as (Perrott (2006))

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(|\eta|^2 + 2Re\{cX_d + Z_{gsw}\} + X_d^2|Z_{gsw}|^2\right) \tag{2.10}$$

where $\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{d0}$, $\eta = 1 - \left(\frac{g_m Z_{deg}}{Z_{deg}+Z_g}\right)$, $Z_g = R_S + j\omega L_g$, $Z_{deg} = j\omega L_{deg}$, $X_d = \frac{g_m}{g_{d0}}\sqrt{\frac{\delta}{5\gamma}}$ and $Z_{gsw} = \frac{1}{j\omega C_{gs}} \parallel \frac{Z_{deg}+Z_g}{1+g_m Z_{deg}}$.

The additional inductor (L_g) gives freedom to set resonance frequency (ω_0) and Z_{in} independently. For 180 nm technology, (2.10) can be written as

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(|\eta|^2 + 2Re\{-j|c|X_d^* Z_{gsw}\} + X_d^2|Z_{gsw}|^2\right) \tag{2.11}$$

where η=1/2, $Z_{gsw} = \frac{1}{2}(2Q_{in} - j)$ and Q_{in} is the quality factor of input RLC network and it is given as

$$Q_{in} = \frac{1}{2\omega_0 R_S C_{gs}} = \frac{\omega_0(L_g + L_{deg})}{2R_S} \tag{2.12}$$

Now the simplified expression of (2.11) is

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\frac{1}{4}\left(1 - 2|c|X_d + (4Q^2 + 1)X_d^2\right) \tag{2.13}$$

The output noise due to the input source is given as

$$\overline{i_{nout}^2} = \left(g_m Q_{in}\right)^2 \overline{v_{nR_S}^2} \tag{2.14}$$

The alternate definition of noise factor is

$$Nf = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ input\ source} \tag{2.15}$$

Now the noise factor of IDCS stage is given as

$$\begin{aligned} Nf &= \frac{\left(g_m Q_{in}\right)^2 \overline{v_{nR_S}^2} + \overline{i_{ndg}^2}/\Delta f}{\left(g_m Q_{in}\right)^2 \overline{v_{nR_S}^2}} \\ &= 1 + \left(\frac{\omega_0}{\omega_t}\right)\gamma \underbrace{\left(\frac{g_{d0}}{g_m}\right)\left(\frac{1}{2Q_{in}}\right)\left(1 - 2|c|X_d + (4Q_{in}^2 + 1)X_d^2\right)}_{\text{Noise scaling factor}} \end{aligned} \tag{2.16}$$

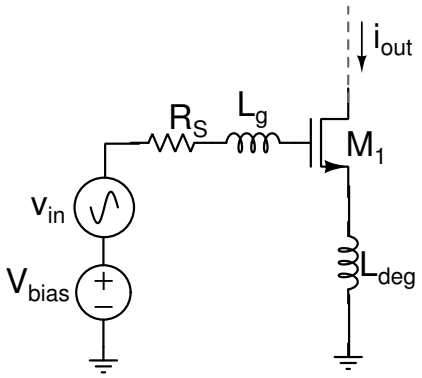


Figure 2.5: Inductive degeneration common source topology.

In (2.16), the noise factor is mainly decided by the ratio of $\left(\frac{\omega_0}{\omega_t}\right)$ and the highlighted portion i.e., noise scaling factor (NSF). To analyze the effect of Q_{in} on the noise factor, we have investigated the variations in NSF against variations in Q_{in} as shown in Figure 2.6. It has been observed that, for $180\,nm$ technology, the value of Q_{in} should not be more than 8. If the Q_{in} is high, the gate noise dominates the thermal noise and leads to poor noise performance.

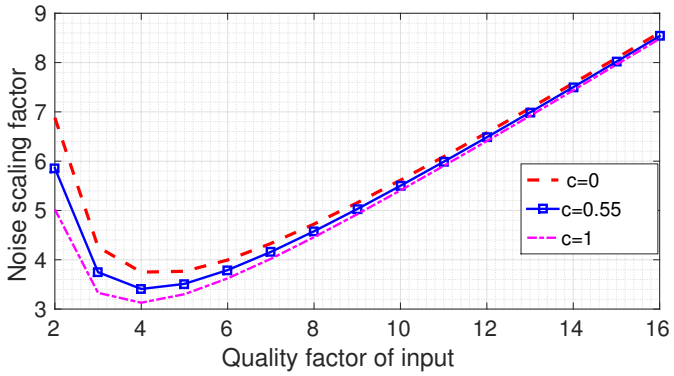


Figure 2.6: Analysis of variation in noise scaling factor against Q_{in}.

2.4 Noise Figure (NF)

Noise figure (NF) is a measure of signal to noise ratio (SNR) degradation as the signal traverses the receiver front-end. Mathematically, Harold Friis defined the noise factor (Nf) as the ratio of the input SNR to the output SNR of the system. The Nf is given by

$$Nf = \frac{SNR_{i/p}}{SNR_{o/p}} \tag{2.17}$$

The noise factor can also be expressed as

$$Nf = \frac{P_{sig}/P_{nR_S}}{SNR_{o/p}} \tag{2.18}$$

where P_{sig} is the input signal power and P_{nR_S} represents the source resistance noise power per unit bandwidth. It follows that:

$$P_{sig} = P_{nR_S} \times (Nf) \times SNR_{o/p} \tag{2.19}$$

The input signal power is distributed across the channel bandwidth, so the total mean square power can be written as

$$P_{sig,tot} = P_{nR_S} \times (Nf) \times SNR_{o/p} \times B \tag{2.20}$$

where B is the bandwidth. The noise performance of a system decides the lower limit of dynamic range. The Nf generally represented in decibels (dB) and it is referred as noise figure (NF).

$$NF = 10 \log_{10}(Nf) \tag{2.21}$$

Now the final expression of NF from (2.20) is given as

$$NF = P_{sig,min}(dB) - (-174\,(dBm/Hz)) - SNR_{o/p,min}(dB) - 10 \log_{10} B \tag{2.22}$$

NF can be defined for each block as well as the entire receiver. NF_{LNA}, for instance, determines the inherent noise of LNA, which is added to signal through the amplification process. In 1947, Friis had derived the noise factor for a cascaded system of m stages and it is given as

$$Nf_{tot} = Nf_1 + \frac{Nf_2 - 1}{A_{p1}} + \frac{Nf_3 - 1}{A_{p1}A_{p2}} + ... + \frac{Nf_m - 1}{A_{p1}A_{p2}..A_{p(m-1)}} \tag{2.23}$$

where Nf_i and A_{pi} are noise factor and power gain of i^{th} stage. From (2.23) it can be observed that noise contributed by each stage decreases as the gain of preceding stage increases. Thus, the gain and noise factor of first stage decides the entire receiver noise performance. In practice, the LNA is the first active block in the receiver chain, so it is responsible for high gain, low noise and should capable with substantial unwanted signals.

2.5 Sensitivity

It is the minimum signal level that a receiver/LNA can detect with acceptable quality. We define acceptable quality as sufficient SNR. Usually for a good receiver it should be as low as possible. Mathematically it is expressed as

$$P_{sen}(dBm) = -174(dBm/Hz) + NF(dB) + SNR_{o/p,min}(dB) + 10 \log_{10} B \tag{2.24}$$

where B represents bandwidth of the RF system in Hz and $SNR_{o/p,min}$ is the minimum SNR in dB at the output of the system/amplifier.

2.6 Distortion and intermodulation

The small signal analysis of analog and RF circuits can be approximated by linear model, but the real life circuits exhibit some degree of nonlinearity results in harmonic distortion (Razavi Behzad (1998)).

2.6.1 Harmonic distortion

If a sinusoidal signal (i.e., $\mathrm{A}\cos\omega t$) is applied to a non-linear memoryless system, the output exhibit not only fundamental frequency, but also integer multiples of input frequency (also called as harmonics). The general expression of non-linear system is given as

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + ... \tag{2.25}$$

where $x(t)$ and $y(t)$ are input and output of a non-linear system. Now the gain of the non-linear system becomes decreasing function of $(\alpha_1 A + \frac{3}{4}\alpha_3 A^3)$, where A is the magnitude of the given input signal. The decrement in gain is called as gain compression and leads to deviation of gain from its ideal characteristics. The most common measures of non-linearity are the 1-dB compression point and the third-order intercept point (IP_3).

2.6.1.1 1-dB compression point

The point at which the practical power gain deviates from its ideal by 1 dB is called as 1-dB compression point. Mathematically, the peak voltage of 1-dB compression is given by

$$A_{in,1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.26}$$

2.6.1.2 Input Intercept Point (IIP)

It is the input level beyond which circuit becomes excessively nonlinear because of the presence of intermodulation components. For a good receiver/LNA it should be as high

as possible. If a weak signal accompanied by two strong interferes experiences third-order non-linearity, then one of the intermodulation (IM) product falls in the band of interest, corrupting the desired component. The 'intercept point' (IP) has been defined to characterize the corruption of signals due to third-order intermodulation of two nearby interferers. It is measured by a two-tone test where two signals are having equal amplitude. The input signal level, where the power of the third-order IM product equals to that of the fundamental is defined as two-tone input-referred third-order intercept point (IIP_3) and the corresponding output level is called the output third-order intercept point (OIP_3).

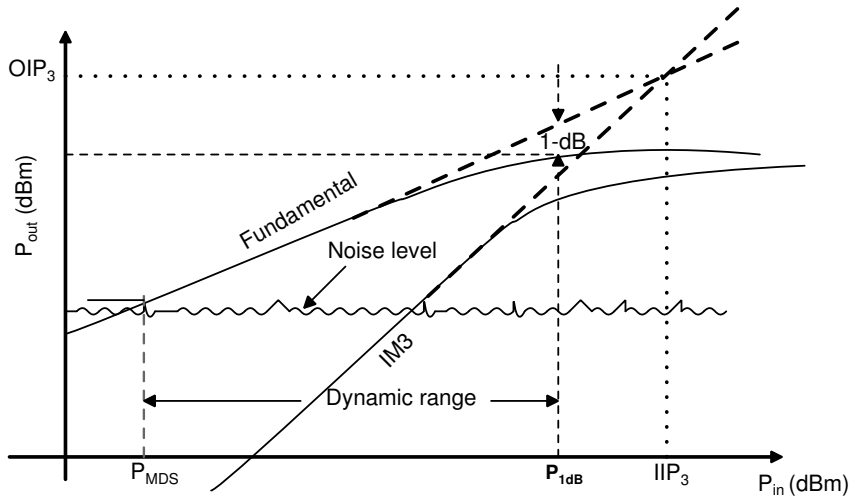


Figure 2.7: Illustration of P_{1dB}, IIP_3 and dynamic range (logarithmic scale).

Dynamic range is the ratio of maximum input level that a receiver can tolerate to minimum input level that it can detect. Usually for a good receiver it should be as high as possible. The maximum level of input signal decides the amount of distortion that the circuit generates. The lower limit on the input (P_{MDS}) is determined by the noise contribution of the circuit. Calculation of IIP_3, P_{1dB} and dynamic range are shown in Figure 2.7.

2.7 S-Parameters

Generally to assess two-port networks we prefer Z, Y and h-parameters. To find these parameters, it is necessary to conduct open and short circuit test, but at higher frequencies it is very difficult to conduct the same because of the presence of parasitic

capacitances and inductances. The inability to perform short and open circuit tests and the possibility of harming the circuit during these tests suggest the use of an alternative solution to characterize the network at high frequencies as given in Collin (1993). One popular solution is the introduction of the S-parameters (S-refers to scattering), which defines the four variables as the incident (reflected) input (output) voltage (or power) waves.

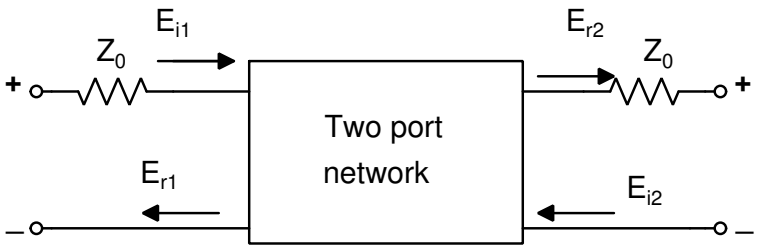


Figure 2.8: S-parameters definition of two port networks.

The definition of S-parameters exploits the fact that a transmission line terminated at its characteristic impedance does not reflect any power at its termination (Lee (2004)). To show the usefulness of this property, consider the block diagram of a two-port network shown Fig. 2.8, where Z_o is the impedance of the source and the load terminations and E_{i1} and E_{r1} are the magnitudes of incident and reflected voltage waves, respectively. The S-parameter coefficients are expressed as:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.27}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.28}$$

where $a_1 = \dfrac{E_{i1}}{\sqrt{Z_0}}$, $a_2 = \dfrac{E_{i2}}{\sqrt{Z_0}}$, $b_1 = \dfrac{E_{r1}}{\sqrt{Z_0}}$ and $b_2 = \dfrac{E_{r2}}{\sqrt{Z_0}}$

The normalization to the square root of Z_o makes the square of magnitude of a_i and b_i equal to the incident and reflected power at both ports. Now, if we terminate second port with Z_o, which sets a_2 equal to zero, and apply a power source to port one, we obtain the following relations:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \frac{E_{r1}}{E_{i1}} \tag{2.29}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{E_{r2}}{E_{i1}} \tag{2.30}$$

where S_{11} is referred as the input reflection coefficient and is a practical measure for the impedance matching at input port of the LNA, S_{21} represents the forward gain of the amplifier. On the other hand, if port one is terminated to Z_o and power is sent from port 2, we have the following relations:

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = \frac{E_{r1}}{E_{i2}} \tag{2.31}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = \frac{E_{r2}}{E_{i2}} \tag{2.32}$$

where S_{12} is the reverse transmission or gain and S_{22} is called as the output reflection coefficient of the network. Using these definitions, we can predict that a good amplifier should possess a large S_{21} to achieve high gain, small S_{11} and S_{22} for good input and output matching, and very small S_{12} to ensure the stability and reverse isolation. The typical value of S_{21} is $>10\,\text{dB}$, S_{12} is $<$–$40\,\text{dB}$ and input and output reflection coefficients are less than $-10\,\text{dB}$, which may vary according to the type of applications.

Chapter 3

LOW POWER HIGH SELECTIVITY SD LNA

3.1 Introduction

In 2009, federal communications commission (FCC) introduced medical device radio service (MedRadio) dedicated for both implantable and wearable medical devices covering the frequency range of 401-406 MHz and channel bandwidths from 100 kHz to 300 kHz for distances less than 10 m (FCC (2009)). The main advantage of medical devices is their motivation for flexibility and cost-effective health monitoring in hospitals and homes. MedRadio spectrum is used for diagnostic and therapeutic purposes in implanted as well as devices worn on a body. MedRadio devices include implanted cardiac pacemaker and defibrillator as well as neuromuscular stimulator that helps to restore sensation, mobility and other functions to limbs and organs. Although the future is promising, there are several design challenges for wireless medical devices (Ba *et al.* (2015)). The transceiver of medical device dominates the overall power consumption. Hence, low power designs are to be investigated to enhance the battery life. Improving the sensitivity of the front-end will dramatically increases the receiver performance. The essential requirement of MedRadio LNA is to sense very small signals ranging from micro to nano volts without causing any significant distortion. Furthermore, the LNA should be optimized for power, noise and impedance without compromising other performance parameters. So, low power single to differential (SD) LNA would suit better in order to build efficient receiver front-end for MedRadio communication.

3.2 Specifications of MedRadio

The maximum radiated power from MedRadio transmitter to the base station is –16 dBm. Assuming the distance between medical device and base station is 10 m, then the free space path loss (FSPL) can be calculated as

$$FSPL = 20\,log(\frac{4\pi df}{c}) \tag{3.1}$$

where d is the distance in km and f is the frequency in MHz. After attenuation due to fade margin, switching and body loss (e.g.,total of 35 dB), the signal level at the receiver can be calculated as

$$P_R = EIRP - FSPL - fade\ margin + G_R \tag{3.2}$$

From (3.1) and (3.2), the maximum/minimum received signal power at the input of LNA is –55 dBm/–97 dBm. Now, the sensitivity of system is given as (Razavi Behzad (1998))

$$P_S = -174\,dBm + 10\log_{10}\,BW + NF_{R_X} + SNR_{R_X} \tag{3.3}$$

where SNR_{R_X} is the minimum SNR at the output of receiver, BW is the signal bandwidth and NF_{R_X} is the noise figure of the receiver. Assuming differential quadrature phase shift keying (DQPSK) modulated data at the rate of 200 kbps, 10 dB SNR and bit error rate (BER) of 10^{-3} with 100 kHz BW, then noise figure is budgeted to be 16 dB to achieve sensitivity of –97 dBm. As per the estimation of other blocks, the noise figure of front-end will be 10 dB.

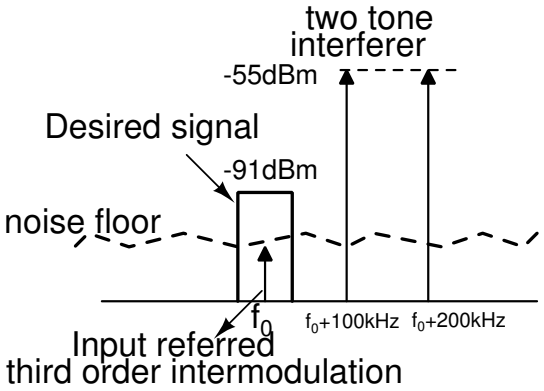


Figure 3.1: Estimation of IIP_3.

There is no unified third order intercept point (IIP_3) for MedRadio. Thus, assumptions are made as shown in Figure 3.1. The IIP_3 should be less than the noise floor. It is given mathematically as

$$P_{IM3,in} \leq P_s - SNR_{R_X} \tag{3.4}$$

where $P_{IM3,in}$ is power level of input referred intermodulation tone. Now the IIP_3 of the RF front-end is defined by (Lee (2004))

$$IIP_3 \geq P_{in} + \frac{P_{in} - P_{IM3,in}}{2} \tag{3.5}$$

where P_{in} is the power level of the interferer. Assuming that the interferes are at maximum allowed level and no FSPL, then IIP_3 of front-end is calculated as –30 dBm. The main specifications of MedRadio receiver front-end are given in Table 3.1 (Mercier and Chandrakasan (2015), Cha *et al.* (2011), Copani *et al.* (2011)).

Table 3.1: Specifications of MedRadio RF front-end.

Parameter	Value
[a]Maximum Effective Isotropic Radiated Power (EIRP)	−16 dBm
[a]Maximum/minimum received signal power	−55.6 dBm/−97 dBm
[b]Noise figure at sensitivity=–98 dBm and BW=100 kHz	10 dB
[b]IIP_3	>-30 dBm
[b]Power dissipation	$\leq 500\,\mu$W
[b]Gain and phase difference	<1 dB and $< 10°$

[a]Given by MedRadio standard [b]Target specifications

3.3 Preliminaries

The primary goal in the design of LNA is input impedance matching. There are many topologies available to match the input impedance of LNA to 50 Ω as shown in Figure 3.2 (Lu *et al.* (2006)). A simple resistor terminated CS stage provide 50 Ω impedance matching, is shown in Figure 3.2(a). The use of resistors in this fashion has a deleterious on noise performance, moreover it also attenuates the input signal

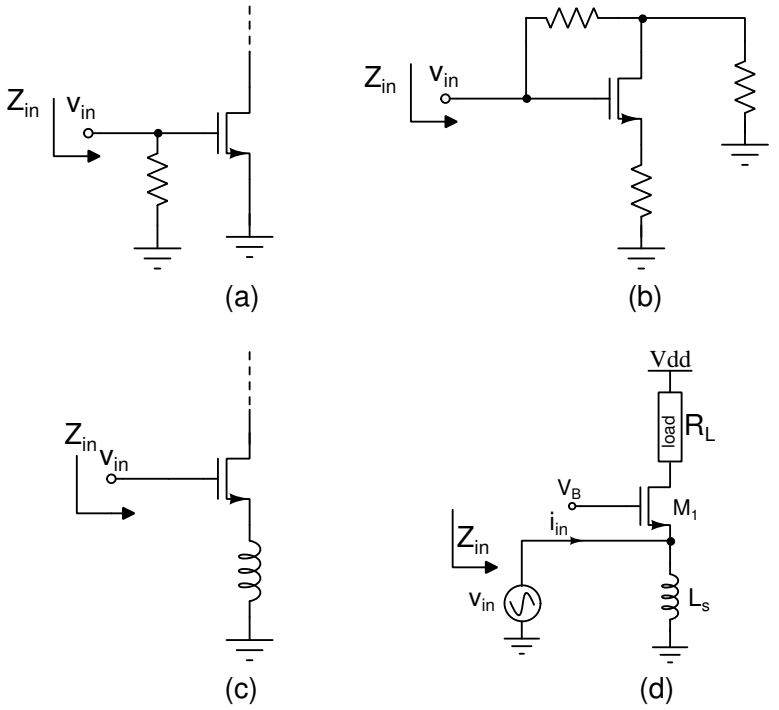


Figure 3.2: LNA architectures (a) Simple resistive termination (b) Shunt-series feedback (c) Inductive source degeneration (d) Common Gate stage.

before applying to the transistor. Figure 3.2(b) illustrates another topology of CS with a shunt-series feedback resistor to match the input and output impedances of LNA. The feedback resistor adds noise to the incoming signal and it should have reasonable quality to fabricate on the chip. However, in CMOS technologies high quality resistors are generally not available.

The third architecture does not use any physical resistor as shown in Figure 3.2(c). It employs inductive source degeneration so as to generate a real term in the input impedance. Note that IDCS topology is very popular for narrow-band applications since input matching series resonant network provides pre-amplification and superior noise performance (since no physical resistor is used for matching). The common gate (CG) technique for wide-band impedance matching is shown in Figure 3.2(d). The smaller input impedance of CG stage makes it attractive for UWB design. The input impedance can be calculated as (Razavi Behzad (1998))

$$\frac{v_{in}}{i_{in}} = \frac{R_L + r_o}{1 + g_m r_o} \tag{3.6}$$

where r_o is the output impedance of transistor M_1. The input parasitic (e.g., bond pad, etc.) is absorbed by resonate network, which is problematic in IDCS topology (i.e., degrades the impedance matching performance). The noise figure (NF) of CG stage is little bit high, but it is independent of ω (frequency of operation) and remains nearly constant irrespective of bandwidth. So the wide-band impedance matching of this technique inspired us to use the CG topology in UWB applications.

3.4 Prior work

Many techniques have been proposed to design MedRadio LNA with inevitable balun device (Dehghani and Abouei (2013), Cruz *et al.* (2015), Mohamed and Sherif (2013)). The additional balun is power hungry and deteriorate gain and phase balance (Martins *et al.* (2011)). In literature, there are very few techniques that have been proposed for single to differential LNA (Wu *et al.* (2011), Tang *et al.* (2011)), but these techniques have not been focused on power and imbalance between differential signals at the output. A low power single-ended complimentary current re-use LNA (CCRLNA) has been reported for MedRadio (Cha *et al.* (2011)).

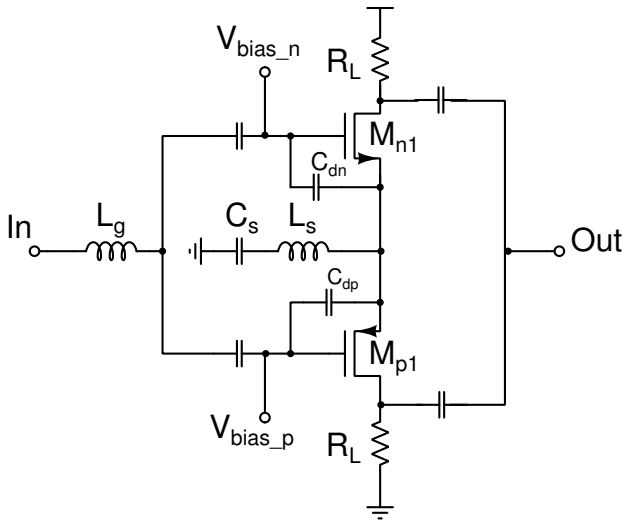


Figure 3.3: Complementary current re-use LNA.

The circuit diagram of CCRLNA is shown in Figure 3.3. In this design a complementary current re-use topology has been employed. This technique does not require any dc feedback circuitry to define biasing point, because an NMOS CS amplifier

is stacked on a PMOS stage to reuse the dc current. Due to low current, the drop across load resistor R_L is less and major portion of the gain is only provided by passive network. Nevertheless, CCRLNA consumes low power (150 μW), the additional headroom and inevitable balun are the bottlenecks. Moreover, the performance parameters of CCRLNA are sensitive to both component (since major portion of the gain is provided by input matching network) and PVT variations. In addition to this, the LNAs proposed by Dehghani and Abouei (2013), Ba *et al.* (2015) are based on IDCS topology which suffer from high power and need additional balun in the front-end.

To improve the gain and linearity, a differential CG-CS LNA is proposed as shown in Figure 3.4 (Mohamed and Sherif (2013)). It is a combination of cross-coupled capacitors and PMOS transistors. The differential input signals are given to the sources of M_{N1}, M_{N2} and are also connected to the gate of opposite NMOS transistors through capacitors, creating a shunt-series negative feedback. The input and output impedances are controlled by both negative and positive feedbacks. However, the linearity degradation by the positive feedback and high power consumption are bottlenecks. So the stumbling balun and low power stipulation of MedRadio motivated us to develop an alternative technique for single to differential LNA.

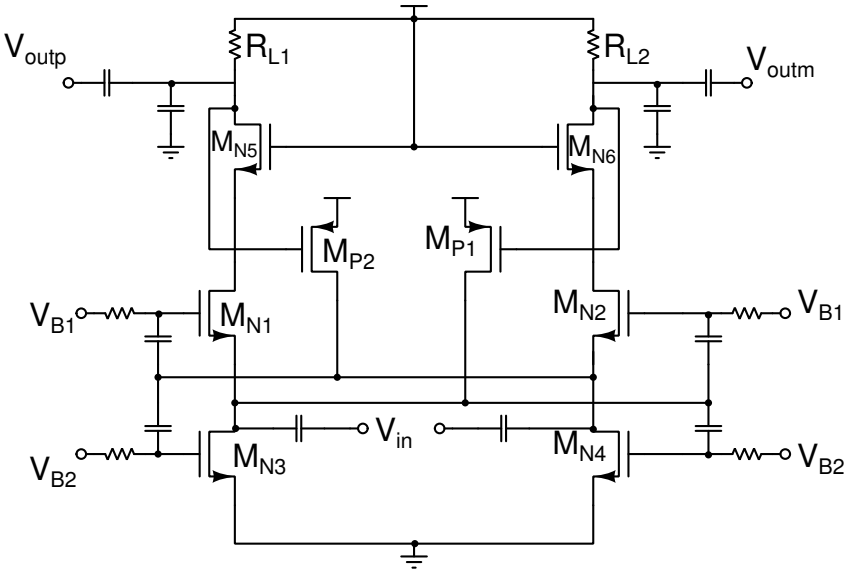


Figure 3.4: Fully differential CG-CS LNA.

3.5 Basic idea and implementation

Current leakages are ever present in the electronic systems, and many forms of leakage are considered by engineers to be unusable. It is exploited that sub-threshold leakage currents of MOSFET can be used for analog applications. A precise control of sub-threshold region offers a new frontiers in ultra-low power design. A finite (non-zero) current does flow in a MOSFET even for gate voltages below the threshold voltage and this effect is more marked for short channel length devices than their long channel counterparts. In strong inversion region, MOSFET model is based on the assumption that the inversion charge Q_I goes to zero when the gate voltage drops below the threshold voltage. However, this is not true for values below V_{TH}, the channel charge drops exponentially with decreasing gate voltage, as shown in Figure 3.5 (Sheu *et al.* (1987)).

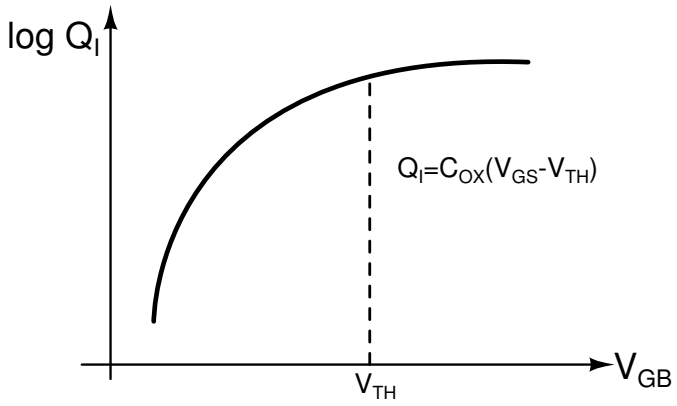


Figure 3.5: Charge variation below threshold voltage .

In sub-threshold region, the current is due to diffusion of carriers and is given by

$$I = I_S\left(\frac{W}{L}\right)exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)\left[1-exp\left(\frac{-V_{DS}}{\eta V_T}\right)\right] \tag{3.7}$$

where I_S is the specific current and is given by $I_S = 2\eta\mu_n C_{OX}V_T^2$. V_{TH} is the threshold voltage of the transistor, V_T is the thermal voltage and η is the sub-threshold slope which is a constant with an approximate value of 1.27. We can neglect V_{DS} term when $V_{DS} \gg 4V_T$. In sub-threshold region, there is a possibility to get high g_m over I_D, which is much needed to reduce noise figure. Though g_m over I_D values are higher than strong inversion region, the value of g_m is smaller. Here, g_m cannot be increased

by increasing W/L values, but can happen if current density is kept constant. In sub-threshold region g_m can be given as

$$g_m = \frac{KI_D}{V_T} \tag{3.8}$$

where K is constant. It is concluded that a low power design is possible by operating core transistor in sub-threshold region. Apart form low power requirement of MedRadio front-end, there are many other challenges like LO feed through, filters with high-Q and additional balun. So, to mitigate all these issues a high selectivity single to differential LNA is proposed by stacking differential converter on top of sub-threshold IDCS topology. The architecture of MedRadio front-end with proposed LNA is shown in Figure 3.6.

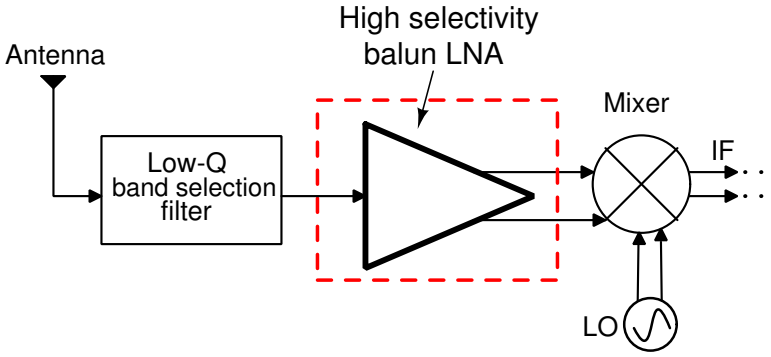


Figure 3.6: Block diagram of MedRadio front-end using proposed LNA.

The main agenda of proposed LNA is to reduce the power consumption and avoid the use of bulky external components for balun and image rejection filter. However, the exponential dependency of g_m on the gate overdrive voltage results in large variations against PVT. Moreover, the variation in threshold voltage leads to fluctuation of the transistor operating region from sub-threshold to moderate and strong inversion. Thus, the impedance matching, noise figure and power will deviate from the target specifications.

In this chapter, two sub-threshold balun LNA designs have been proposed for MedRadio applications. The circuit topology is based on current re-use technique to have low power design. The balun LNA adopts power constrained simultaneous noise impedance matching (PCSNIM) technique, that was proposed by (Andreani and Sjöland (2001)) to optimize power, noise and impedance matching. In our work, the idea is further extended such that a sub-threshold IDCS topology ensures better per-

formance than PCSNIM. Moreover, differential conversion of input signal is achieved by stacking a cascaded stage on top of the IDCS stage. The proposed LNA uses LC tank as the load at both stages, which inherently increases the selectivity. Thus, a conventional band selection filter with low quality factor is adequate rather than a high-Q filter.

3.6 Proposed design-I

The schematic of sub-threshold PCSNIM technique is shown in Figure 3.7. The PCSNIM technique is known for achieving a good noise and impedance matching performance with low power. However, in order to achieve DC current less than 400μA (considering the target power dissipation of less than $500\,\mu$W and supply voltage less than 1.8 V), the transistor M_1 must be biased in sub-threshold region. Though this region of operation has low IIP_3, it will provide higher g_m/I_D ratio at low power consumption (suitable for MedRadio specifications). An additional inductor L_g is used to set ω_0 and L_{deg} independently. Furthermore, an external capacitance C_{ex} is used to reduce the value of L_{deg} for better noise performance. The variation of L_g affects both ω_0 and quality factor (Q_{in}) of input matching network as shown in Figure 3.8. The low values of L_g increase the bandwidth, but degrades both gain and noise performance. Proper choice of Q_{in} provides noise optimization along with passive amplification (i.e., inductive peaking). The design of sub-threshold IDCS stage is pivotal since it decides the power consumption and other important parameters of the proposed balun LNA.

In the proposed balun LNA, sub-threshold IDCS topology (stage-I) is used to match impedance with antenna and provide good gain and linearity at minimum power. So a good start must be required to avoid multiple iterations in the design of stage-I. The design flow of proposed sub-threshold IDCS topology is given in Figure 3.9. The good starting point is the design of load tank, sizes of transistors and other components (i.e., Inductors and capacitors). In general, noise of a MOS transistor is modeled by thermal noise of both drain and gate. The power spectral density of drain thermal noise is $4kT\gamma g_{d0}$. It is almost constant and has less impact on narrow-band operation as compared to the wide-band. The influence of gate noise is sensitive to source impedance of MOSFET and it has more impact if the source impedance is reactive when compared with resistance. In this case, the gate noise contribution is a function of Q_{in} and at some value of Q_{in}, gate noise exceeds the drain noise. The gate noise of M_1 becomes dominant at higher value of Q_{in}.

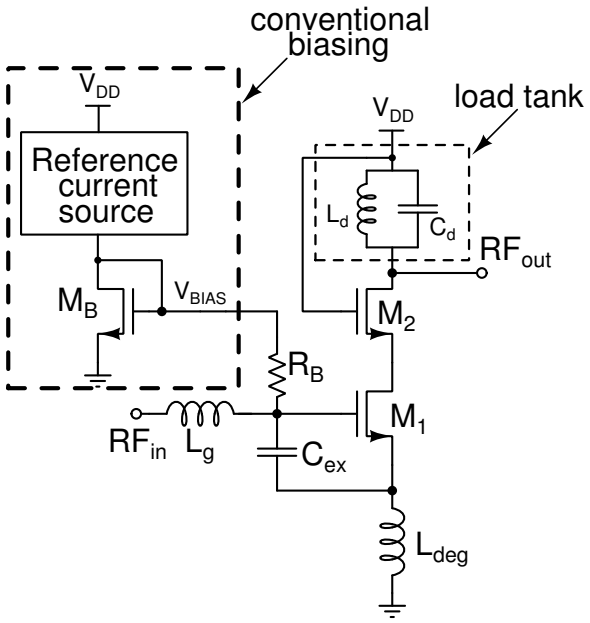


Figure 3.7: PCSNIM LNA with conventional biasing.

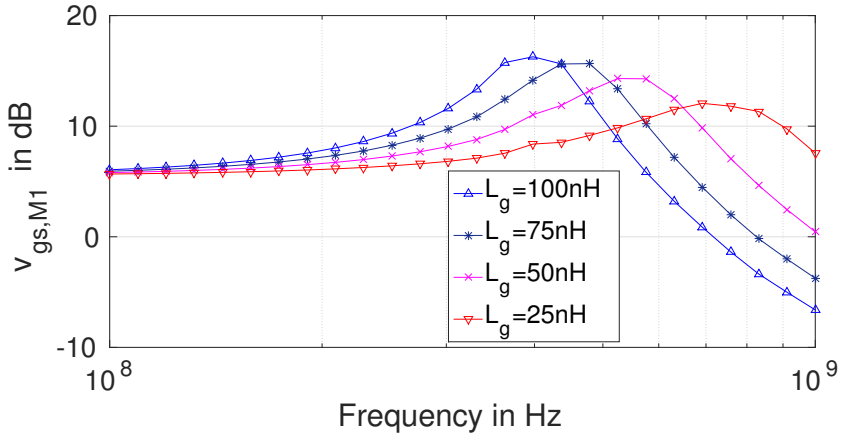


Figure 3.8: Variation of ω_0 and Q_{in} against L_g.

Noise factor of transistor M_1 in Figure 3.7 is given as

$$Nf = 1 + (\frac{\omega_0}{\omega_T})\gamma(\frac{g_{d0}}{g_m})\frac{1}{2Q_{in}}\underbrace{(1 - 2cX_d + (4(Q_{in})^2 + 1)X_d^2)} \tag{3.9}$$

where γ is excess noise coefficient, ω_T and ω_0 are transition and operating frequency, g_{d0} is the transconductance at $V_{DS} = 0$, c is the noise correlation factor of gate and

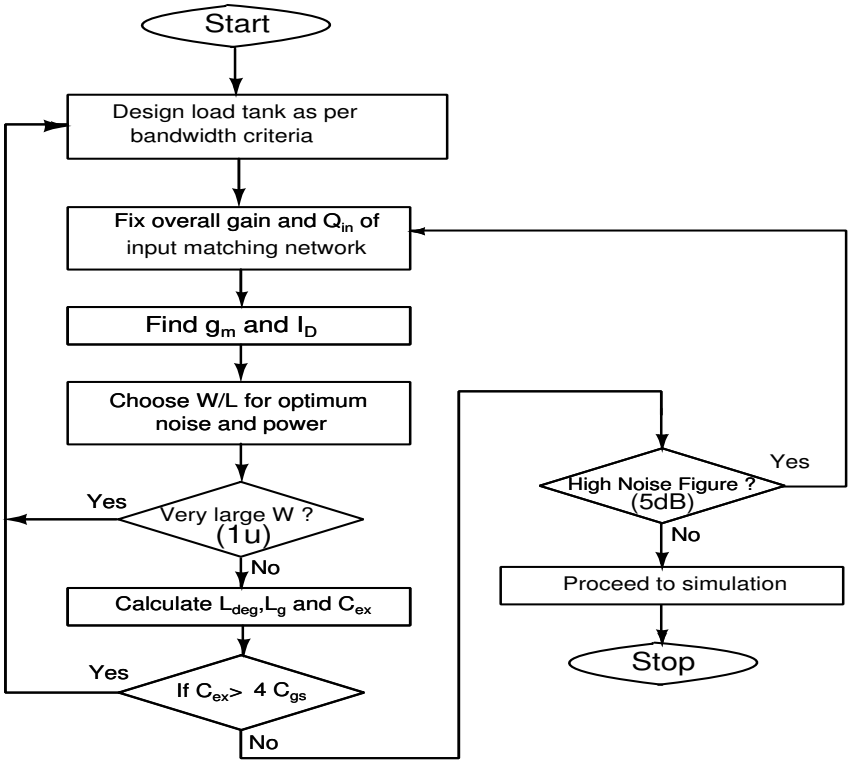


Figure 3.9: Design flow of sub-threshold IDCS topology.

drain. Q_{in} and X_d are determined from circuit elements as given by

$$Q_{in} = \frac{1}{2\omega_0(C_{ex} + C_{gs})R_s} = \frac{\omega_0(L_{deg} + L_g)}{2R_s} \tag{3.10}$$

and

$$X_d = \frac{g_m}{g_{d0}}\sqrt{\frac{\delta}{5\gamma}} \tag{3.11}$$

where δ is gate noise coefficient. In (3.9), the highlighted term is gate noise contribution as a function of Q_{in}. So the selection of Q_{in} and dimensions (W/L) of input transistor has enormous impact on noise factor and f_T respectively. Furthermore, the selection of Q_{in} impacts the overall gain of the balun LNA. The complete circuit diagram of proposed balun LNA is shown Figure. 3.10. The proposed LNA comprises of stacking of a power phase splitter (stage-II) on top of sub-threshold IDCS stage. A cascode transistor (M_2) is used to avoid reflections from load to source. The balanced differential conversion has been achieved by stacking power phase splitter on top of the first stage. A simple differential amplifier is used as power phase splitter. Under

the resonance condition, impedance seen in to the stage-I is very high which actually establishes the single to differential conversion (Lee and Lai (2007)). The value of C_{ff} has taken larger than C_{gs3} to avoid the loss of signal strength while transferring from stage I to II. The gain and phase imbalance between differential outputs has been curtailed using feedback capacitor C_{fb}.

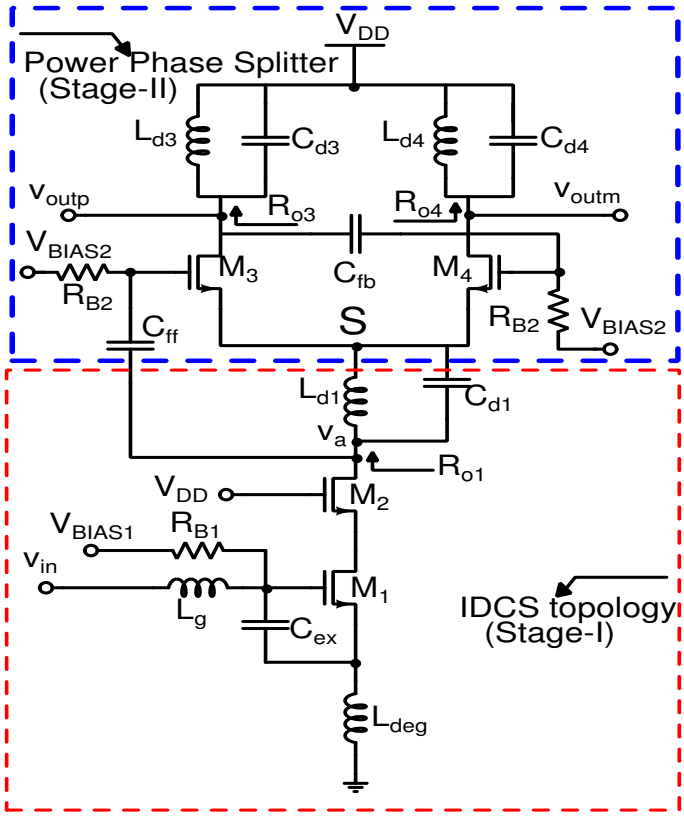


Figure 3.10: Proposed sub-threshold balun LNA (Biasing circuit is not shown).

3.6.1 Gain analysis

The small signal analysis of proposed balun LNA is shown in Figure 3.11. To make the analysis simple, channel length modulation has been neglected. The input matching network provides passive amplification for the incoming RF signal by Q_{in} times. The gate to source voltage of M_1 is given as

$$v_{gs,M_1} = \frac{v_{in}}{2\,R_S + \dfrac{1}{\omega C_t} + \omega L_t} . \frac{1}{\omega C_t} \tag{3.12}$$

where $C_t = C_{gs} + C_{ex}$ and $L_t = L_g + L_{deg}$. Now at the resonance condition i.e., $\omega = \omega_0$

$$v_{gs,M_1} = \frac{v_{in}}{2\,R_S\omega_0 C_t} = Q_{in}v_{in} \tag{3.13}$$

The output voltage at the first stage can be calculated as

$$v_a = -g_{m1}Q_{in}v_{in}R_{o1} \tag{3.14}$$

where R_{o1} is the output impedance of stage-I at the resonance. The current through M_3 is given as

$$i_{d3} = -g_{m3}g_{m1}Q_{in}v_{in}R_{o1}\frac{C_{ff}}{C_{gs3} + C_{ff}} \tag{3.15}$$

The current through M_4 is almost same as i_{d3} (some portion of i_{d3} sinks in to the load tank of first stage which can be compensated by C_{fb} as explained in the following section). Now the output voltage v_{outp} is given as

$$v_{outp} = g_{m3}g_{m1}Q_{in}v_{in}R_{o1}\frac{C_{ff}}{C_{gs3} + C_{ff}}R_{o3} \tag{3.16}$$

The gain of proposed balun LNA can be calculated as

$$gian = \frac{v_{outp}}{v_{in}} = g_{m3}g_{m1}Q_{in}R_{o1}\frac{C_{ff}}{C_{gs3} + C_{ff}}R_{o3} \tag{3.17}$$

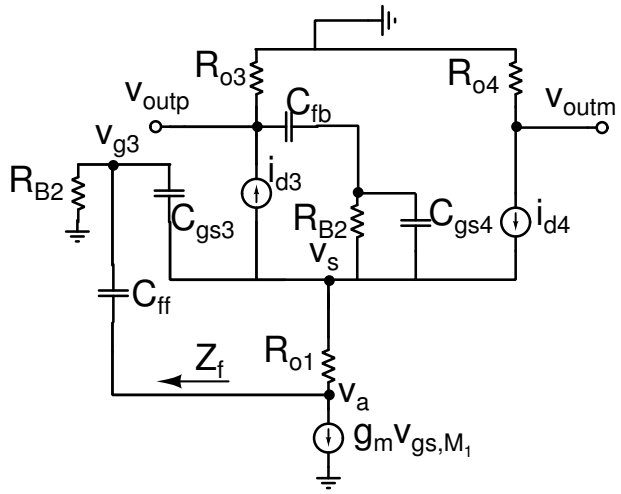


Figure 3.11: Small signal analysis of proposed balun LNA.

3.6.2 Effect of C_{fb} on gain and phase

It can be seen that same current flows through M_1 and M_2. Hence $i_{d1} = i_{d2}$, given by

$$i_{d1} = i_{d2} = -g_{m1} Q_{in} v_{in} \tag{3.18}$$

The voltage at the node v_a is calculated as

$$v_a = -g_{m1} Q_{in} v_{in} R_{o1} \tag{3.19}$$

Now voltage at the input of M_3 is

$$v_{g3} = -g_{m1} Q_{in} v_{in} R_{o1} \frac{C_{ff}}{C_{gs3} + C_{ff}} \tag{3.20}$$

The current through M_3 is

$$i_{d3} = -g_{m3} v_{g3} \ (since\, v_s \simeq 0) \tag{3.21}$$

Under the resonance condition same current (i.e., i_{d3}) has to flow through M_4, but the non-ideal of first stage load tank sinks some portion of i_{d3}. This error between i_{d3} and i_{d4} is fountainhead for gain and phase imbalance. A feedback capacitor (C_{fb}) is connected to compensate the imbalance between output signals. The compensation current flows through M_4, is given by

$$i_{Cfb,M_4} = g_{m4} g_{m3} g_{m1} Q_{in} v_{in} R_{o1} R_{o3} \frac{C_{ff}}{C_{gs3} + C_{ff}} \frac{C_{fb}}{C_{gs4} + C_{fb}} \tag{3.22}$$

Now the total current flowing through M_4 is

$$i_{d4} = p i_{d3} + i_{Cfb,M_4} \tag{3.23}$$

The simplification of (3.23) gives

$$p + g_{m4} R_{o3} \frac{C_{fb}}{C_{gs4} + C_{fb}} = 1 \tag{3.24}$$

From (3.24), it is obvious that gain and phase error can be adjusted by choosing proper value of C_{fb}, W/L and load of PPS stage as claimed.

3.7 Proposed design-II

The design-I has following shortcomings: (i) improper selection of initial parameters, (ii) the bias voltage and Q_{in} decides the width of transistor M_1 but not the gain, (iii) the condition $C_{ex} > 4C_{gs}$ can be avoided and (iv) it has a severe problem of both noise and signal leakage from stage-I to II and vice-versa. An improved design flow has been proposed to overcome these shortcomings as shown in Figure 3.12. The design flow starts with load tank of IDCS stage and then calculation of circuit elements L_{deg}, L_g and width (W) of M_1. The modifications in the enhanced design flow are highlighted with red color. The selection of noise factor (Nf), Q_{in} and bias voltage (V_{BIAS}) determines the C_{ex} and C_{gs}. The calculation of overall gain avoids multiple iterations since it depends on W, C_{ex} and load tank. The noise figure (NF) calculation is placed after simulation to avoid its calculation at each iteration.

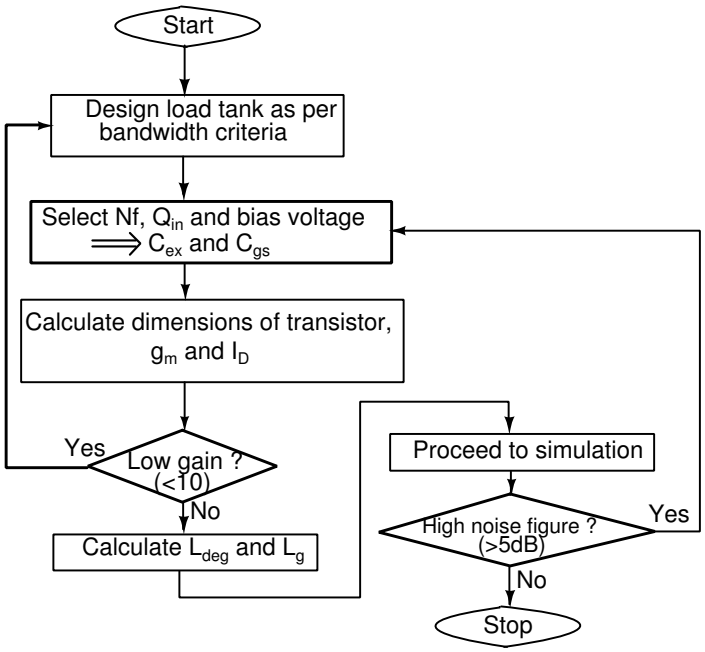


Figure 3.12: Enhanced design flow of sub-threshold IDCS topology (stage-I) (modifications are highlighted).

A cascaded common source stage (stage-II) is stacked on top of the IDCS stage (stage-I) to convert incoming single-ended antenna signal into differential signal. The balun LNA reported in Section 3.6 gives the immense performance if the impedance seen from node S to down is very high. But, practically this is very difficult since the

quality factor of on-chip inductor (L_{d1}) is not more than 15. Moreover, this lower impedance confess the signal into the stage-II. This leakage is the fountainhead for poor noise performance and imbalance at differential output. So, an improved circuit has been proposed for balun LNA to mitigate the above mentioned issues of design-I. The design-II of balun LNA is shown in Figure 3.13a.

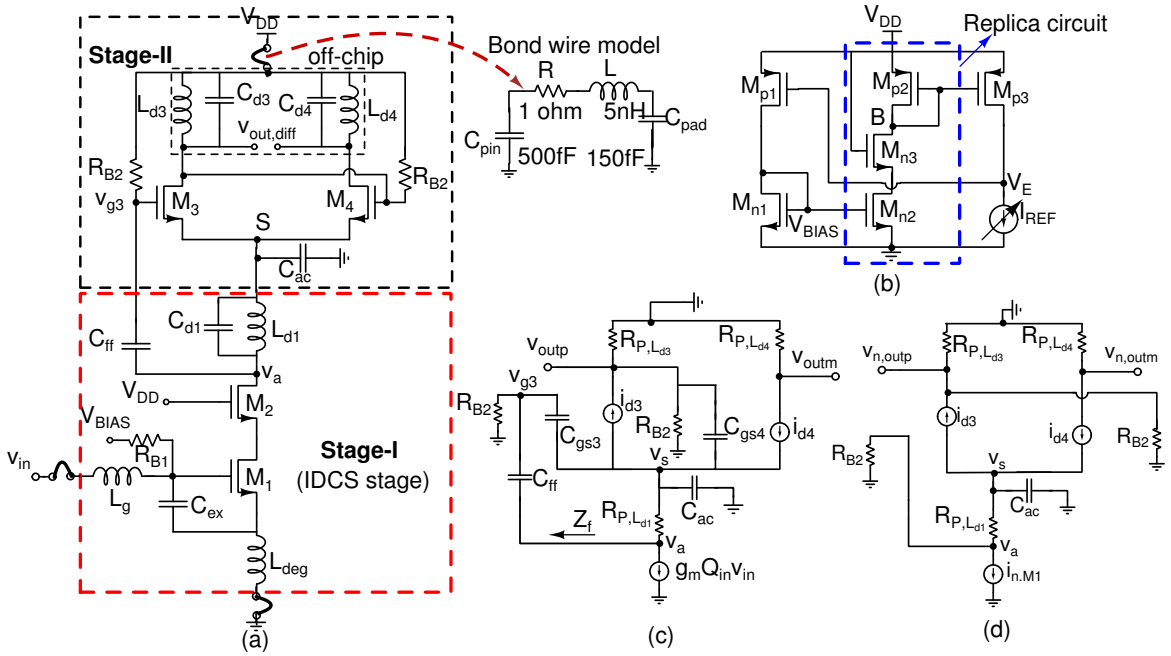


Figure 3.13: (a) Proposed sub-threshold balun LNA (b) PVT compensated bias circuit (c) Small signal equivalent circuit at resonance (403 MHz) (d) Simplified noise equivalent circuit at 403 MHz (only M_1 noise is shown).

The output of stage-I is fed into the stage-II through C_{ff}. An additional capacitor C_{ac} is used at node S to improve both noise performance and imbalance error at the output of stage-II. The capacitor C_{ac} provides small signal ground after 300 MHz of input frequency and avoids both noise and signal leakage. The large value of the C_{ac} has better attenuation of noise and signal leakage from stage-I to stage-II. The load of both stages are designed with LC tank to achieve high gain and narrow bandwidth. This arrangement enhances the roll-off rate in the outside band. Thus selectivity of the LNA increases. In conventional, LNA is preceded by convoluted high-Q filter to remove out-of-band signals. But, the high selectivity of proposed LNA makes it attractive to design cost-effective RF front-end with low-Q band selection filter. Moreover the proposed LNA gives the provision to avoid the use of image rejection filter in the front-end of MedRadio.

Also, a PVT compensated bias circuit is designed to minimize the variations in LNA parameters. Bias circuit comprises of negative feedback and charge pump to track the PVT variations in the balun LNA. Figure 3.13b shows the biasing circuit. A replica circuit is designed in the bias compensation circuit to avoid the involvement of actual balun LNA. The transistors M_{n2} and M_{n3} are considered to design replica circuit. The transistor M_{p2} is considered as the load, to set required voltage at node B and mirror the current into M_{p3}. The transistor M_{p3} scales down the current of replica circuit and compares the reference current (I_{REF}). The difference of current in M_{p3} and reference source will generate error voltage (V_E). The transistor M_{p1} acts as a variable current source according to the error voltage. It can be seen that the proposed bias circuit will not give complete compensation against PVT since the variations in $|V_{DS_{p2}}|$ of M_{p2} are not exactly equal to that of actual LNA. But, it has been observed that the PVT variations are reduced by 55% as compared to conventional biasing. An external variable current reference (I_{REF}) has been used to control the variations in gain against inductor and capacitor corners (since passive amplification of LNA is sensitive to L_{deg}, L_g and C_{ex} variations). The error voltage V_E tunes the V_{BIAS} according to the variations in LNA. The quad flat no-lead (QFN) package model is used at each pin to resemble the practical scenario.

3.7.1 Gain analysis

The small signal equivalent of balun LNA is shown in Figure 3.13c. The analysis of gain and noise figure are carried out with the following assumptions.

Assumptions:

1. The small signal voltage at node $v_s \simeq 0$ after 300 MHz.
2. $\dfrac{1}{|sC_{gs3}|} \gg R_{B2}$
3. $\dfrac{1}{|sC_{ff}|} \ll R_{B2}$

From the above assumptions it can be concluded that

$$|Z_f| \simeq R_{B2} \tag{3.25}$$

4. $|Z_f| \gg R_{P,L_{d1}}$, since $R_{B2} \gg R_{P,L_{d1}}$, where $R_{P,L_{d1}}$ is equivalent parallel resistance of L_{d1}.

The input matching network provides passive amplification for the incoming RF signal

by Q_{in} times. The gate to source voltage of M_1 is given by

$$v_{gs,M_1} = \frac{v_{in}}{2\,R_S\omega_0 C_t} = Q_{in}v_{in} \tag{3.26}$$

The output voltage at the first stage is given by

$$v_a = -g_m Q_{in} R_{P,L_{d1}} v_{in} \qquad (\text{since } |Z_f| \gg R_{P,L_{d1}}) \tag{3.27}$$

From the assumptions, the gate voltage of M_3 is,

$$v_{g3} \simeq v_a (\text{since } R_{B2} \gg 1/|sC_{ff}| \text{ and } R_{B2} < 1/|sC_{gs3}|) \tag{3.28}$$

Now the output voltages are given by (3.29) and (3.30).

$$v_{outp} = i_{d3} R_{P,L_{d3}} \tag{3.29}$$

$$v_{outm} = -g_{m4} v_{outp} R_{P,L_{d4}} \tag{3.30}$$

The necessary condition for gain and phase balance at differential output is

$$v_{outm} = -v_{outp} \tag{3.31}$$

$$v_{outm} = -g_{m4} v_{outp} R_{P,L_{d4}} = -v_{outp} \tag{3.32}$$

Hence from (3.32), the condition for balanced output is

$$g_{m4} R_{P,L_{d4}} = 1 \tag{3.33}$$

3.7.2 Effect of C_{ac} on noise figure

The selection of C_{ac} has vital impact on the noise figure of balun LNA. The value of C_{ac} should be sufficiently large to reduce the noise leakage from load of stage-I to stage-II. A detailed analysis is given to validate the above statement. The simplified noise equivalent circuit is shown in Figure 3.13d. In the equivalent circuit, only the noise of M_1 is considered to analyze the impact of C_{ac}. The noise current of M_1 (i_{n,M_1}) is given by

$$i_{n,M_1} = \frac{v_a}{R_{B2}} + \frac{v_a - v_s}{R_{P,L_{d1}}} \tag{3.34}$$

From (3.34), we have

$$i_{n,M_1} R_{B2} R_{P,L_{d1}} = v_a R_{P,L_{d1}} + (v_a - v_s) R_{B2} \tag{3.35}$$

$$\Rightarrow v_s = \frac{v_a(R_{P,L_{d1}} + R_{B2}) - i_{n,M_1} R_{B2} R_{P,L_{d1}}}{R_{B2}} \tag{3.36}$$

Now, the final expression of v_a and v_s are given by (3.37) and (3.38) as derived in Appendix A-1.

$$v_a = \frac{i_{n,M_1} R_{B2} R_{P,L_{d1}}.y}{(R_{P,L_{d1}} + R_{B2})y - R_{B2}x} \tag{3.37}$$

$$v_s = \frac{\frac{i_{n,M_1} R_{B2} R_{P,L_{d1}} (R_{P,L_{d1}} + R_{B2})y}{(R_{P,L_{d1}} + R_{B2})y - R_{B2}x} - i_{n,M_1} R_{B2} R_{P,L_{d1}}}{R_{B2}} \tag{3.38}$$

where $x = g_{m3} + \dfrac{1}{R_{P,L_{d1}}} - g_{m3} g_{m4} R_{P,L_{d3}}$ and $y = g_{m4} + sC_{ac} + x$. In (3.38), we can observe the impact of C_{ac} on the noise figure. At higher values of C_{ac}, the value of $(R_{P,L_{d1}} + R_{B2})y$ becomes much higher than $R_{B2}x$. This condition makes the node v_s to approximately zero, which reduces the noise at both the outputs. So, the necessary condition for choosing the capacitor (C_{ac}) value is

$$(R_{P,L_{d1}} + R_{B2})y \gg R_{B2}x \tag{3.39}$$

Now, noise at the output can be written as

$$v_{n,outp} = -g_{m3} i_{n,M_1} (\frac{1}{R_{B2}} + \frac{1}{R_{P,L_{d1}}}) R_{P,L_{d3}} \tag{3.40}$$

$$v_{n,outm} = g_{m4} g_{m3} i_{n,M_1} (\frac{1}{R_{B2}} + \frac{1}{R_{P,L_{d1}}}) R_{P,L_{d3}} R_{P,L_{d4}} \tag{3.41}$$

The variations of noise figure for different values of capacitor (C_{ac}) are shown in Figure 3.14. The noise figure is very high in the absence of C_{ac}. The analysis shows that the higher value of C_{ac} (15 pF) has an improvement in NF by 1.3 dB as compared to noise figure (i.e.,4.4 dB) of design-I. The W/L ratio of transistors and values of other components are calculated to meet the target specifications and assumptions. The values of all components are enlisted in Table 3.2.

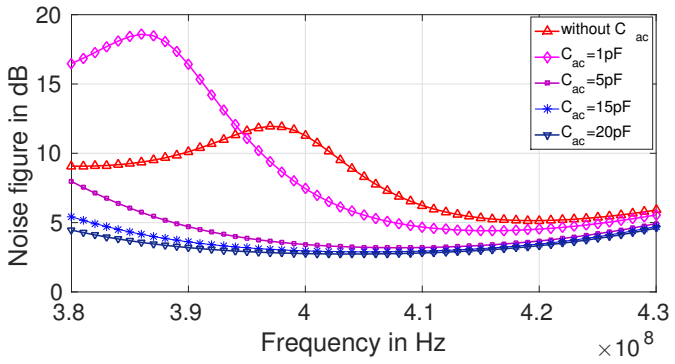


Figure 3.14: Variation in noise figure against C_{ac} (post-layout).

Table 3.2: Component values of proposed balun LNA.

Component	Value	Component	Value
L_{deg}	4 nH	M_1(W/L)	415 μm/0.18 μm
L_{d1}	11.6 nH	M_2(W/L)	205 μm/0.18 μm
L_{d3}	13 nH	$M_{3,4}$(W/L)	250 μm/0.18 μm
L_{d4}	10 nH	R_{B1}	30 kΩ
$L_g(Q)$	100 nH(15)	R_{B2}	10 kΩ
C_{d1}	12 pF	C_{ex}	310 fF
C_{d3}	10.1 pF	C_{ff}	2 pF
C_{d4}	14.1 pF	C_{ac}	15 pF

3.8 Post-layout simulation results

The proposed balun LNA is implemented in UMC 0.18-μm CMOS technology. The layout of LNA is shown in Figure 3.15a. The area including test buffers and biasing is 850 μm $\times$ 978 μm. The layout is optimized for minimum routing resistance. The routing resistance becomes crucial at the load of first stage, since the quality factor of L_{d1} is sensitive to its routing resistance. The large values of inductor restricts the shortest routing. The routing resistance has been reduced by stacking metal 6 and 5 with vias in between. This technique has given decrement in routing resistance by 70%. But, we cannot reduce it further by stacking other metals, since it causes deviation in the resonance frequency. Figure 3.15b shows the frequency response of proposed balun LNA. The out-of-band roll-off rate is 70 dB/dec, which is comparable with the characteristics of high-Q filter. So, a low Q cost-effective BSF filter is adequate before the proposed balun LNA. The linearity of balun LNA is validated by calculating third order input intercept point (IIP_3). Figure 3.15c shows the IIP_3 of proposed LNA is –27.5 dBm.

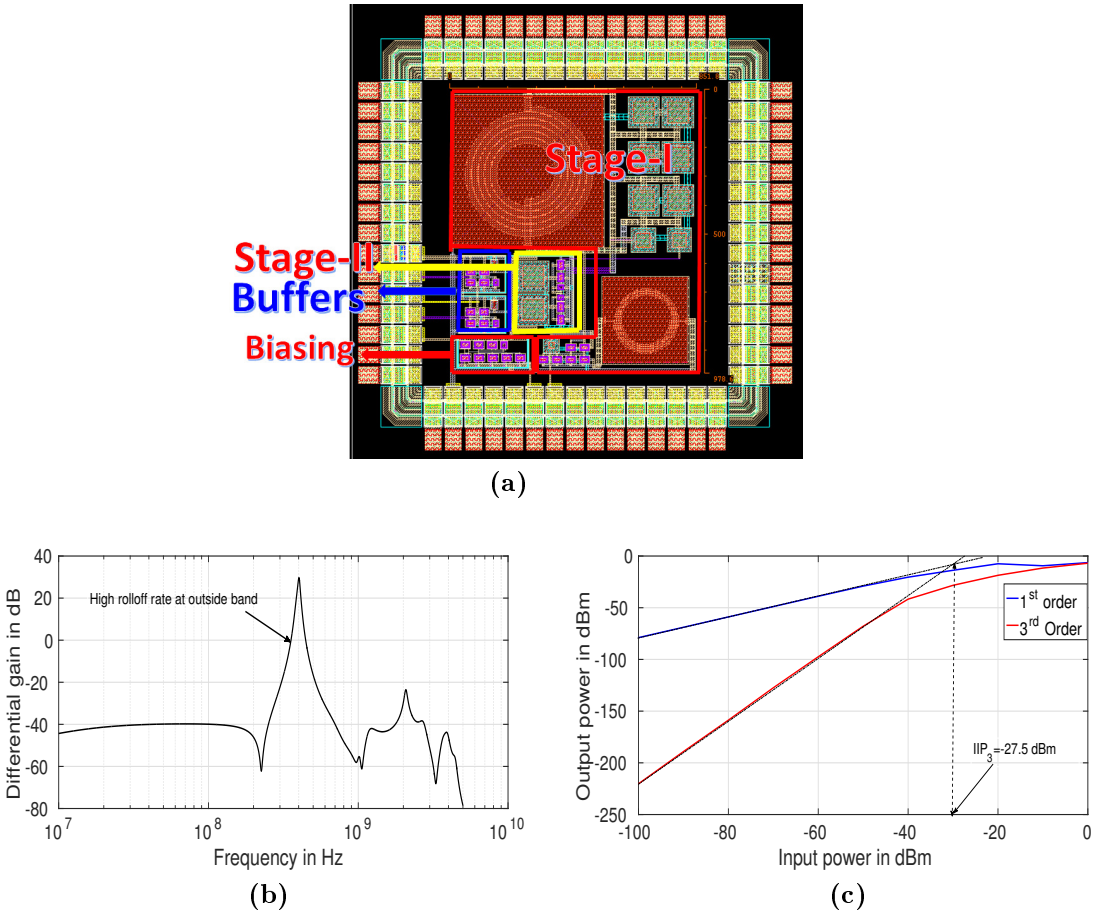


Figure 3.15: (a) Layout of proposed balun LNA including biasing circuit and test buffers (pad frame size is 1 mm×1 mm) (b) Frequency response of proposed LNA (High roll-off rate is marked with arrow) (c) Calculation of third order input intercept point (IIP_3) at 403 MHz (Post-layout).

Figure 3.16 shows the test set-up used to measure the S-parameters of single to differential LNA. Two additional buffers have been used at the output of LNA to match the 50 Ω port. A passive network can also be used instead of buffer, but the on-chip advantage of buffer makes it attractive and keeps the measurement process simple. However, the additional buffer leads to attenuation in power gain by 3 to 4 dB.

From Figure 3.17a it can be seen that the power gain is 23 dB, input and output reverse isolation is less than –12 dB. Figure 3.17b shows that the noise figure at the band of interest is 3.1 dB. The gain and phase errors are tuned to possible minimum values using the load of M_3, M_4 and capacitor C_{ac}. The maximum gain and phase error is 0.8 dB and 10° respectively. Figure 3.17c and 3.17d shows the gain and phase

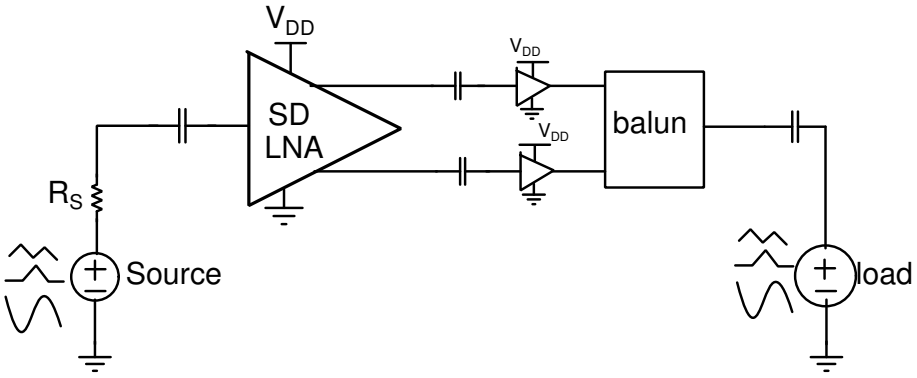
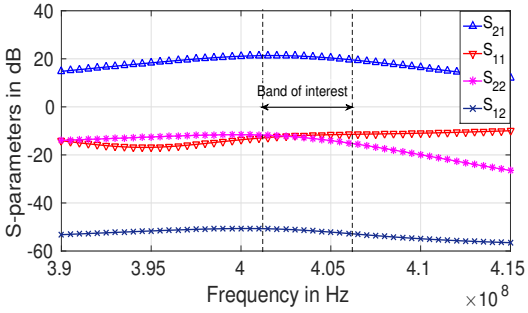
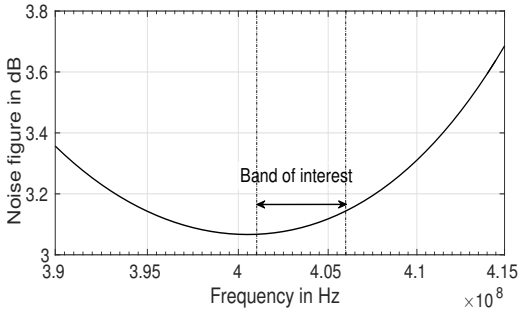


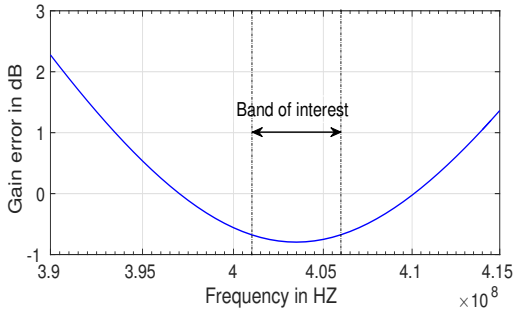
Figure 3.16: Test bench set-up for S-parameter measurement.



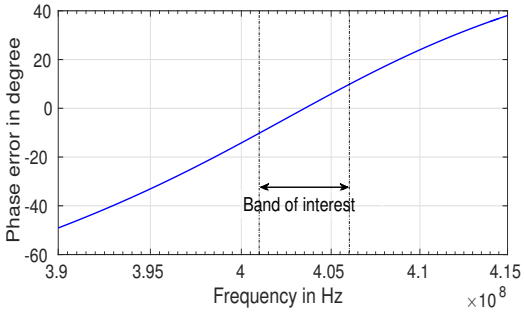
(a) Analysis of S-parameters



(b) Noise figure



(c) Gain error



(d) Phase error

Figure 3.17: Post-layout simulations of proposed balun LNA (including buffers at the output).

error against input signal frequency. Table 3.3 summaries the post-layout simulations of the proposed MedRadio balun LNA and compares to that of other related published works. Honorable comparison has been done using figure of merit (FoM_1) (Choi *et al.* (2016)). The FoM_2 is defined to include gain and phase errors. The units of FoM_1 and

Table 3.3: Performance comparison of Low Noise Amplifier (MedRadio).

Work	Technology (μm)	Frequency (MHz)	Voltage Gain (dB)	Noise Figure (dB)	Power dissipation (mW)	IIP_3 (dBm)	Gain(dB)& Phase(degree) error	Additional balun	FoM_1	FoM_2
Cha *et al.* (2011) MTT'11(Measured)	0.18	401-406	20.2	2.8	0.15	-8.1	N/A	Yes	3.4^{a}	N/A
Martins *et al.* (2011) ISCAS'11(Post-layout)	0.13	2400	30	2.6	3.6	- 19	2 & 10	Yes	0.1	8.3 m at 2.4 GHz
Dehghani and Abouei (2013) EL'13 (Pre-layout)	0.36	401-406	23	3.7	3.59	-18	N/A	Yes	0.017	N/A
Cruz *et al.* (2015) TCAS-I'15 (Measured)	0.18	402-405	10	10	0.94	-16	N/R	Yes	0.012	N/R
Mohamed and Sherif (2013) TCAS-I'13 (Measured)	0.13	402-405	31	13.6	2.7	3	N/R	Yes	$2.46^{a,b}$	N/R
Wu *et al.* (2011) TCAS-II'11 (Measured)	0.18	1500	18.75	2.52	1.926	-19.86	0.4 & 3.32	No	0.068	20.5 m at 1.5 GHz
Choi *et al.* (2016) MWC'16 (Measured)	0.18	401-457	29	5	0.37	-19.5	N/R	Yes	$0.25^{a,b}$	N/R
Proposed (Post-layout)	0.18	401-406	31	3.1^{c}	0.29	-27.5	0.8 & 10	No	0.08	38.5 m at 403 MHz
[a] Additional balun consumes more area, power and degrades FoM [b] RF front-end (LNA+mixer) N/A= Not Applicable N/R= Not Reported [c] Including buffer noise m-Milli										

FoM_2 are GHz and GHz/degree respectively. As some of the references given power gain and others voltage gain, an absolute gain has been taken in FoM calculation. The mathematical expression of FoM_1 and FoM_2 is given by

$$FoM_1 = \frac{Gain[abs] \times IIP_3[mW] \times f[GHz]}{P_{DC}[mW] \times (NF-1)[abs]} \tag{3.42}$$

$$FoM_2 = \frac{Gain[abs] \times IIP_3[mW]}{P_{DC}[mW] \times (NF-1)[abs]} \times \frac{f[GHz]}{gain\ error[dB] \times phase\ error[degree]} \tag{3.43}$$

Absolute gain of amplifier is expressed as

$$Absolute\ gain = 10^{VG/20} = 10^{PG/10} \tag{3.44}$$

where VG and PG are voltage gain and power gain in dB. Higher values of FoM gives the better performance. The FoM_1 of proposed balun LNA is 0.08. The FoM_1 of Cha *et al.* (2011) is high (almost 100 times that of the proposed design) because of IIP_3. Suppose the linearity of proposed design is –8 dBm, then FoM_1 is observed to be much better (3 times) than Cha *et al.* (2011). However, IIP_3 requirement of MedRadio (which is more than –30 dBm) and other advantages (i.e., SD conversion and low power) of proposed design makes it competitive when compared to other reported LNAs. The FoM_2 of proposed design is observed to be almost five times as compared to the existing balun designs.

3.9 Summary

In this work, a high selectivity sub-threshold balun low noise amplifier is designed for low power wearable and implantable medical devices. The proposed LNA uses current re-use technique to stack cascaded common source stage on top of the IDCS stage. A sub-threshold IDCS stage is designed to match the input impedance (50 Ω) at optimum noise and power without compromising other LNA parameters. An improved design flow has been proposed to avoid multiple iterations in the design of IDCS stage. The additional capacitor C_{ac} is used to provide small signal ground between two stages. Analysis show that higher value of C_{ac} reduces the noise leakage from stage-I to stage-II. The proposed LNA has good out-off band rejection, since there are two load tank between input and output. After dedicated sizing and bias optimization, the LNA is designed in UMC 0.18-μm CMOS technology. The layout of proposed LNA occupies 850 μm × 978 μm including buffers and bias circuit.

The post-layout results show the differential gain of 31 dB, noise figure of 3.1 dB and IIP_3 of –27.5 dBm while consuming DC current of 290 μA from 1 V supply. The proposed LNA is distinguished from the performance over the process corners and temperature range from 0°C to 80°C. The worst case gain and phase error is observed to be 0.8 dB and 10° respectively.

Chapter 4

LOW POWER UWB BALUN LNA

4.1 Introduction

The Federal Communications Commission (FCC) has allocated 7.5 GHz bandwidth for UWB applications in the frequency range of 3.1 to 10.6 GHz (Lu *et al.* (2006)), which is divided in to 14 sub-bands with a band-width of 528 MHz each as shown in Figure 4.1. These sub-bands are arranged as five band-groups.

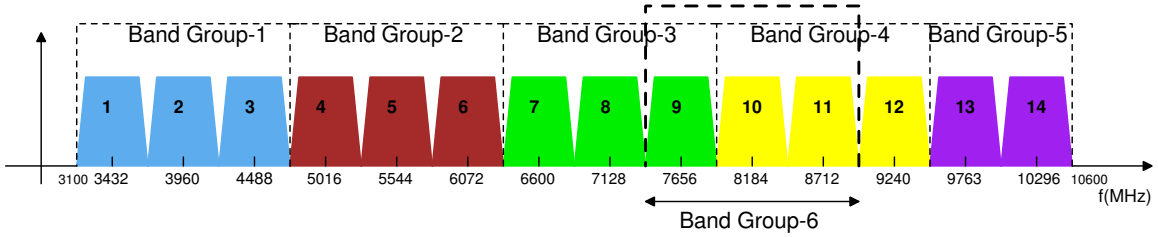


Figure 4.1: Spectrum division of UWB.

In any UWB system the first group must be covered, while the other groups are optional. The second group is completely occupied by wireless local area network (WLAN) communication system, so it is always ignored. Owing to stipulations made by government for military or other special agencies in different countries, the other sub-bands accommodated in third, fourth, and fifth groups are selected for use by UWB companies in different ways. It is found that the sub-bands 9, 10, and 11 are having fewer restrictions in the wireless market, so a new sixth group is identified. Currently, the first and sixth groups became focal point for most UWB companies and enterprises. In all types of UWB receivers the first amplifying block is low noise

amplifier (LNA), which is one of the pre-eminent stage to sense all range of signals at low power (Commission (2002), Porcino and Hirt (2003)). The UWB technology became very popular in all types of applications, since (i) extremely difficult to detect by unintended users, (ii) appears as a noise to other communication systems and (iii) common architecture for global positioning, radar and short distance communication. The main advantage of UWB technology can be comprehended by Shannon's channel capacity theorem given as

$$C = B \log_2(1 + SNR) \tag{4.1}$$

where C is the channel capacity in bits per second. A channel capacity grows linearly with bandwidth (B) but logarithmically with SNR. In other words, the channel capacity can be increased by increasing the bandwidth than the SNR. Another advantage is, low power is sufficient to transfer the same amount of data. Further, the channel fading effect in UWB systems is less when compared to narrow-band systems because high temporal resolution helps to distinguish extremely short pulses propagating over different paths (Wang (2005)). UWB has many potential applications like high data rate WPAN, indoor localization, medical applications and many other.

There are many design challenges in low noise amplifier since it is responsible for entire receiver performance. As per the UWB wireless standards LNA should sense all types of signals in wide-band at optimum noise, gain and power. In UWB applications, the main challenges in the design of LNA are: (i) wide-band impedance matching (ii) bandwidth extension at low power (iii) flat gain and good linearity and (iv) suppress the effect of narrow-band jammers i.e., interference from existing radio systems. In addition, phase and gain imbalance between the outputs should be minimum, otherwise it will degrade the SNR performance.

4.2 Specifications of UWB

UWB differs substantially from conventional narrow-band radio frequency (RF) and spread spectrum technologies, such as bluetooth technology and 802.11a/g. In a given period of time the transmission of data in UWB is more, since it uses an extremely wide band of RF spectrum.

The maximum radiated power from UWB transmitter is restricted to –41.3 dBm/MHz. The free space path loss over a distance of 10 m is –44 dBm (Pahlavan and Krishnamurthy (2013)). The maximum received power at the receiver is -86 dBm/MHz. The

target specifications of LNA for UWB applications are as follows:

- Frequency range (GHz) : 3.1 - 10.6
- Gain : $>10\,\mathrm{dB}$
- Gain difference : $<1\,\mathrm{dB}$ and Phase difference : $<10^{\circ}$
- NF : $<5\,\mathrm{dB}$
- IIP_3 : $>-15\,\mathrm{dBm}$
- S_{11} : $<-10\,\mathrm{dB}$
- Power dissipation : $<10\,\mathrm{mW}$

4.3 Prior work

Many wide-band LNA techniques have been matured in the literature (Yu *et al.* (2006), Huang *et al.* (2015), He *et al.* (2010), Alavi-Rad *et al.* (2013)). However, there are still some deterrents among them. For example, two stage LNA architectures and the conventional distributed amplifier suffers from high power consumption (Yu *et al.* (2006)). The inductively degenerated topology with active/passive element in the feedback is a well known technique used in wide-band amplifiers (Huang *et al.* (2015), He *et al.* (2010)), but it is hard to convince gain and noise requirements simultaneously. But all these techniques have used minimum two stages to achieve UWB requirements at the cost of power and area (since it requires additional balun to convert single-ended signal to differential) . In literature considerable research has been conducted on a range of LNA design for UWB applications, however the research is heavily biased towards the single-ended design. But, the design of SD LNA has not been experienced the same attention. There are very few single to differential LNAs have been developed by Blaakmeer *et al.* (2008*a*), Martins *et al.* (2011), Kim and Silva-Martinez (2012). The CG-CS noise cancellation technique is one of the familiar architecture which does single to differential conversion at low noise, but this technique is suffering from lower band-width.

A direct conversion receiver is most preferable choice for constructing wide-band receiver. However, a double balanced mixer is indispensable to avoid LO leakage and

even order distortion. So, a fully-differential signal should be required at the output of LNA. A simple way to design single to differential LNA is parallel connection of CG and CS stages as shown in Figure 4.2. The primary advantages of CG-CS topology

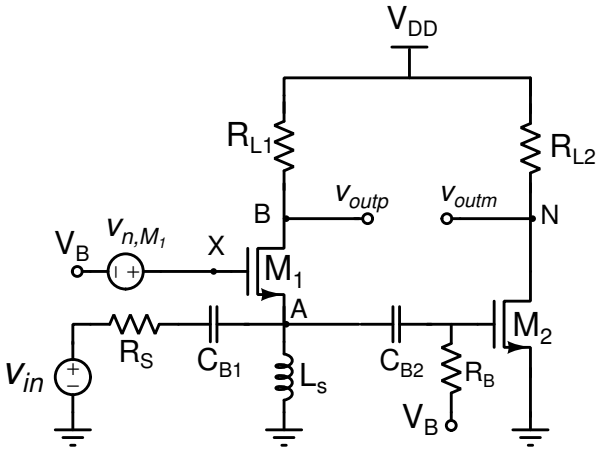


Figure 4.2: CG-CS single-differential LNA.

are: (i) The input transistor (M_1) provides the input matching and amplifies the input signal without any phase difference (since it is a common gate transistor), on the other hand M_2 (connected in common source) also amplifies the input signal and provides 180^0 phase shift. (ii) The noise of input transistor (i.e.,v_{n,M_1}) cancels by M_2. The circuit follows the noise cancellation principle because (a) the noise of M_1 sees a source follower and common source path to node A and B respectively, evincing opposite polarities at these two nodes, and (b) the signal sees a common-gate path through A and B, evincing same polarity. Transistor M_1 produces half of its noise voltage at A if the input is matched. Transistor M_2 senses this noise and amplifies it by a factor of $-g_{m2}R_{L2}$. The condition for noise cancellation is given as

$$R_{L1} = g_{m2}R_{L2}R_s \tag{4.2}$$

Nevertheless the noise of M_1 is cancelled, the noise arises from M_2, R_{L1} and R_{L2}. The principle advantage of CG-CS noise cancellation technique is that it affords broadband characteristics. It is consequently benefited to systems operating across a wide frequency.

Low power full band LNAs have been proposed using CS/CG topology with negative feedback as shown in Figure 4.3 (He *et al.* (2010), Weng *et al.* (2010)). Figure 4.3a

shows a full band LNA uses staggered tuning and current re-use techniques to extend bandwidth at low power consumption. The CG topology provides wide band impedance matching. However, the trade-off between NF and gain is the major issue of this technique. Figure 4.3b shows a two stage inductive degeneration CS topology with resistance-capacitance (RC) shunt feedback. Though it is good at bandwidth and noise figure, the power consumption is 15 mW. In addition, an additional balun is required for both the techniques to convert single-ended incoming signal. There are some fully differential LNAs for UWB applications (Bevilacqua *et al.* (2006), Khurram and Hasan (2013)). The problem with fully-differential LNA is that, it must be preceded by balun whose noise contribution directly hits the entire receiver NF. Even though the NF is not a major concern of receiver, the additional balun causes for phase and gain imbalance (Martins *et al.* (2011)).

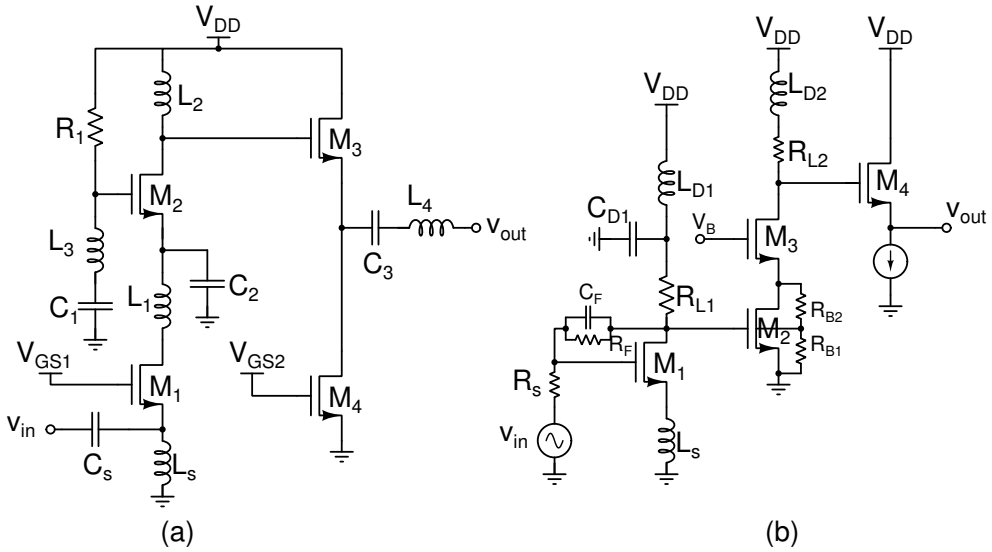


Figure 4.3: Single-ended UWB LNA (a) Full band LNA using staggered tuning and current re-use techniques (b) IDCS LNA using parallel RC feedback.

A single to differential LNA would be the better option to implement wide-band receiver. An improved CG-CS LNA has been proposed by Blaakmeer *et al.* (2008*b*) as shown in Figure 4.4. It exploits noise and distortion cancellation of common-gate (CG) stage and common-source (CS) stage with transconductance scaling. This technique avoids the use of balun and provides good linearity. However, the power consumption is high (i.e.,14 mW) and should be reduced to meet specifications of UWB. Further, the resistive load restricts the bandwidth upto 4 GHz. So, the stumbling balun and low

bandwidth of traditional CG-CS topology motivated us to develop a new methodology of low power LNA to cover first and sixth groups with minimum phase and gain error.

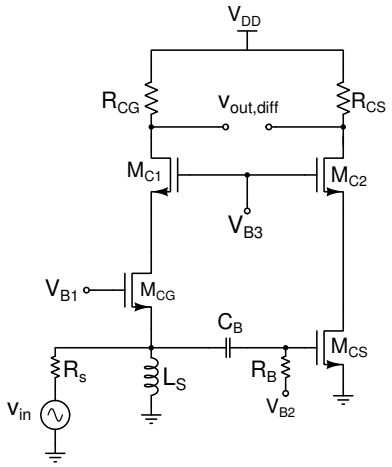


Figure 4.4: CG-CS balun LNA with cascode transistors.

4.4 Basic idea

In this chapter an alternate topology of SD LNA is proposed. The block diagram of LNA is shown in Figure 4.5.

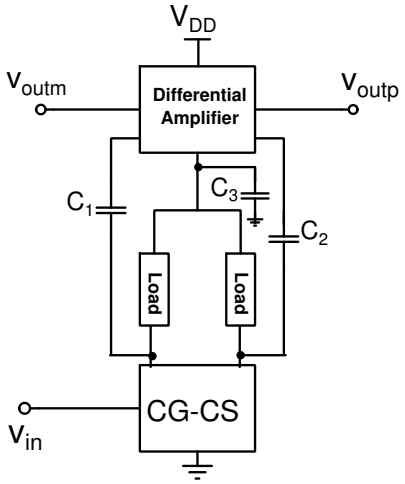


Figure 4.5: Block diagram of proposed balun LNA for UWB applications.

The proposed balun LNA uses both noise cancellation and current re-use techniques to resolve issues of UWB front-end (explained in section 1.3). A single to

differential conversion is done by the first stage (i.e.,CG-CS) and a differential amplifier is stacked on top of the CG-CS stage to expand the bandwidth. The idea behind proposed technique is staggered tuning, where first and second stage oscillates at different frequencies. The basic idea behind the proposed bandwidth extension is, the first stage resonates at lower frequency of the desired band and second stage at higher frequency. The full band frequency response of proposed LNA is shown in Figure 4.6. The low power consumption and single to differential conversion of proposed LNA

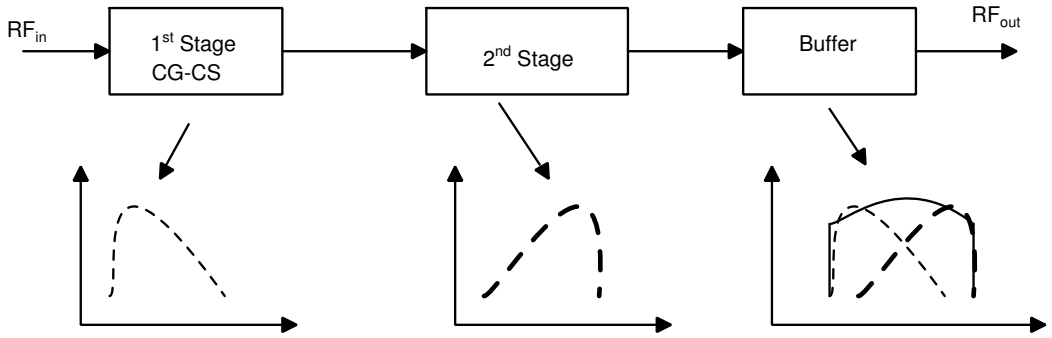


Figure 4.6: Full-band frequency response of proposed LNA using noise cancellation and staggered tuning technique.

solves the issues of wide-band front-end. The noise of CG transistor get cancels by CS transistor and no additional power is used for bandwidth extension. The block diagram of UWB receiver with the proposed LNA is shown in Figure 4.7. In DCR receivers, the phase error between in-phase and quadrature components should not be high.

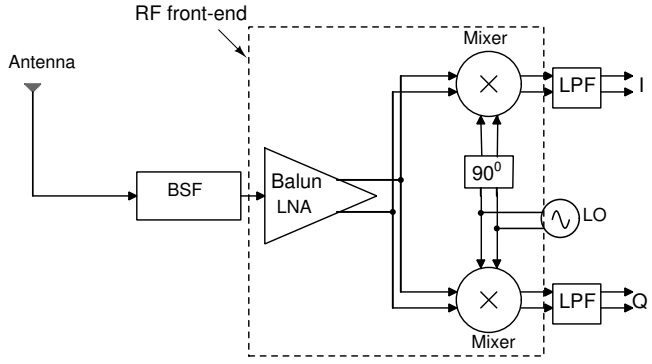


Figure 4.7: UWB receiver with proposed balun LNA.

4.5 Proposed UWB LNA

Most of the existing designs are either inevitably comply with additional feedback and balun network, or consume relatively high power, which is not worthy for low power applications. Further, the NF and bandwidth needs to be improved to meet specifications of UWB. Hence, a compact, simple and sturdy topology of UWB LNA is proposed, which provides single to differential conversion at very low power (i.e.,below 5 mW) and NF (i.e.,below 4 dB). A single integrated circuit amalgamating the balun and LNA functionality seems an attractive option to perceive a wide-band low-noise receiver front-end. In MOSFET characteristics, assumption of square law behavior is highly inaccurate for sub-micron devices. The issue of velocity saturation causes for high power consumption. In this region of operation g_m is no longer function of V_{GS}, higher V_{GS} causes for increase in I_D but little variation in g_m. So, a careful investigation has been done on the selection of biasing point to avoid deep saturation.

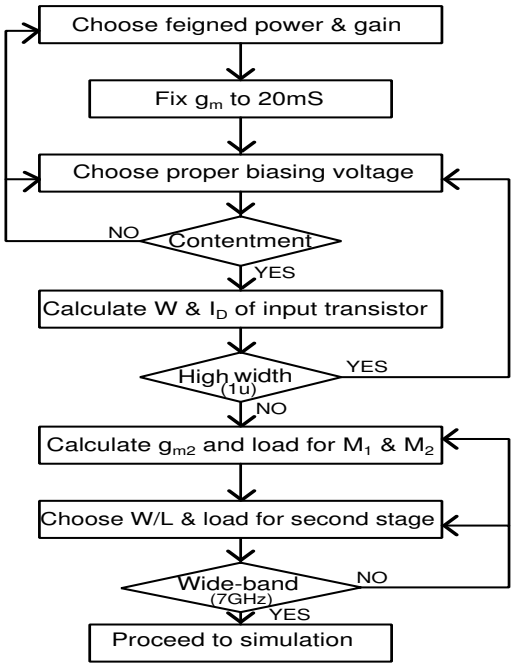


Figure 4.8: Design flow of proposed UWB-LNA.

Staggered tuning has been employed in the proposed technique by stacking a differential amplifier (stage-II) on top of the CG-CS (stage-I) topology. The stage-I and II are tuned to 4 GHz and 7 GHz respectively so that a wide band is covered. The proposed

LNA comprises of CG-CS topology and a differential configuration. The second stage splits the single-ended signal into differential at minimum gain and phase error. A complete design flow is given to avoid multiple iterations in the proposed LNA as shown in Figure 4.8.

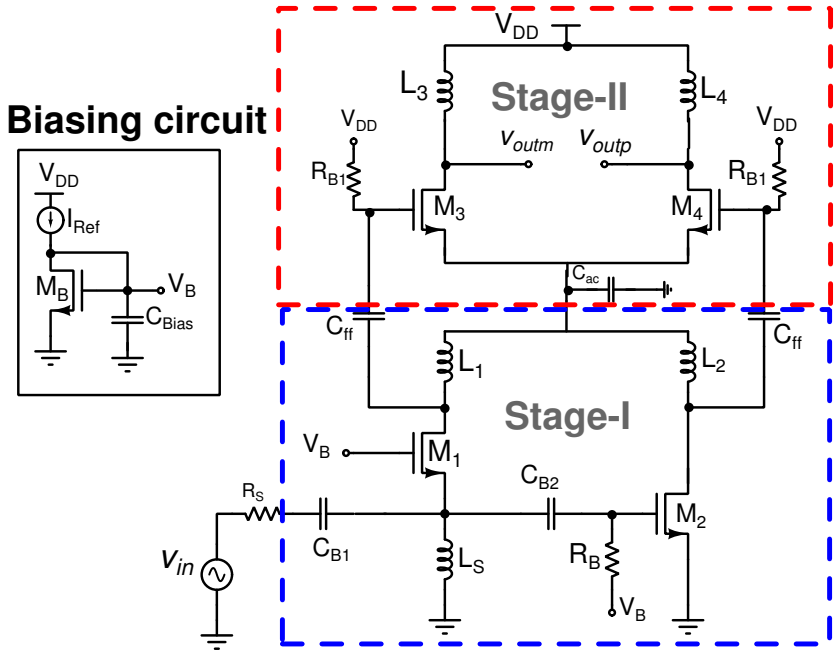


Figure 4.9: Proposed UWB-LNA using noise cancellation and current re-use techniques.

The circuit diagram of the proposed balun LNA using noise cancellation and current re-use techniques is shown in Figure 4.9. The fine tuning has been done by varying (W/L) ratio, g_m and load resistance of M_1 & M_2 to achieve gain and phase balance between two outputs of CG-CS stage. The output of first stage is applied to gate of M_3 & M_4 through the capacitor C_{ff}. The capacitor C_{ac} provides the small signal path to the second stage. Nevertheless, the proposed method looks like a cascode topology, it is cascaded connection of stage-I and II.

4.5.1 Gain analysis

The small signal equivalent of proposed balun LNA for UWB applications is shown in Figure 4.10. The channel length modulation has been neglected and following assumptions are made for contended gain analysis of proposed SD LNA.

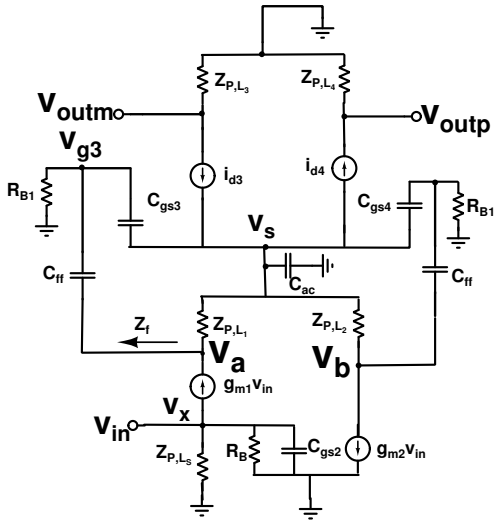


Figure 4.10: Small signal analysis of proposed balun LNA.

Assumptions:

1. $v_s \simeq 0$ after 900 MHz
2. $\dfrac{1}{|sC_{gs3}|} \gg R_{B1}$
3. $\dfrac{1}{|sC_{ff}|} \ll R_{B1}$

So from these assumptions the final conclusion is $|Z_f| \simeq R_{B1}$

4. $|Z_f| \gg |Z_{P,L_1}|$ i.e., $R_{B1} \gg |Z_{P,L_1}|$

The incoming signal from antenna gets divided by 2 at the node v_x, since the impedance seen in to the M_1 is $1/g_m$ which is equal to R_S. The impedance offered by L_S is tuned to high value so that exemplary impedance matching. The gain and phase balance between two outputs (i.e.,v_{outp} and v_{outm}) has been achieved by choosing suitable values of W/L, g_m and load. The output of first stage is connected to second stage through C_{ff}. The capacitor C_{ff} is chosen such that the ratio $\dfrac{C_{ff}}{C_{ff} + C_{gs3,4}}$ is approximately equal to 1. The capacitor C_{ac} provides small signal ground to the differential stage. Now the total output voltage is given as

$$v_{out} = v_{outp} - v_{outm} = g_{m3}(v_b Z_{P,L_4} + v_a Z_{P,L_3}) \qquad (assume\ g_{m3} = g_{m4}) \qquad (4.3)$$

So the overall gain of the proposed balun LNA is given as

$$A = \frac{v_{out}}{v_S} = g_{m1} g_{m3}(Z_{P,L_2} Z_{P,L_4} + Z_{P,L_1} Z_{P,L_3}) \qquad (assume\ g_{m1} = g_{m2}) \qquad (4.4)$$

Here Z_{P,L_1}, Z_{P,L_2}, Z_{P,L_3} and Z_{P,L_4} are frequency dependent impedances, so gain varies accordingly. At the first resonance frequency, Z_{P,L_1} and Z_{P,L_2} have maximum value and contribute high gain. Similarly, Z_{P,L_3} and Z_{P,L_4} have maximum values at second resonance frequency.

4.5.2 Noise analysis

Noise behavior of the proposed technique has been analyzed. The noise equivalent circuit is shown in Figure 4.11. The noise factor of any circuit can be calculated as (Razavi Behzad (1998))

$$Noisefactor = 1 + \frac{\overline{v_{n,out}^2}}{A^2}.\frac{1}{4kTR_S} \tag{4.5}$$

where $\overline{v_{n,out}^2}$ is output mean square noise excluding source noise. The noise of M_1 is cancelled by M_2, so the noise at v_x and v_y is given as

$$v_{n,x} = v_{n,L_1} \tag{4.6}$$

$$v_{n,y} = v_{n,L_2} + i_{n,M_2} Z_{P,L_2} \tag{4.7}$$

The noise of biasing resistors is neglected, since large values have been taken to avoid

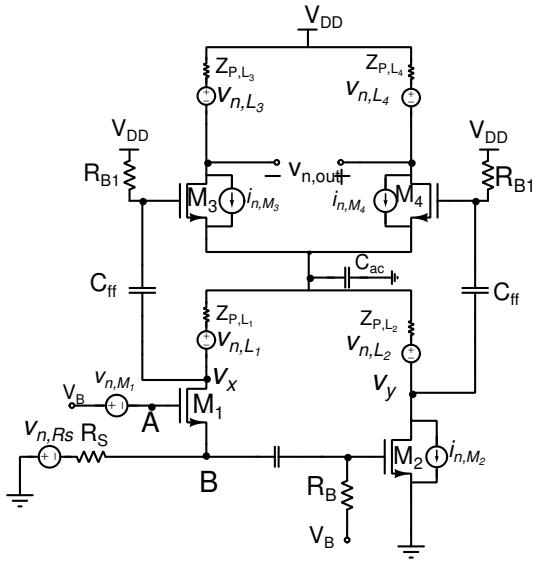


Figure 4.11: Noise equivalent circuit of balun LNA.

this. Further, the noise of stage-II is ignored to make analysis simple. The noise at v_{outp} and v_{outm} is given as

$$v_{n,outm} = g_{m3} Z_{P,L_3} v_{n,L_1} \tag{4.8}$$

$$v_{n,outp} = g_{m4} Z_{P,L_4} (v_{n,L_2} + i_{n,M_2} Z_{P,L_2}) \tag{4.9}$$

Now the overall noise can be calculated as

$$v_{n,out} = g_{m3} Z_{P,L_3} (v_{n,L_1} + v_{n,L_2} + i_{n,M_2} Z_{P,L_2}) \ (Assume\ that\ Z_{P,L_3} = Z_{P,L_4}) \tag{4.10}$$

The mean squared output noise is given as

$$\overline{v_{n,out}^2} = (g_{m3} Z_{P,L_3})^2 (4kTZ_{P,L_1} + 4kTZ_{P,L_2} + 4kT\gamma g_{m2} Z_{P,L_2}^2) \tag{4.11}$$

The noise factor of overall circuit can be calculated as

$$Noisefactor = 1 + \frac{(g_{m3} Z_{P,L_3})^2 (4kTZ_{P,L_1} + 4kTZ_{P,L_2} + 4kT\gamma g_{m2} Z_{P,L_2}^2)}{4(g_{m1} Z_{P,L_1})^2} . \frac{1}{4kTR_S} \tag{4.12}$$

Now, further simplification of noise factor is given as

$$Noisefactor = 1 + \frac{Z_{P,L_1}}{4R_S} + \frac{Z_{P,L_2}}{4R_S} + \frac{1}{4} \times \frac{\gamma g_{m2} Z_{P,L_2}^2}{R_S} \tag{4.13}$$

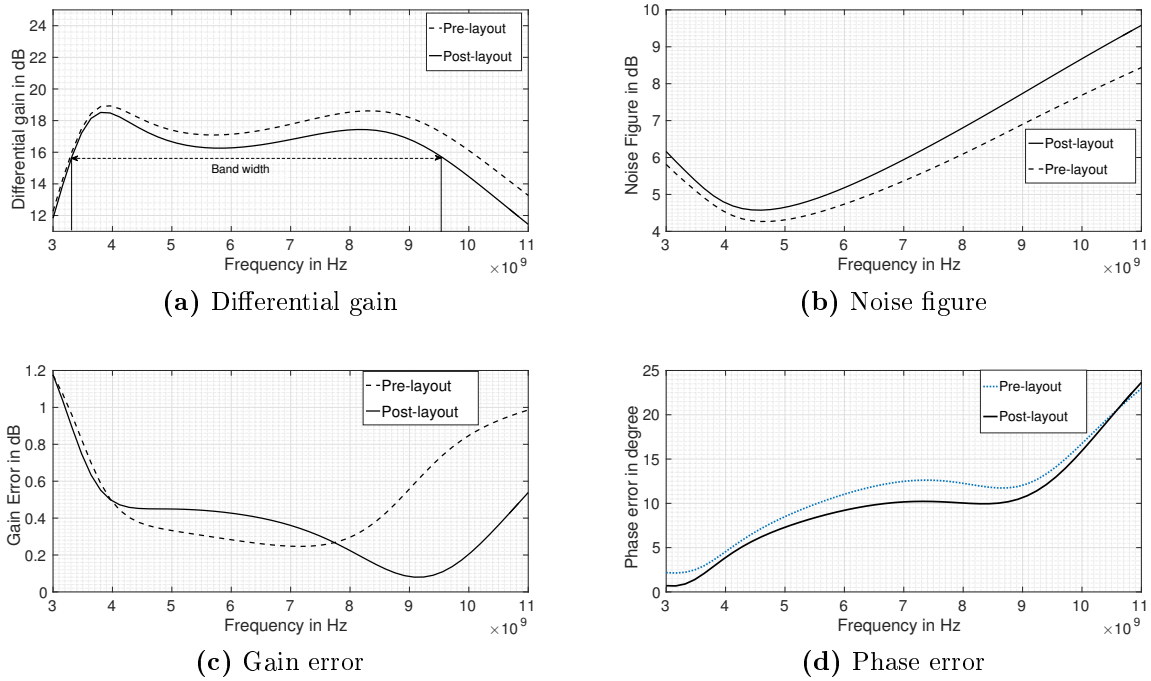
From (4.13), we can observe that the major contribution is from transistor M_2 and load resistance. The component values chosen for the proposed balun LNA are enlisted in Table 4.1.

Table 4.1: Component values chosen for proposed balun LNA.

Parameter	**Value**
L_S ($197\mu/20\mu/3.5$)	4.82 nH
L_1 ($216\mu/10\mu/3.5$)	5.342 nH
L_2 ($216\mu/10\mu/3.5$)	5.342 nH
L_3 and L_4 ($129.98\mu/20\mu/2.5$)	1.5966 nH
C_{B1} and C_{B2} ($31.47\mu/31.47\mu$)	999.8 fF
R_B	10 kΩ
C_{ff} ($31.47\mu/31.47\mu$)	999.8 fF
$(W/L)_1$ ($\mu m/\mu m$)	95/0.18
$(W/L)_2$ ($\mu m/\mu m$)	90/0.18
$(W/L)_3 = (W/L)_4$ ($\mu m/\mu m$)	90/0.18
V_{DD}	1.2 V

4.6 Post-layout results

The proposed LNA was studied in detail and optimized through careful investigation and extensive simulation using UMC 0.18-μm CMOS technology. Two output test buffers (source follower) and one balun have been used to admix the balun LNA with port (i.e., to measure S-parameters).



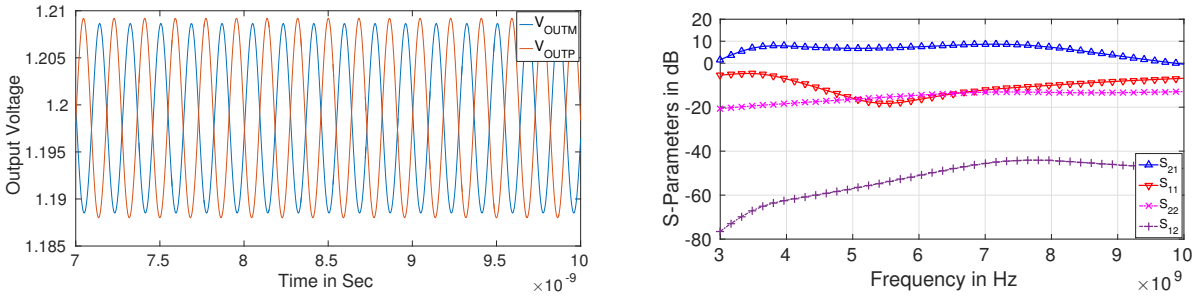
(a) Differential gain **(b)** Noise figure

(c) Gain error **(d)** Phase error

Figure 4.12: Schematic and Post-layout simulations of proposed LNA.

The differential gain and noise figure of proposed LNA over wide-band is shown in Figure 4.12a and Figure 4.12b respectively. The noise performance in the upper band is penurious. There are two authoritative reasons, the first one is, the magnitude response of designed buffer is not uniform through-out the band (i.e., there is approximately 3 dB difference from lower to upper band which is clearly observed in Figure 4.12a) and second one is, noise from extracted resistance and buffer. The gain and noise accomplishment of proposed balun LNA core alone has flat band response when compared to presence of test buffers. The gain error between differential outputs (i.e., v_{outp}, v_{outm}) has been brought down to less than 0.8 dB by careful tuning of W/L and load. The simulation result in Figure 4.12c shows worst case gain difference is 0.8 dB over a band of 3.1 GHz to 9.8 GHz. Both schematic and post layout simulation

result shows that phase error between differential output is less than 10° as shown in Figure 4.12d.



(a) **(b)**

Figure 4.13: Post-layout simulations of proposed LNA (a) Transient response at $f_{in} = 5\,GHz$ and P_{in}=–40 dBm (b) Analysis of S-parameters.

Figure 4.13a shows the transient response at the output (after buffers) for the input power (P_{in}) of –40 dBm. Figure 4.13b shows the analysis of S-parameters. The power gain of 9 dB with a 3-dB bandwidth sheathing a range 3.1 GHz to 9.8 GHz. Since the voltage gain loss of the test buffer is 3.5 dB, the authentic LNA voltage gain is 12.5 dB, which is sufficient to eliminate the effect of mixer losses (Henderson and Camargo (2013)). The input (S_{11}) and output (S_{22}) reflection coefficient are less than –10 dB throughout the band and matches very well with post layout results. The layout of proposed LNA is shown in Figure 4.14. The active area of core balun

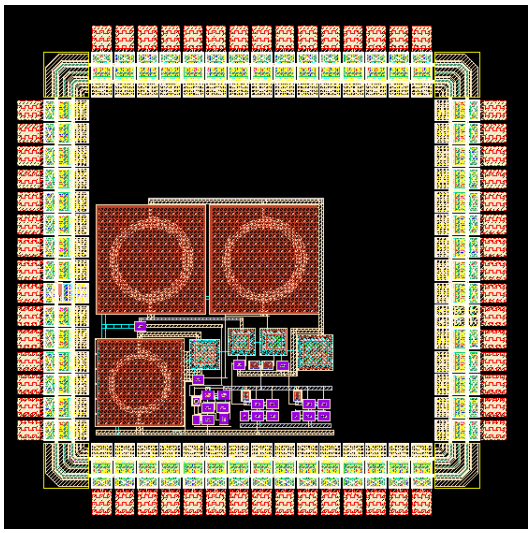


Figure 4.14: Layout of balun LNA core.

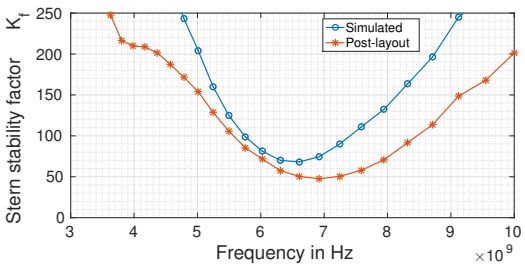


Figure 4.15: Analysis of stability factor.

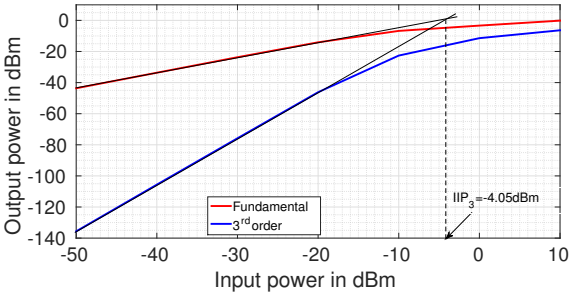


Figure 4.16: Calculation of IIP_3.

LNA including biasing circuit and buffers is $700\mu\text{m} \times 730\mu\text{m}$. The detailed stability analysis has been done using Stern stability analysis. The stability factor K_f is given by

$$K_f = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \tag{4.14}$$

where Δ=$S_{11}S_{22} - S_{12}S_{21}$. As per Stern stability analysis, the stability factor (K_f) should be ≥ 1 and Δ is <1 for unconditional stable system. The analysis of K_f is shown in Figure 4.15. Figure 4.16 shows the calculation of IIP_3. The feasibility of the proposed balun LNA is commonly established using a pertinent figure of merit (FoM) that calibrate its accomplishment. The fair comparison has been done using two FoMs. The FoM_1 is included with gain, band-width (BW), noise figure and power consumption to meet wide-band system specifications as given in Linten *et al.* (2005).

$$FoM_1 = \frac{Gain[abs].BW[GHz]}{(NF-1)[abs].(P_{DC}(mW)/10^{-3})} \tag{4.15}$$

The FoM_2 of proposed balun LNA is defined to include both gain and phase error. FoM_2 is given as

$$FoM_2 = \frac{Gain[abs].BW[GHz]}{(NF-1)[abs].(P_{DC}(mW)/10^{-3}).gain\,error[abs].phase\,error[degree]} \tag{4.16}$$

Table 4.2 encapsulates the simulated performance of the proposed UWB balun LNA and compares with recent state of the art LNAs that have earmark similar applications. It is clear from the comparison that higher values of FoM_1 and FoM_2 of proposed balun LNA proves better as compared to other reported LNAs.

Table 4.2: Performance comparison of UWB LNA.

Work	Technology (μm)	Frequency (GHz)	Gain (dB)	Noise Figure (dB)	Power dissipation (mW)	S_{11} (dB)	IIP_3 (dBm)	Topology	Gain(dB)& Phase(Degree)error	FoM_1	$FoM2$
Yousef *et al.* (2014) Pre-layout	0.18	3.1-10.6	12.25	3.8	18	$<$-10	2.5	SE	N/A	4.96	–
Baraani *et al.* (2015) Post layout	0.18	3-5	16	3.2	19.4	$<$-10	-22^b	FD	N/A	3.76	–
Lo and Kiang (2011) Measured	0.18	3.1-10.3	9.6	3.9	13.4	$<$-9	-3	SE	N/A	3.07	–
Bevilacqua *et al.* (2006) Measured	0.13	3-5	9.5	3.5	16.5	$<$-10	-6^b	FD	N/A	0.87	–
Chen *et al.* (2013) Post-layout	0.13	3.5-4	28^a	3.4	2.1	$<$-6 dB	^{c}	SD	^{c}	20.0	–
Blaakmeer *et al.* (2008*b*) Measured	0.065	0.2-5.2	13^a	3.5	21	$<$-10	$>$0	SD	0.7 & 2	1.92	0.817
Kim and Silva-Martinez (2012) Measured	0.13	0.1-2	7.6	4.15	3	$<$-10	0.5	SD	0.5 & 5	2.27	0.404
Martins *et al.* (2011) Post-layout	0.13	2.4	30^a	2.6	3.6	$<$-10	^{c}	SD	2 & 10	16.98	1.071
Liu *et al.* (2014) Measured	0.18	0-1.4	16	3	12.8	$<$-10	-13.3	SD	1 & 2.5	4.37	1.388
Zokaei *et al.* (2014) Pre-layout	0.13	3-4	11.2	3	16.9	$<$-12 dB	1.5	FD	N/A	0.783	–
This work:: Post-layout	0.18	3.1-9.8	18^a	4.2	3.8	$<$-10	-4.05	SD	0.8 & 10	14.5	32.7

^{a}Voltage gain, ^{b}1-dB compression point, SE - Single Ended, FD - Fully Differential, SD - Single to Differential, ^{c}Data not given. N/A-Not Applicable

4.7 Summary

A low power, noise cancellation and current re-use balun LNA is proposed for UWB applications using UMC 0.18-μm CMOS technology. CG-CS topology has been used as a basic technique for wide-band impedance matching and noise cancellation of input transistor. The bandwidth of CG-CS stage has been expanded by stacking differential amplifier with staggered tuning. The transistors are operated in saturation with optimum biasing and W/L ratios to eschew velocity saturation, voltage headroom and power consumption. The capacitor C_{ac} is used to provide small signal ground to differential amplifier. This capacitor improves the noise and balance operation of LNA.

The differential voltage gain of proposed balun LNA is 18 dB over a band-width of 3.1 GHz to 9.8 GHz. The input and output isolation is less than –8 dB and –14 dB respectively. The noise figure is 3.9 dB, IIP_3 of –4.05 dBm and consuming only 3.8 mW from 1.2 V supply. The gain and phase errors are 0.8 dB and 10^0 respectively. The proposed LNA is covering both band-group 1 and 6 which is the main corner-stone of all UWB wireless companies. The simulation results of the proposed UWB LNA shows very competitive performance with lowest power consumption and balun function over recently published UWB LNAs.

Chapter 5

INDUCTORLESS BALUN LNA

5.1 Introduction

Nowadays, the design of high-end wireless devices focuses on wide-band to cover minimum of 5 to 10 standards over different frequency bands. This trend will become popular in the future and creates many new design challenges with low area, power and single chip RF front-end. One of the main advantages of wide-band system is their re-usability and low cost. The performance of multi-standard receiver architecture depends on the design of low noise amplifier. The parallel connection of narrow-band LNAs have the disadvantage of large die area and lack of reconfigurability (explained in Section 1.4). Nevertheless, tunable LNA with active inductor covers the desired band, the poor noise performance beneath its advantage (Slimane *et al.* (2012)). Many countries are using ultra high frequency (UHF) band for ISM applications (260 to 470 MHz), high quality digital signal for digital TV (DTV) applications (470 to 890 MHz) and GPS & B_2 systems for GNSS receivers (Wu *et al.* (2011), ATScomm (2004)).

A wide-band LNA with operating frequency of 0.2 to 2 GHz would be better choice to meet the demand of high-end devices. Furthermore, to reduce the chip area and integration complexity of target applications, an inductor-less wide-band LNA is preferred over its parallel connections of single-ended counter part (Liu *et al.* (2014)). The specifications of targeted multi-standard RF front-end are given in Table 5.1. The maximum received signal power varies from –80 to –30 dBm. The targeted specifications are derived from (3.3) and (3.5) by considering 400 kbps DQPSK input with bit error rate better than 10^{-3} and 10 dB SNR at the output of front-end. There

Table 5.1: Specifications of multi-standard front-end.

Parameter	Value
[a]Maximum/minimum received signal power	−30 dBm/−80 dBm
[b]Noise figure at sensitivity=−80 dBm and BW=6 MHz	16.2 dB
[b]IIP_3 (if maximum strength of interferer is −40 dBm)	>-15 dBm
[b]Power dissipation	≤ 7 mW
[b]Gain and phase difference	<1 dB and $< 5°$
[a]Given by UHF-ISM, digital TV and GPS standard [b]Target specifications	

is no unified inter-modulation specification for multi-band applications. Thus, it is assumed that the power of interferer is at a maximum level of the receiving signal. So, according to (3.5), the third order input intercept point is greater than –15 dBm.

5.2 Prior work

Many inductor-less wide-band techniques have been proposed for multi-standard applications. Most of the designs are either single-ended (Yu *et al.* (2010), Slimane *et al.* (2014), De Souza *et al.* (2017)) or fully differential (Sobhy *et al.* (2011), Geddada *et al.* (2014), Pan *et al.* (2017)) with inevitable balun. The additional balun inherently leads to gain and phase imbalance at the differential output. Some specific designs are reported on inductor-less single to differential (SD) LNA (Im *et al.* (2010), Wang *et al.* (2010), Kim and Silva-Martinez (2012)). The LNA proposed in (Wang *et al.* (2010)) is based on CG-CS technique, in which common source (CS) stage is replaced with a complementary current re-use CS amplifier. Similarly, the LNA reported in (Kim and Silva-Martinez (2012)) uses a local feedback to enhance the g_m of CG stage. Nevertheless, both the designs provide good gain and linearity, but the signal imbalance and additional noise from cascode transistor are bottlenecks. Furthermore, most of the proposed designs are sensitive to PVT variations. This demands for additional bias compensation circuit which effects overall LNA performance.

An inverter based inductor-less single-to-differential wide-band LNA is proposed for digital TV applications. It comprises of three inverter-based gain stages with a global shunt feedback resistor as shown in Figure 5.1 (Liu *et al.* (2014)). Further, in the third gain stage a shunt capacitor with a current bias transistor is used to

enhance the gain/phase imbalance and the linearity of LNA. The first stage is an inverter-based amplifier with a feedback network and a self bias network to establish impedance matching and biasing point. The last two stages have local feed back to set the bias point. However, this technique consumes more power (i.e., 12.8 mW) and poor balanced operation with phase error of 4°.

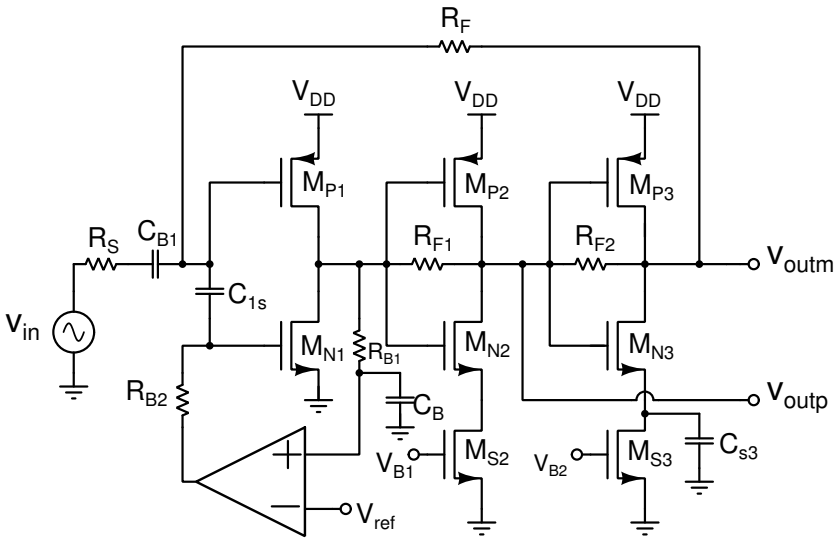


Figure 5.1: Inverter-based SD LNA with a global shunt feedback.

A fully differential CG LNA is proposed for digital TV applications as shown in Figure 5.2 (Im and Nam (2014)). It comprises a wide-band noise cancelling common gate LNA with a capacitively cross-coupled current source (CCCS). It offers wide-band noise cancelling without RF choke inductors in the range of 54 to 882 MHz. However, the complexity involved in the design of CCCS and high power consumption (i.e., 27 mW) degrades its superiority.

5.3 Basic idea and implementation

The design of single to differential (SD) LNA is very crucial in the multi-standard receiver systems. A low power inductor-less LNA is the preferable choice to fulfill ever increasing demand on superior functionality without compromising the portability of system. The moderate or inversion region of MOSFET is the traditional technique for low power designs. But, this leads to the following shortcomings: (i) poor LNA noise performance (ii) large variations in g_m against unavoidable PVT (Luo *et al.* (2014)).

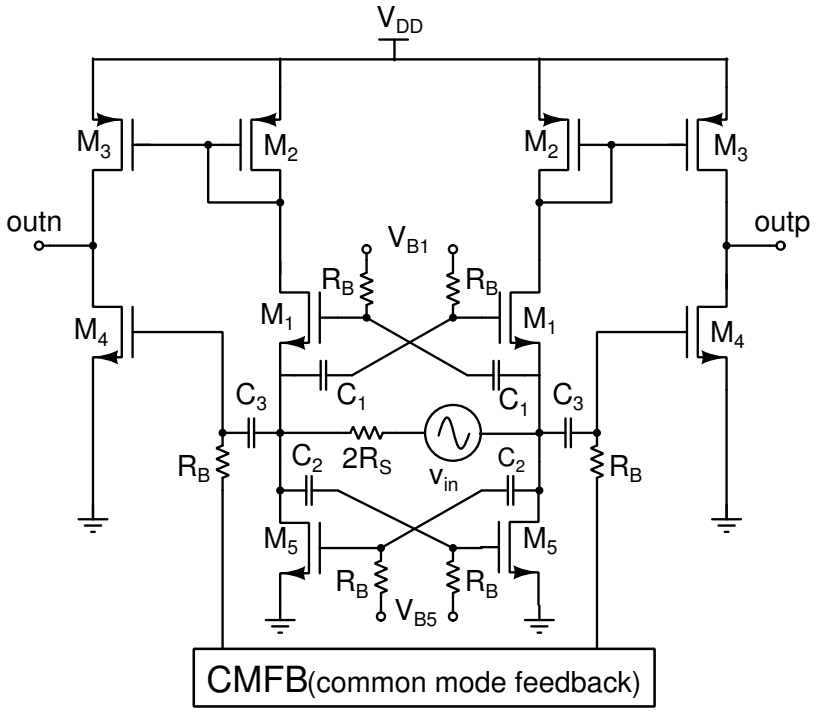


Figure 5.2: Noise cancelling CG LNA adopting a CCCS to remove RF choke inductors.

However, many bias compensation techniques have been proposed to minimize the variations in transconductance of core transistor (Jansen *et al.* (2013), Talebbeydokhti *et al.* (2006)). But, these techniques demand for additional power as well as core device of LNA to be a part of bias compensation. So, to avoid the use of additional compensation circuit, the transistors of proposed LNA are operated in the saturation region. From the highlighted portion of Figure 5.3, we can observe that, though the lower values of g_m over I_D leads to high power consumption, has less variation in g_m against V_{GS}. The feed-forward technique is familiar to reduce the overall power consumption and avoid the tight relationship between input resistance and noise figure of CG transistor. The common-gate stage with a feed-forward technique is shown in Figure 5.4a. This technique enhances the g_m of transistor M_1 by $(1+A)$ times, where A is the voltage gain of the amplifier. In the proposed design, similar g_m enhancement is achieved differently by using voltage-shunt feedback. Simple CG-CS topology has been used in the proposed LNA for differential conversion of incoming antenna signal as shown in Figure 5.4b. The current bias is replaced with a transistor to reduce the variations in bias point and have low area advantage. However, the biasing circuitry using the passive resistor could cause uncertain bias points because

of process variations. The bulky and low-noise off-chip inductor can be used to reduce the noise, but the advantage of the inductor-less architecture is discounted.

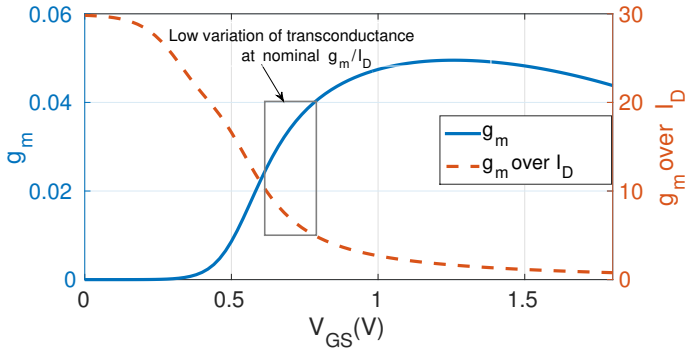


Figure 5.3: Variation of g_m(S) and g_m/I_D against the bias voltage for 0.18-μm CMOS transistor at W=25μm and L=0.18μm.

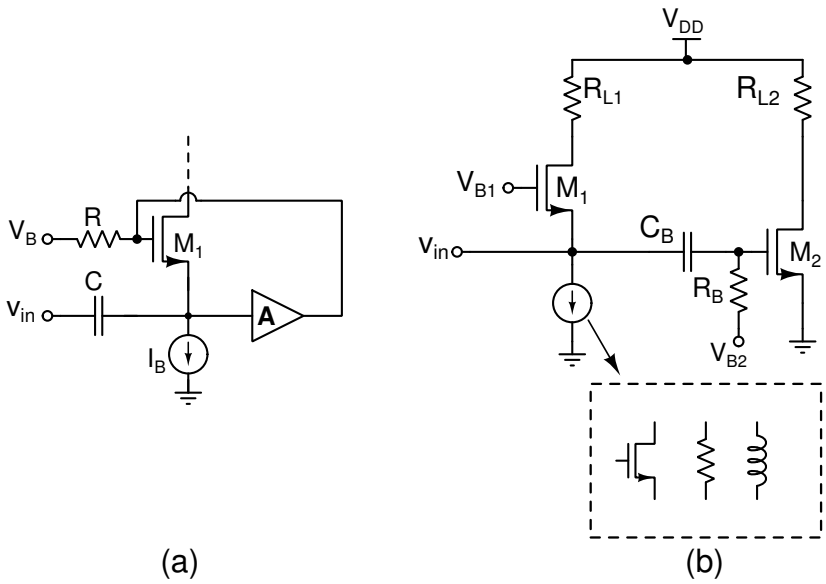


Figure 5.4: (a) CG stage with feed-forward technique (b) Traditional CG-CS LNA.

In multi-band receivers, the choice of receiver architecture depends on bandwidth of the channel. In literature both low-IF heterodyne and homodyne architectures have been used for better performance. However, in multi-band systems the probability of narrow-band channel is high, so using low-IF heterodyne would be the better choice to preserve the channel loss during the demodulation. As we have discussed in Section 1.4, redundant LNAs increase the cost and area. An inductor-less balun LNA is the

suitable choice to vanquish the above mentioned issues and meet the requirements of low area and power. In this Chapter, a PVT independent inductor-less balun LNA suitable for multi-standard applications is proposed. The proposed LNA uses traditional CG-CS technique with a local voltage shunt feedback technique. The biasing point of all transistors is chosen such that the variation in g_m across PVT is not more than 10%. Though, the idea for PVT independent behavior increases the power consumption, the shunt feedback technique reduces the overall power consumption. The pole at the output of CG stage is pulled to lower frequency to correct gain and phase error without disturbing the noise performance unlike the technique reported in Kim and Silva-Martinez (2012). Finally, less number of components have been used to design the proposed LNA. The block diagram of multi-standard front-end with proposed LNA is shown in Figure 5.5.

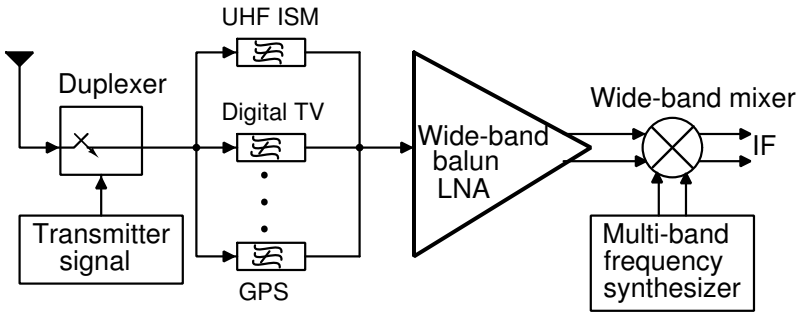


Figure 5.5: Block diagram of the multi-standard front-end using proposed inductor-less balun LNA.

5.4 Inductor-less LNA schematic and analysis

The complete circuit diagram of inductor-less balun LNA is given in Figure 5.6. The proposed LNA is mainly constructed by CG-CS topology with transistor (M_{B1}) as biasing element instead of resistor or inductor. The noise/distortion of CG transistor (M_1) appears as a common mode noise at the output and it get cancelled by the CS transistor (M_2). Furthermore, a voltage shunt feedback (C_{fb}) has been used to enhance the g_m of CG transistor without disturbing the noise cancellation condition. The condition for noise cancellation is given as

$$g_{m1}(1 + A_{V_{CS}})R_{L1} = g_{m2}R_{L2} \tag{5.1}$$

where $A_{V_{CS}}$ is the voltage gain of CS stage. The input impedance R_{in} is given by

$$R_{in} = \frac{1}{g_{m1}(1 + A_{V_{CS}})} \tag{5.2}$$

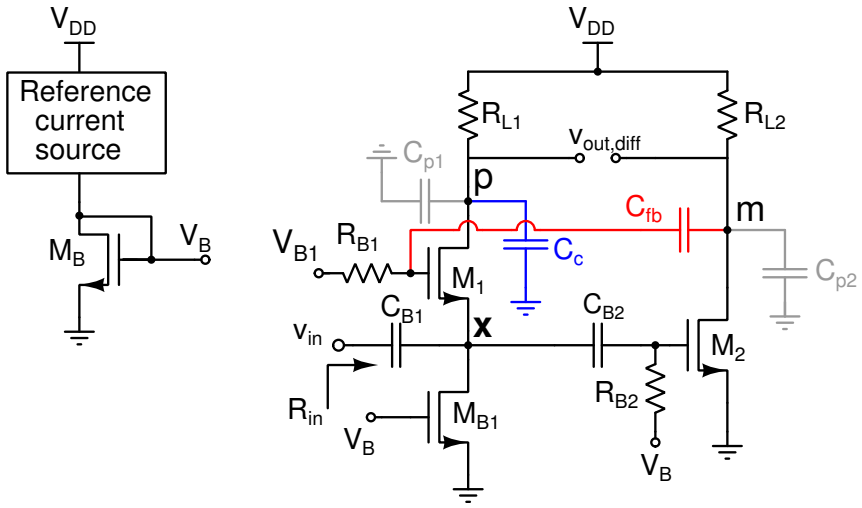


Figure 5.6: Proposed PVT independent inductor-less balun LNA.

The noise contribution of CS stage is inversely proportional to its g_m (i.e.,g_{m2}). So, higher values of g_{m2} improves the noise performance of LNA. The feedback capacitor and higher width of M_2 reduces the bandwidth at the output node of CS transistor. Moreover, the capacitor C_{fb} leads to gain and phase imbalance at the outputs. So, a compensation capacitor C_c is used at the output of CG transistor to pull the pole for minimum gain and phase error. Now even if, the proposed LNA drives the next stage (i.e., mixer), the imbalance between signals will not get disturbed by the parasitics of next stage (since the mixer is differential, same parasitics will be added on both sides). As the proposed LNA is insensitive to PVT variations, a simple bias circuit is used to bias all the transistors.

5.4.1 Effect of C_c on gain and phase imbalance

The small signal equivalent circuit of proposed LNA is shown in Figure 5.7. The voltage at node 'x' is given by

$$v_x = \frac{v_{in} \times r_{on,M_{B1}}}{R_S + r_{on,M_{B1}}} \simeq v_{in} (\because R_S \gg |\frac{1}{sC_{B1}}| \; and \; r_{on,M_{B1}} \gg R_S) \tag{5.3}$$

$$Z_f = \frac{1}{sC_{fb}} + \left(R_{B2} \| \frac{1}{sC_{gs_1}} \right) \simeq \frac{1 + R_{B2} sC_{fb}}{sC_{fb}} \tag{5.4}$$

$$Z_{L2} = \frac{R_{L2}}{1 + sC_{p2}R_{L2}} \tag{5.5}$$

where Z_{L2} is the output impedance at node 'm'. Now, the overall output impedance (Z_{o2}) at node 'm' is given by (5.6).

$$Z_{o2} = \frac{(R_{L2}/2)}{1 + sC_{p2}(R_{L2}/2)} \tag{5.6}$$

The output voltage at node 'm' and 'p' is given by

$$v_{outm} = \frac{-g_{m2}R_{L2}}{2} \times \frac{1}{1 + sC_{p2}(R_{L2}/2)} \times v_{in} \tag{5.7}$$

$$v_{outp} = g_{m1} \left(1 + \frac{g_{m2}R_{L2}}{2} \frac{1}{1 + sC_{p2}(R_{L2}/2)} \right) \times \frac{R_{L1}}{1 + sC_t R_{L1}} \times v_{in} \tag{5.8}$$

It is noticed from (5.7) and (5.8) that, both gain and phase balance is possible if there

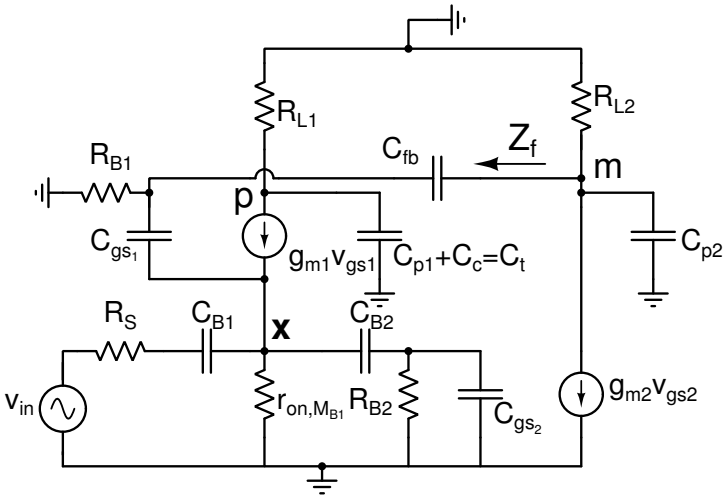


Figure 5.7: Small signal equivalent circuit.

is a control over capacitance C_t. As we have taken feedback from node 'm', the pole shifts toward the lower band-width and leads to gain and phase mismatch between outputs. The variation of gain error against variations in C_c is little but has a huge

effect on the phase error. The variation of phase error for different values of C_c has been analyzed and shown in Figure 5.8. In the absence of C_c, the maximum phase error in the band of interest is 7°. So, a suitable value of C_c is chosen to minimize the phase error (i.e., 0.8°) without disturbing other performance parameters of LNA.

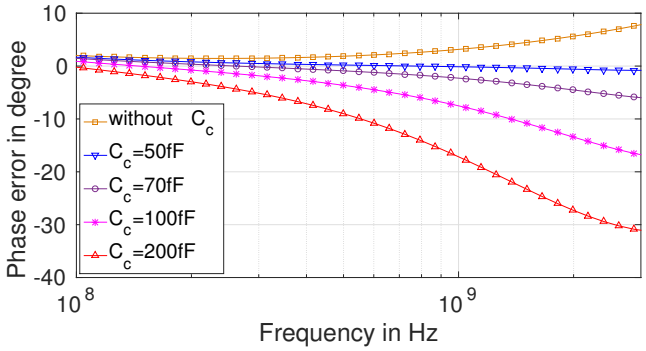


Figure 5.8: Effect of C_c on phase error.

5.4.2 Noise analysis

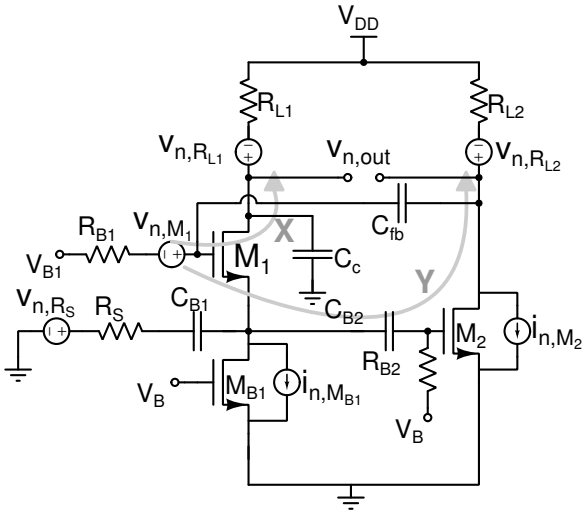


Figure 5.9: Noise equivalent circuit of proposed LNA.

The noise equivalent circuit of inductor-less balun LNA is shown in Figure 5.9. The noise power of M_1 ($\overline{v_{n,M_1}^2}$) sees two paths to the output (i.e., X and Y). The path 'X' amplifies the noise by $g_{m1}(1 + A_{V_{CS}})R_{L1}$ times and the path 'Y' provides the gain of $g_{m2}R_{L2}$. The noise of M_1 appears as common mode noise at the output since the

gain of both paths 'X' and 'Y' is equal as given in (5.1). Now, the noise contribution of M_{B1} and M_2 is given by

$$\overline{v^2_{n_{out},M_{B1}}} = \overline{i^2_{n,M_{B1}}} R_S^2 \times (g_{m1} g_{m2} R_{L1} R_{L2})^2 \tag{5.9}$$

$$\overline{v^2_{n_{out},M_2}} = \overline{i^2_{n,M_2}} R_{L2}^2 \tag{5.10}$$

In general, the overall noise factor (Nf) of the circuit is given as

$$Nf = 1 + \frac{\overline{v^2_{n,out}}}{A^2} \times \frac{1}{4kTR_S} \tag{5.11}$$

where $\overline{v^2_{n,out}}$ is the output noise power excluding source noise, A is the overall gain of LNA. Now the Nf of proposed LNA is given by

$$\begin{aligned} Nf = 1 + \gamma g_{m1} R_S + \frac{\gamma}{(g_{m1} R_{L1})^2 g_{m2} R_S} \\ + \frac{\gamma}{(g_{m1} g_{m2} R_{L2})^2 R_S R_{L1}} + \frac{\gamma}{(g_{m1} g_{m2} R_{L1})^2 R_S R_{L2}}. \end{aligned} \tag{5.12}$$

From (5.12), we can observe that the noise contribution from M_2 depends on its transconductance. Furthermore, the lower value of $g_{m1}R_S$ product gives the better noise performance. So, transconductance scaling and g_m enhancement technique has been employed on CS and CG stage respectively.

5.5 Gain switching

In multi-standard systems, few common difficulties are: (i) the presence of inter-modulation degrades the sensitivity and SNR (Meghdadi *et al.* (2017)) (ii) The strong input level, which may degrade the linearity of subsequent stages. These difficulties can be avoided using high dynamic range LNA. The gain switching of LNA is an effective method to improve the dynamic range and linearity (Jeong *et al.* (2008)).

As the proposed LNA is single to differential (SD), switching has to be done on both CG and CS stage. But, from (5.1) the gain of both outputs is mainly decided by CS stage. The transistor M_{SW2} is used to switch the gain by step of 4 dB. Unfortunately, this technique inherently disturbs the g_m enhancement of CG stage. This can be avoided by using an additional transistor in parallel to M_1, but impedance matching

will get disturbed. So, a transistor M_{SW1} is used to avoid impedance mismatch at the input without disturbing noise cancellation and g_m enhancement techniques. The complete circuit diagram of proposed LNA with gain switching mechanism is shown in Figure 5.10.

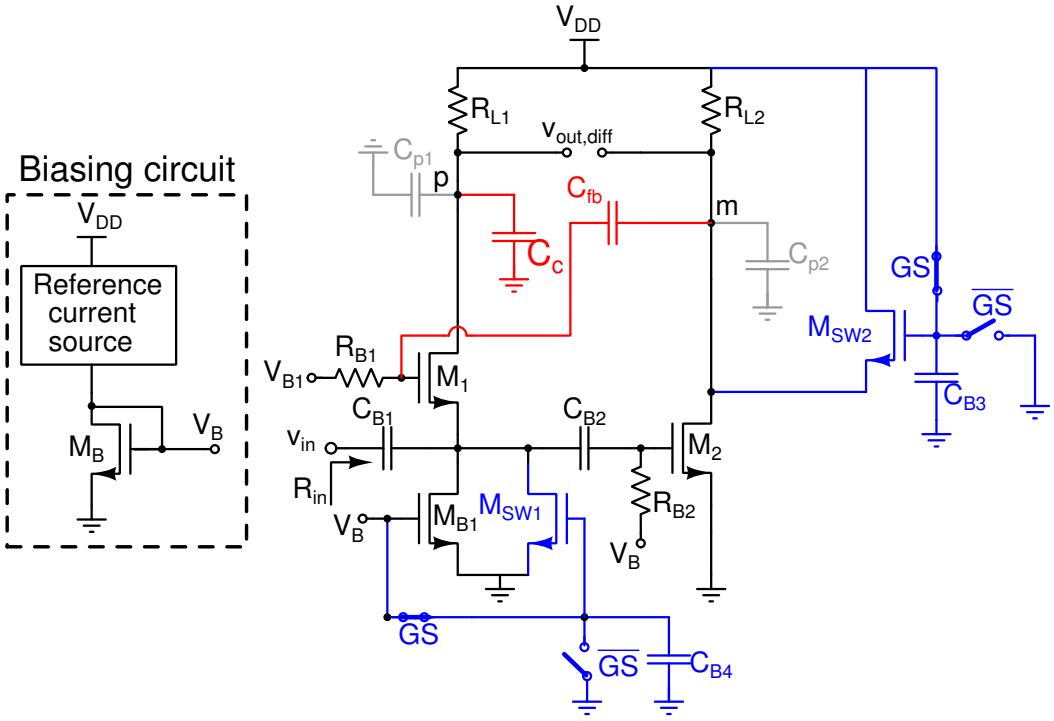


Figure 5.10: Inductor-less balun LNA with gain switching.

When gain switching is enabled, the transistor M_{SW2} enters into saturation and draws a portion of current from M_2. This decreases the gain at node 'm' and also at 'p' because of voltage shunt feedback. But, degradation in the gain of CS stage ($A_{V_{CS}}$) disturbs the input impedance matching. So, a transistor M_{SW1} is used to avoid this effect by increasing the g_m of transistor M_1. The proposed switching technique offers a gain step of 4 dB at little increase in both power and noise. The periodic ac and noise analysis has been carried-out to analyze the gain and NF of proposed gain switching LNA. In the low gain mode it offers gain of 17 dB and noise figure of 3.85 dB (i.e., including switching noise). The performance summary of both high and low gain mode of proposed LNA is given in Table 5.2.

Table 5.2: Performance summary of proposed balun LNA.

Name of the Parameter	High gain mode	Low gain mode
Frequency in GHz	0.2-2	0.2-2.2
Gain in dB	21	17
Noise figure in dB	2.8	3.85
S_{11} in dB	<–11	<–11
IIP_3 in dBm	–4	–2
Power dissipation in mW	5.76	6.05
Gain and phase error	0.3 dB and 0.8°	1 dB and 0.5°

5.6 Post-layout simulation results

The proposed inductor-less LNA is implemented using 0.18-μm CMOS technology. The layout of LNA is highlighted in Figure 5.11 and it is compared with UWB LNA designed by inductors to enrich the importance of proposed inductor-less LNA. The area of the core LNA is 182μm×181μm, which is even less than a single inductor of a value 4 nH. The differential gain is 21 dB and noise figure is 2.8 dB as shown in Figure 5.12a. Figure 5.12b shows that the third order input intercept point (IIP_3) is –4 dBm and is good enough for all applications in the range of 0.2 to 2 GHz. The gain and phase error between the outputs has been minimized through careful investigation and extensive simulation. The worst-case gain and phase error in the band of interest is 0.3 dB and 0.8° as shown in Figure 5.12c.

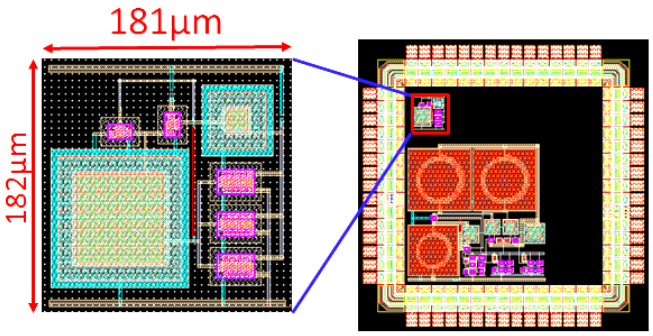
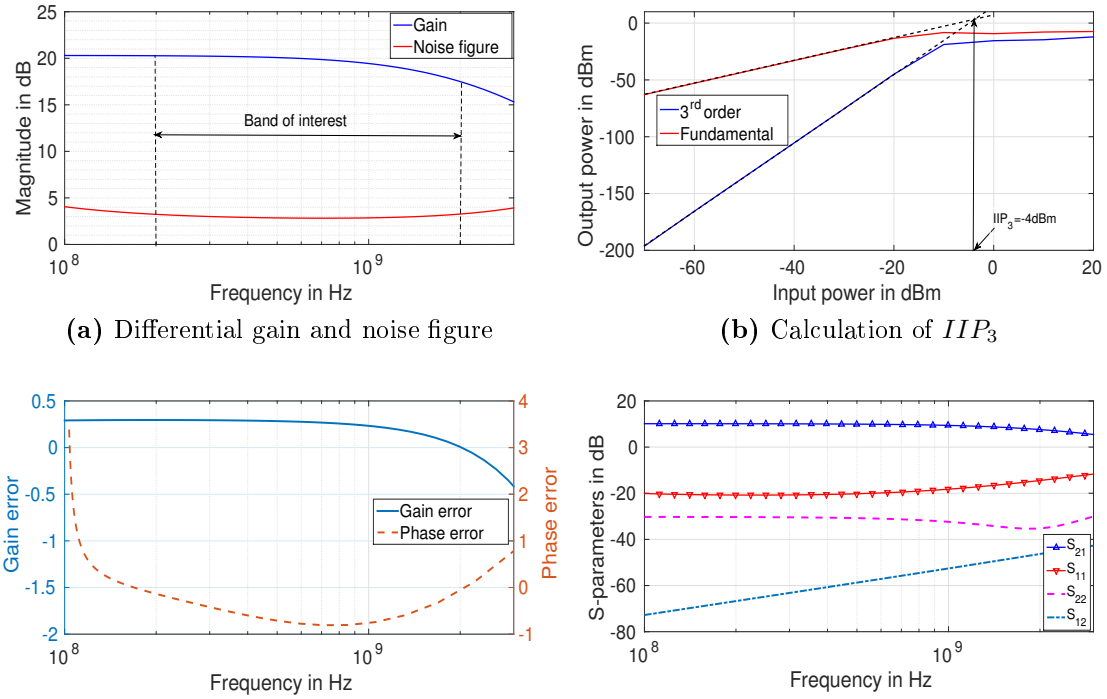


Figure 5.11: Layout of proposed inductor-less LNA (Layout of wide-band LNA is considered for comparison).

The S-parameter analysis has been done to validate the design. As the proposed LNA is single to differential, two test buffers and a balun have been used to match with the output port. The power gain supposed to be 14 dB, but it is 10 dB since

there is loss of 4 dB from additional buffer. The input and output reverse isolation is less than −12 dB. The reverse voltage gain is less than −40 dB. Figure 5.12d shows the analysis of S-parameters.



(a) Differential gain and noise figure

(b) Calculation of IIP_3

(c) Gain (in dB) and phase (in degree) error

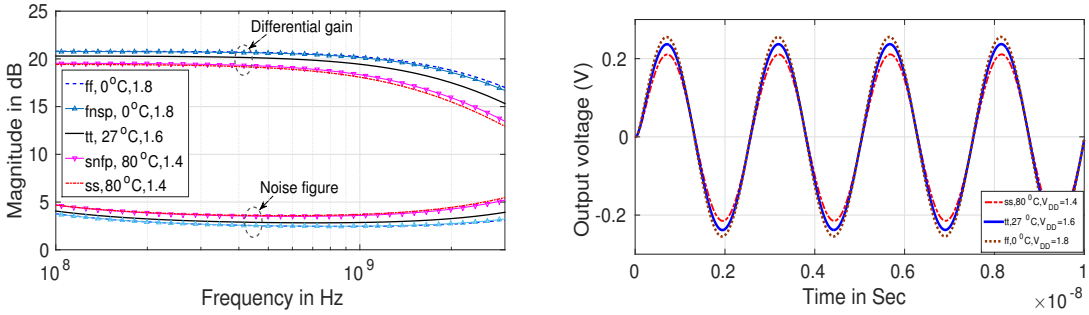
(d) Analysis of S-parameters

Figure 5.12: Post-layout simulations of proposed LNA.

Table 5.3: Performance variations of proposed balun LNA against PVT and resistor variations.

LNA Parameter	Process corners	Supply variation (±10%)	Temperature 0°C to 80°C	Resistor corners	Worst case corner variation
Δ Gain in dB	0.29	0.6	0.3	1.5	0.9
Δ NF in dB	0.17	0.7	0.13	0.2	0.8

The sensitivity of the proposed LNA against unavoidable PVT variations decides its superiority over existing designs. So, the sensitivity of LNA has been analyzed over five process corners (i.e., $ff, fnsp, tt, snfp, ss$), supply voltage (±10%) and temperature range from 0°C to 80°C. It has been observed that, the worst-case corners are ff corner with 0°C and 1.8 V and ss corner with 80°C and 1.4 V. The maximum variation of differential gain and noise figure is not more than 1 dB when compared to the



(a) Differential gain and noise figure **(b)** Transient analysis

Figure 5.13: Post-layout simulations of proposed LNA against process corners, supply and temperature at P_{in}=–40 dBm.

nominal corner ($tt, 27°C$). The complete frequency response against PVT variations is shown in Figure 5.13a. The transient analysis is also observed to verify the linearity performance of proposed LNA for the input power of –40 dBm from 50 Ω antenna. Figure 5.13b shows the transient analysis of output voltage for all possible worst-case corners. The maximum variation of gain and noise figure across PVT and component variations are tabulated in Table 5.3.

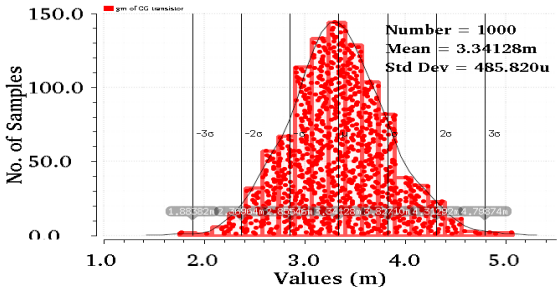
Finally, the proposed LNA has been validated by rigorous Monte Carlo simulations for both process and mismatch statistical variable with 1000 runs. Figure 5.14a and 5.14b shows the transconductance of CG and CS transistors at room temperature (27°C). The g_m of CG transistor has minimum spread with a standard deviation of 0.48 mS and g_m of CS transistor has 4.7 mS. Figure 5.14c and 5.14d show the variation of differential gain and noise figure. The standard deviation (σ) of gain and NF is 0.235 dB and 0.065 dB. The percentage of 3σ deviation in both gain and NF is less than 5% when compared to the mean value of typical corner.

The performance summary of inductor-less LNA along with recently published multi-standard CMOS LNAs is given in Table 5.4. The figure of merit (FoM) reported in Pan *et al.* (2017) is used for the comparison to select the most relevant parameters of LNA. The FoM is given by

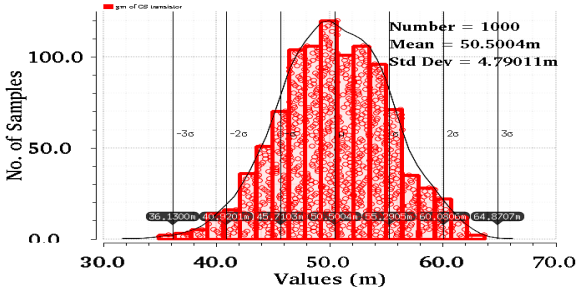
$$FoM = 20log_{10}\left(\frac{G_{max}[abs] \times BW[GHz]}{P_{DC}[mW] \times (NF[abs] - 1)}\right) \tag{5.13}$$

where G_{max} is the maximum voltage gain in linear units, BW is the bandwidth in GHz, P_{DC} is defined to be static power dissipation in mW and NF is the noise figure in

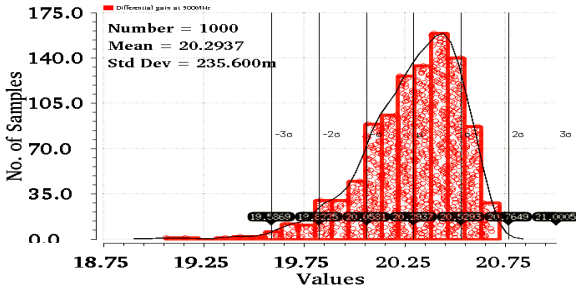
linear units. From Table 5.4, we can observe that the FoM of proposed LNA has third highest value as compared to other LNAs. The proposed LNA offers relevant performance and cost saving, since it has good ratio of FoM to chip area (182 μm×181 μm). Furthermore, the proposed inductor-less LNA has a good robustness against the PVT variations.



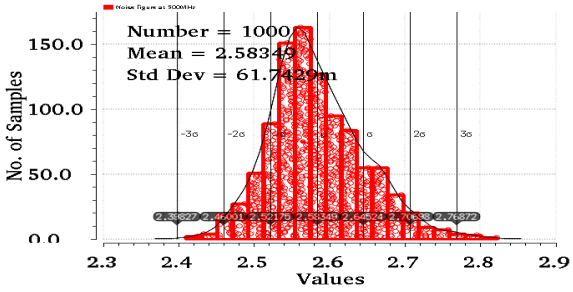
(a) Transconductance distribution of CG stage (g_{m1})



(b) Transconductance distribution of CS stage (g_{m2})



(c) Gain distribution of proposed LNA at 500 MHz



(d) Noise figure distribution of proposed LNA at 500 MHz

Figure 5.14: Monte Carlo analysis for both process and mismatch statistical variable at room temperature (27°C).

5.7 Summary

An inductor-less balun LNA is designed, analyzed and simulated for wide-band (0.2 - 2 GHz) to cover UHF-ISM band, digital TV and global navigation satellite system. As there is a demand for high-end devices with robustness, a PVT independent LNA is designed in UMC 0.18-μm CMOS technology. The proposed LNA uses CG-CS noise cancellation technique to have single to differential conversion of incoming antenna signal. A voltage shunt feedback and transconductance scaling techniques have been

Table 5.4: Performance comparison of Inductor-less LNA.

Work	Technology (μm)	Frequency (GHz)	Voltage Gain (dB)	Noise Figure (dB)	Power dissipation (mW)	IIP_3 (dBm)	Gain(dB)& Phase(degree) error	No. of Inductors	FoM	Active area (mm^2)
Liu *et al.* (2014), IEEE MWCL(Measured)	0.18	DC-1.4	16.4	3[a]	12.8	−13.3	1 &4.5°	0	−2.7	0.0383
Kim and Silva-Martinez (2012), IEEE MWT(Measured)	0.13	0.1-2	7.6	4.15[a]	3	0.5	0.5 &5°	0	7.14	0.075
De Souza *et al.* (2017), IEEE TCAS-I[b](Measured)	0.13	0.1-2.1	21.2	2	7.9	12.5	N/A	0	14.9	0.007
Zhu *et al.* (2015), IEEE JSSC(Measured)	0.065	0.2-1.6	24	3.6	20.2	14.5	N/A	0	-1.423	N/R
Wang *et al.* (2010), IEEE TCAS-I[c](Measured)	0.13	0.2-3.8	19	3.4	5.7	−4.2	N/R	0	13.55	0.025
Manstretta (2008), IEEE RFIC(Measured)	0.09	0.1-1	10	5[a]	7.5	−1	N/R	1	−5.1	0.032
Pan *et al.* (2017), IEEE MWCL[c](Measured)	0.065	0.1-4.3	21.2	4	2	−7.7	N/R	0	24	0.05
Huang *et al.* (2018), AEU[b](Post-layout)	0.18	0.3-3.5	14.6	3.5	14.8	1.2	N/A	0	−0.45	0.275
Ebrahimi *et al.* (2015), AEU[c](Post-layout)	0.18	0.01-1	28	1.4	27	−11	N/R	0	7.77	0.0454
Proposed (Post-layout)	0.18	0.2-2	21	2.8	5.76	−4	0.3 & 0.8°	0	11.81	0.032
[a]Minimum NF [b]single-ended LNA [c]differential LNA N/A= Not Applicable N/R= Not Reported										

deployed to optimize both power and noise. A capacitor C_c is used to minimize gain and phase error at the differential output. Layout of the proposed LNA occupies $182\,\mu\text{m} \times 181\,\mu\text{m}$.

The post-layout simulation of proposed LNA offers differential gain of 21 dB, noise figure of 2.8 dB and IIP_3 of −4 dBm while drawing 3.6 mA from 1.6 V supply. The proposed design is validated by sensitivity analysis against PVT and component variations. The worst-case variation in performance parameter is less than 5 % as compared to the nominal value. Furthermore, the proposed design is examined by rigorous Monte Carlo simulation for both process and mismatch statistical variable. The standard deviation in differential gain and noise figure is narrow and maximum deviation (3σ) is less than 0.7 dB and 0.18 dB respectively. The FoM value and area of proposed LNA makes it attractive for high performance receiver front-end. Finally, the proposed LNA uses less number of components and avoid the use of additional balun and bias compensation circuit.

Chapter 6

BIAS CIRCUIT COMPENSATION

6.1 Introduction

Irrespective of receiver architectures, in all receivers from cellular to medical applications low noise amplifier plays a vital role in improving the performance. Nowadays restriction on power consumption is increasing to meet high performance demands compromising on portability of the system.

The sub-threshold region and current re-use technique offers low power design. However, the exponential dependency of g_m on the overdrive voltage has large variations against PVT. The process and temperature variations pushes the sub-threshold transistor into either saturation or near cut-off region. This leads to change in g_m and I_D. Moreover the impedance matching, noise figure and power will be deplored for targeted applications.

6.2 PVT compensation

A conventional bias circuit is used for the proposed balun LNA explained in Chapter 3 (both design-I and design-II). Figure 6.1a shows the conventional bias comprises of a reference current source and bias transistor. It has been observed that, the variation in g_m and I_D of transistor M_B is more than 50% across PVT variations. It is also observed that, the variation in performance parameters of proposed LNA is more than 40%. Many constant-g_m circuits have been proposed for general purpose circuits such as filters and operational trans-conductance amplifiers (OTAs) (Laxminidhi *et al.* (2009), Zhang and Yuan (2012)). If these techniques are used for LNA, the core

transistor of the amplifier to be connected as part of the compensating mechanism, which in turn, affects the performance parameters of the LNA. So, there is thirst on low power LNA with compensation mechanism to tackle the parameter deviations against PVT variations.

In this work, a new PVT compensated bias circuit is proposed as shown in Fig. 6.1b. Bias circuit comprises of negative feedback and charge pump to track the variations in the balun LNA. A replica of LNA circuit has been taken to avoid the failure of entire circuit and deviation in LNA parameters.

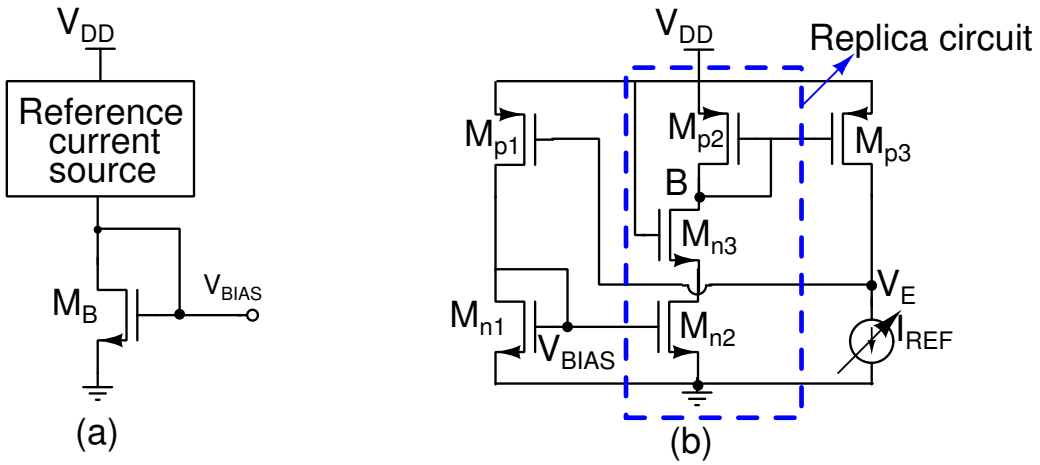


Figure 6.1: (a) Conventional bias circuit (b) Proposed PVT compensation bias circuit.

The transistors M_{n2} and M_{n3} are taken to replicate the actual balun LNA. The transistor M_{p2} is taken as load to set the required voltage and mirror the current. The transistor M_{p3} scales down the current of the replica circuit and compares with the reference current. The transistor M_{p1} acts as a variable current source according to the error voltage (V_E). This bias circuit will not provide complete compensation for parameter variations against PVT since the variation in $|V_{DS_{p2}}|$ of M_{p2} is not exactly equal to the actual LNA. But, it has been observed that the PVT variations are reduced by 55% as compared to conventional biasing. An external current reference has been taken to control the variations in gain against inductor and capacitor corners (since passive amplification of LNA is sensitive to L_{deg}, L_g and C_{ex} variations). The error voltage V_E tunes the V_{BIAS} according to the variations in LNA.

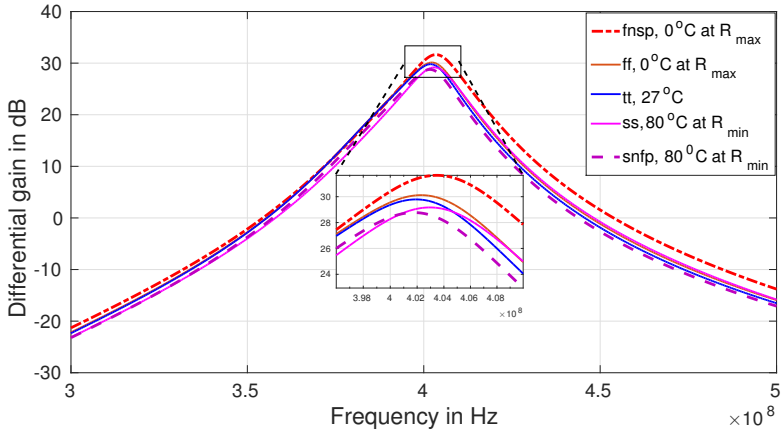
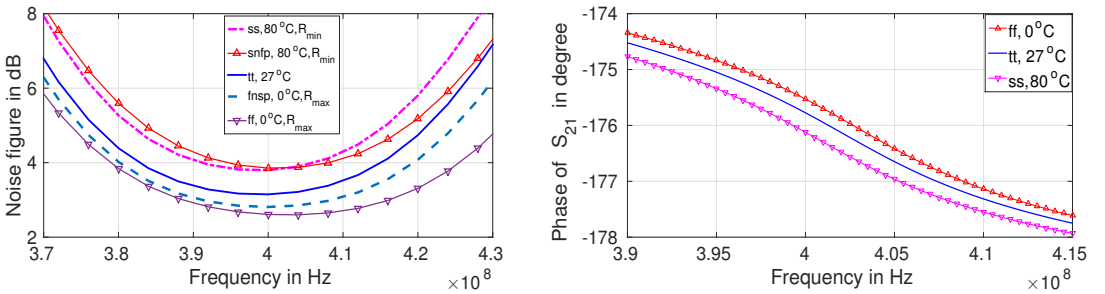


Figure 6.2: Post-layout simulations of differential gain against component and PVT variations.



(a) Noise figure **(b)** Phase variation of LNA transfer function

Figure 6.3: Post-layout simulations of proposed LNA against component and PVT variations.

Table 6.1: Variation of power and group delay across process corners.

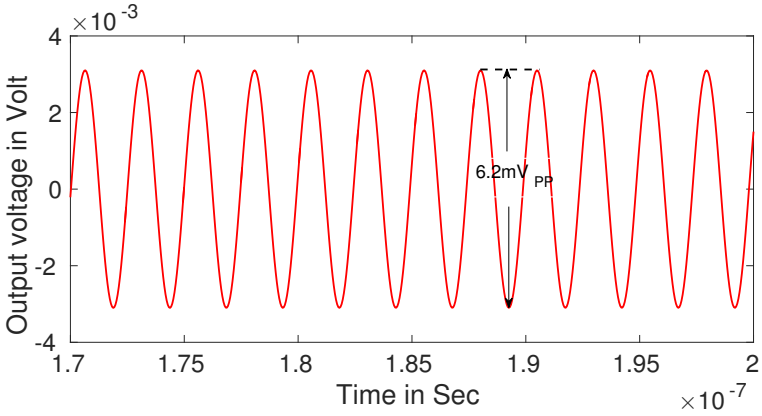
Name of the parameter	tt,27°C	ff,0°C	ss,80°C
Gain in dB	30.6	31.6	28.5
Current in μA	290	310	280
Power in mW	0.29	0.31	0.28
Group delay in ns	0.39	0.406	0.36

The sensitivity analysis of proposed LNA has been verified across different process corners of transistor, resistor and inductor over the temperature range from 0°C to 80°C. The maximum variation of differential gain and noise figure is ± 2.3 dB and ± 0.65 dB respectively as compared to the nominal corner (tt, 27°C). The variation of

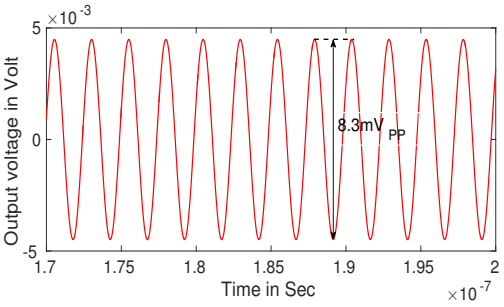
differential gain against all possible worst-case corners is shown in Figure 6.2. Figure 6.3 shows the post-layout simulations of noise figure and group delay across all process corners. The group delay is the derivative of phase of the system transfer function. In general, it is defined as

$$Group\ delay\ (t_g) = -\frac{\partial\phi}{\partial\omega} = -\frac{1}{360^\circ}\frac{\partial\theta}{\partial f} \tag{6.1}$$

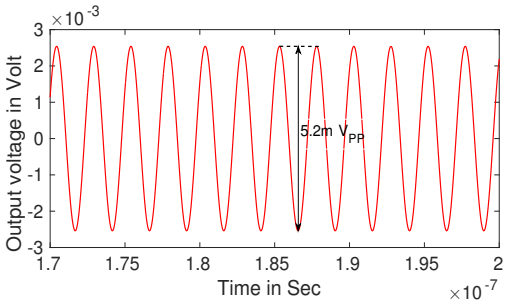
where ϕ and θ are the phase in radians and degrees respectively.



(a) *transient response at tt, 27° C*



(b) transient response at ff, 0°C



(c) transient response at ss, 80°C

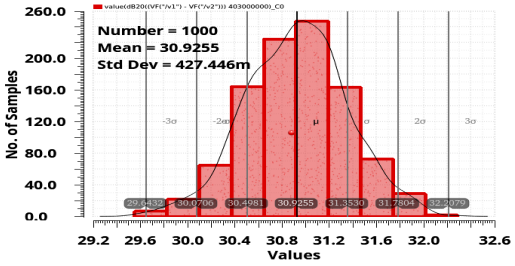
Figure 6.4: Post-layout simulations of proposed LNA for process corners over 0°C to 80°C at P_{in} = –70 dBm.

The group delay decides the amount of delay taking by the input frequencies while passing through the amplifier. In the band of interest, the lower variation of group delay is desirable to pass all the frequencies with relatively same amount of delay. The t_g of proposed LNA is calculated by differentiating the phase of S_{21} with frequency aperture of 6 MHz. The variation of phase against PVT variations is shown

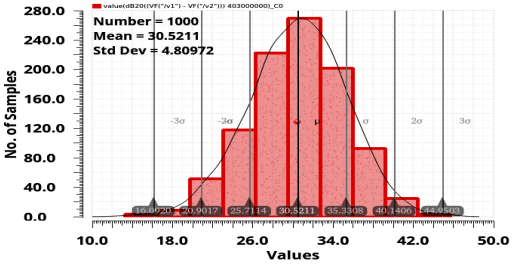
in Figure 6.3b. The analysis of gain, current, power consumption and group delay across worst case corners is given in Table 6.1. The maximum variation in t_g across all corners is 0.04 ns. Even the deviation in gain and current is less than 7% when compared to the nominal corner. The transient analysis has been observed across worst-case corners as shown in Figure 6.4. The output voltage swing at nominal corner with temperature 27°C is 6.2 mV_{PP} for an input power of –70 dBm from 50Ω antenna. Similarly, transient response has been observed for corners *tt* and *ss* to validate linearity of the proposed design. The variations in gain and noise figure across all corners including supply variations (±10% of V_{DD}) are given in Table 6.2.

Table 6.2: Performance summary of proposed compensated balun LNA against PVT and component variations.

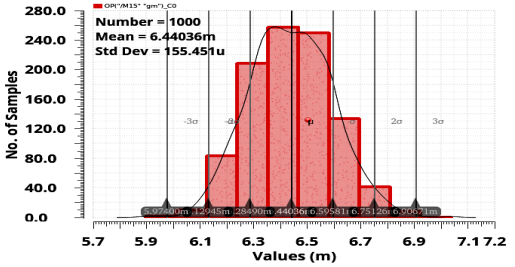
LNA Parameter	Process corners	Temperature 0°C to 80°C	Resistor corners	Inductor corners	Worst corner variations including supply (±10%) (with compensation)	Worst corner variations including supply (±10%) (with conventional)	Percentage reduction of parameter variation at worst corners
Δ Gain in dB	1.5	1	0.2	1	4.6 (±2.3 dB as compared with nominal	10.2 (±5.1 dB as compared with nominal)	55%
Δ NF in dB	0.6	0.3	0.1	0.1	1.3 (±0.65 dB as compared with nominal	2.5 (±1.25 dB as compared with nominal)	48%



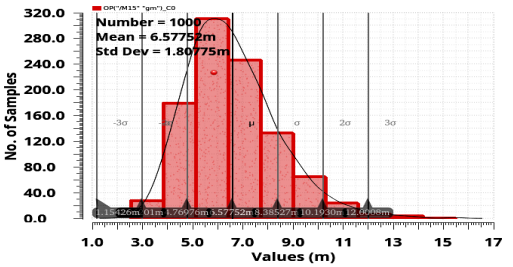
(a) Gain distribution of compensated LNA



(b) Gain distribution of conventionally biased LNA



(c) g_m distribution of compensated LNA



(d) g_m distribution of conventionally biased LNA

Figure 6.5: Monte Carlo analysis for both process and mismatch statistical variable (for $\sigma = 3$).

Finally, Monte Carlo simulations include both process and mismatch statistical variable for 1000 occurrences are carried out. Figure 6.5 shows the distribution of differential gain (at f_{in}= 403 MHz) and transconductance of the transistor (M_1 in Figure 3.13) at 27°C temperature. The proposed balun LNA has been analyzed with both conventional and compensated biasing circuits. The analysis shows that, the differential gain and g_m of proposed compensated balun LNA has a narrower spread with a standard deviation of 0.42 dB and 0.155 mS respectively. The 3σ deviation of differential gain and transconductance of core transistor for proposed LNA with bias compensation is less than 4%.

6.3 Process and temperature compensation

The balun LNA shown in Figure 4.9 is proposed for UWB applications. As discussed in Section 4.5, the transistors M_1 and M_2 are operated in saturation region to meet the target specifications. Initially, a conventional bias circuit has been used to bias the transistors. So, to analyze the parameter variations, the sensitivity analysis of proposed LNA has been elucidated by focusing on the gain and noise figure against PVT variations.

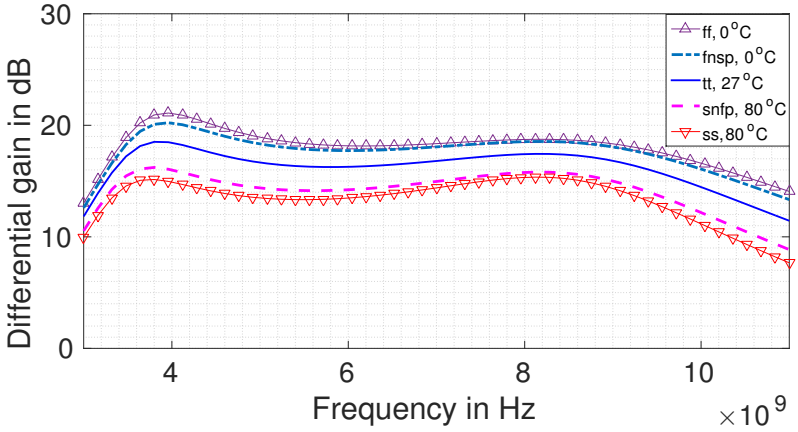


Figure 6.6: Differential gain against PVT variations (post-layout).

The proposed balun LNA has been substantiated under five different corners (i.e., $ff, fnsp$, nominal, $fpsn, ss$), temperature range from 0°C to 80°C and supply variation of ±10%. Figure 6.6 shows the variation of gain across worst-case corners. It is noticed that, the variation in LNA parameters are comparatively less, but needs to be

improved. The trans-conductance (g_m) of MOSFET plays a critical role in determining LNA parameters. It is often desirable to design constant g_m circuit against PVT variations. A simple supply independent beta multiplier circuit is used to define the g_m as shown in Figure 6.7 (Lee (2004)). It comprises of a self-biased quad of MOSFET and a resistor (R_S).

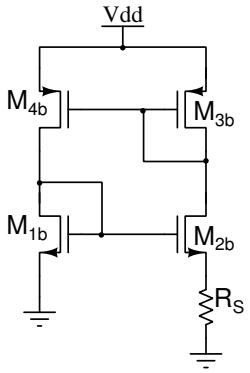


Figure 6.7: Conventional beta multiplier.

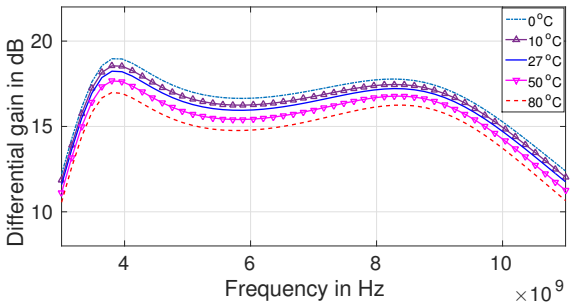


Figure 6.8: Post-layout simulations of differential gain with conventional beta multiplier.

The g_m of M_{1b} is given by

$$\begin{aligned} g_{m,1b} &= \sqrt{2\mu C_{ox}(\frac{W}{L})I_{D,1b}} \\ &= \frac{2}{R_S}(1-\frac{1}{\sqrt{K}}) \end{aligned} \tag{6.2}$$

where K is the W/L ratio between M_{2b} and M_{1b}. If R_S is constant with temperature, a stable g_m is provided for the core transistor of LNA. But practically, no resistive material provides constant value against temperature variation.

The g_m of the transistor varies over temperature due to the variation of R_S. It has been observed that, resistor has 30% variations across process corners and leads to more than 40% variations in g_m. The proposed balun LNA is analyzed with conventional beta multiplier. Figure 6.8 shows the variation of differential gain against temperature. It is observed that the maximum variation in differential gain is more than 2.5 dB (i,e., 30% variation as compared to typical value). So, we need a controllable resistance which can be used to generate a constant g_m across temperature. A controllable resistance can be generated using a MOSFET operating in a triode region. Figure 6.9a shows bias compensation circuit, where R_S is replaced with tran-

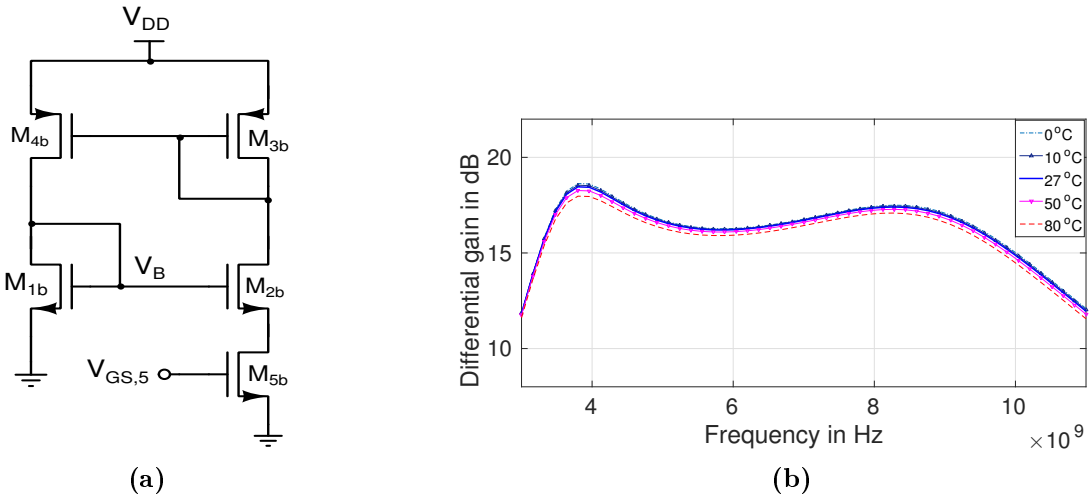


Figure 6.9: (a) Resistor-less beta multiplier (b) Post-layout simulations of differential gain with resistor-less biasing.

sistor M_{5b}. When transistor M_{5b} biased with suitable V_{GS}, it offers constant resistance against temperature. So, this leads to generate temperature invariant reference current. One added advantage of this circuit is, MOSFET resistance has less variation against process and temperature as compared to the R_S. Figure 6.9b shows the improvement in variation of gain over temperature. The maximum variation in gain is not more than 0.45 dB. Moreover, proposed bias circuit will also provide compensation against process by tuning $V_{GS,5}$. It has been observed that the change in $V_{GS,5}$ across worst-case process corners is $\pm$ 50 mV.

The resistance of a MOSFET operating in triode region can be represented by

$$R_{triode} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS,5} - V_{TH,5})} \tag{6.3}$$

Now, substituting (6.3) in (6.2) we have,

$$g_{m,1b} = \mu_n C_{ox} \frac{W}{L} V_{OV,5}(1 - \frac{1}{\sqrt{K}}) \tag{6.4}$$

In (6.4), it is observed that a specific overdrive voltage is needed to ensure MOSFET $M_{5,b}$ operates in triode region and generates the desired resistance. Furthermore, the sensitivity of gain and NF has been investigated to the inductor variations. Figure 6.10 and 6.11 shows LNA gain and NF variation for all the inductor variations presented

in balun LNA. Table 6.3 gives the maximum variations of proposed LNA. The low variations of gain and NF exonerate the proposed design.

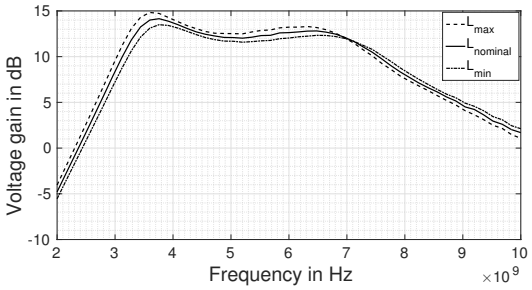


Figure 6.10: LNA gain versus inductor variations.

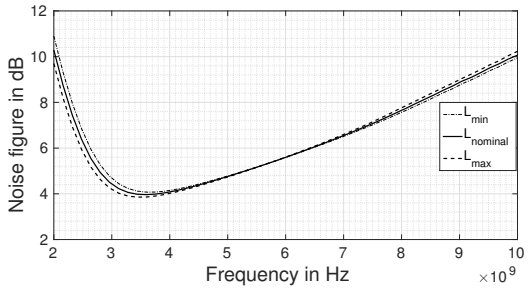


Figure 6.11: LNA NF versus inductor variations.

Table 6.3: Maximum variation of LNA gain and noise figure.

LNA Parameter	Process corners	Temperature 0°C to 80°C	Supply ±10%	Inductor variations
Δ Gain in dB	3	2.2	1.2	1.2
Δ NF in dB	1.4	1.3	0.4	0.2

6.4 Summary

A bias compensation circuit has been proposed to minimize the parameter variations of sub-threshold balun LNA. The proposed balun LNA is analyzed using both conventional and proposed bias compensation circuits. The variation of gain and NF against worst case corners are reduced by 55% and 48% as compared to conventional biasing. Monte Carlo simulations were performed, which shows the spread in differential gain and g_m is decreased by 91% and 90% respectively. A resistor-less beta multiplier is used for UWB balun LNA, where the core transistor operates in saturation region. The variation of differential gain is reduced from 2.5 dB to 0.45 dB using bias compensation. The sensitivity of proposed design has been substantiated through PVT variations. The performance of balun LNA over PVT variations shows that the proposed UWB LNA is distinguished.

Chapter 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

- A high selectivity sub-threshold balun low noise amplifier is designed for low power wearable and implantable medical devices. The worst case gain and phase error is 0.8 dB and 10° respectively. After dedicated sizing and bias optimization, the LNA is designed in a 0.18-μm CMOS technology. The layout of proposed LNA occupies 850 μm $\times$ 978 μm including buffers and bias circuit.

- A low power SD LNA using noise cancellation and current re-use techniques has been implemented for ultra wide-band applications. The proposed LNA is covering band-groups 1 and 6, which is the main corner-stone of current UWB wireless companies. The simulation results of proposed UWB LNA shows very competitive performance with lowest power consumption and better balun functioning over recently published UWB LNAs.

- A PVT compensated bias circuit is designed to minimize variations in sub-threshold LNA parameters. The variation of gain and NF against worst case corners are reduced to 55% and 48% respectively. Monte Carlo simulation (both process and mismatch) is performed for 1000 runs, which shows the standard deviation in differential gain and g_m is 2.9% and 2.4% respectively.

- A resistor-less beta multiplier is designed to reduce parameter variations of UWB LNA (core transistor operates in saturation region) against PVT.

- An inductor-less balun LNA is designed, analyzed and simulated for wide-band (0.2 - 2 GHz) to cover UHF-ISM band, digital TV and global navigation satellite system. As there is a demand for high-end devices with robustness, a PVT independent LNA is designed in UMC 0.18-μm CMOS technology. The layout of proposed LNA occupies $182\,\mu\text{m} \times 181\,\mu\text{m}$. A voltage shunt feedback and trans-conductance scaling techniques have been deployed to optimize both power and noise. A capacitor C_c is used to minimize gain and phase error at the differential output.

7.2 Scope for future study

Large signal behavior and the linearity performance of the LNA were not priories in the implementation of the proposed LNA for MedRadio communication. The linearity of the sub-threshold LNA requires further investigation to clarify the effects of circuit components on linearity of the LNA. Also, a suitable mixer topology for MedRadio communication should be designed, in order to enrich the proposed LNA. Further, the power consumption of both wide-band and multi-band LNAs can be reduced without compromising on linearity.

Nevertheless, the proposed bias compensation for UWB LNA shows better performance against VT variations, an improved circuit can be designed to reduce the variation against process corners using complementary to absolute temperature (CTAT) and constant current generator. The further noise analysis needs to be done on the proposed inductor-less LNA to estimate the noise contribution of switches.

Appendix
DERIVATIONS

A-1 Noise analysis of sub-threshold LNA

The noise at outputs (shown in Fig. 3.13d) are given by

$$v_{n,outp} = -g_{m3}(v_a - v_s)R_{P,L_{d3}} \tag{A.1}$$

$$v_{n,outm} = -g_{m4}(v_{n,outp} - v_s)R_{P,L_{d4}} \tag{A.2}$$

By applying KCL at node $'S'$, we have

$$g_{m4}(v_{n,outp} - v_s) = v_s.sC_{ac} + \frac{v_s - v_a}{R_{P,L_{d1}}} + g_{m3}(v_s - v_a) \tag{A.3}$$

Now substituting (A.1) in (A.3),

$$\begin{aligned} g_{m4}(-g_{m3}(v_a - v_s)R_{P,L_{d3}} - v_s) = v_s.sC_{ac} + \frac{v_s - v_a}{R_{P,L_{d1}}} \\ +g_{m3}(v_s - v_a) \end{aligned} \tag{A.4}$$

$$v_s(g_{m4} + sC_{ac}) = (v_a - v_s)[\frac{1}{R_{P,L_{d1}}} + g_{m3} - g_{m3}g_{m4}R_{P,L_{d3}}] \tag{A.5}$$

From (A.5),
$v_s[g_{m4} + sC_{ac} + g_{m3} + \frac{1}{R_{P,L_{d1}}} - g_{m3}g_{m4}R_{P,L_{d3}}] = v_a[g_{m3} + \frac{1}{R_{P,L1}} - g_{m3}g_{m4}R_{P,L_{d3}}]$
In the above equation, let us consider that
$x = g_{m3} + \frac{1}{R_{P,L_{d1}}} - g_{m3}g_{m4}R_{P,L_{d3}}$

Now, the further simplified expression of (A.5) is,

$$v_s[g_{m4} + sC_{ac} + x] = v_a.x \tag{A.6}$$

By substituting (3.36) in the above equation,

$$\frac{v_a(R_{P,L_{d1}} + R_{B2}) - i_{n,M_1}R_{B2}R_{P,L_{d1}}}{R_{B2}}[g_{m4} + sC_{ac} + x] = v_a.x$$

$$\Rightarrow v_a(R_{P,L_{d1}} + R_{B2}) - i_{n,M_1}R_{B2}R_{P,L_{d1}} = \frac{v_a x R_{B2}}{g_{m4} + sC_{ac} + x}$$

$$\Rightarrow v_a[R_{P,L_{d1}} + R_{B2} - \frac{xR_{B2}}{g_{m4} + sC_{ac} + x}] = i_{n,M_1}R_{B2}R_{P,L_{d1}}$$

$$\Rightarrow v_a = \frac{i_{n,M_1}R_{B2}R_{P,L_{d1}}[g_{m4} + sC_{ac} + x]}{(R_{P,L_{d1}} + R_{B2})(g_{m4} + sC_{ac} + x) - xR_{B2}} \tag{A.7}$$

In (A.7), for further simplification assume that

$$y = g_{m4} + sC_{ac} + x \tag{A.8}$$

Now, the final expression of v_a is given

$$v_a = \frac{i_{n,M_1}R_{B2}R_{P,L_{d1}}.y}{(R_{P,L_{d1}} + R_{B2})y - R_{B2}x} \tag{A.9}$$

Substituting (A.9) in (3.36), the final expression of v_s is given by

$$v_s = \frac{\frac{i_{n,M_1}R_{B2}R_{P,L_{d1}}(R_{P,L_{d1}} + R_{B2}y)}{(R_{P,L_{d1}} + R_{B2})y - R_{B2}x} - i_{n,M_1}R_{B2}R_{P,L_{d1}}}{R_{B2}} \tag{A.10}$$

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