LOW VOLTAGE, LOW POWER INTEGRATED CONTINUOUS TIME FILTERS FOR LOW FREQUENCY APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by

GOTTAM HANUMANTHA RAO

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA
SURATHKAL, MANGALORE - 575025

December 2020

DECLARATION

I hereby ***declare*** that the Research Thesis entitled **LOW VOLTAGE, LOW POWER INTEGRATED CONTINUOUS TIME FILTERS FOR LOW FREQUENCY APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

GOTTAM HANUMANTHA RAO
Reg. No. 155083/EC15FV02
Department of Electronics and
Communication Engineering.

Place: NITK-Surathkal.
Date: 11-12-2020.

CERTIFICATE

This is to certify that the Research Thesis entitled **LOW VOLTAGE, LOW POWER INTEGRATED CONTINUOUS TIME FILTERS FOR LOW FREQUENCY APPLICATIONS** submitted by **GOTTAM HANUMANTHA RAO** (Register Number: 155083EC15FV02) as the record of the research work carried out by him, is accepted as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

Dr. Rekha S.
Research Guide,
Assistant Professor,
Dept. of E&C Engg.,
NITK Surathkal - 575025.

Chairman-DRPC
(Signature with Date and Seal)

Acknowledgements

Firstly, I would like to express my sincere gratitude and deep regards to my research adviser Dr. Rekha S. for her constant guidance and support provided throughout the course of this research work. Her patience, motivation and immense knowledge made me to accomplish this. I owe my deepest gratitude to her, also for bringing this thesis in the present form. I could not have imagined having a better adviser for my Ph.D.

Besides my adviser, I express my gratitude to Prof. M. S. Bhat, Head of the department, E&C Engg. during my enrolment for Ph.D. program for his help and invaluable suggestions throughout the course of this research work. My sincere thanks to Prof. Laxminidhi T., Head, Dept. of E&C Engg. for his technical advice and constant support. Also, I thank Prof. U. Shripathi Acharya, Head, Dept. of E&C Engg. during my research work for his support and help. My sincere thanks to RPAC members, Prof. G. S. Punekar, Dept. of E&E Engg. and Prof. Laxminidhi T. for their invaluable suggestions during every step of my progress in the research work.

I take this opportunity to thank Dr. Ramesh Kini for his help during my course work and also for helping me with cadence tools. I am very grateful to Mr. Thilak for maintaining servers in VLSI lab. I also take this opportunity to thank all the faculty and staff of E&C department, NITK Surathkal. I also thank the staff in Academic, Admission and Cash sections of NITK for their assistance.

I would like to express my gratitude to all friends and colleagues at NITK for encouraging me in good and bad times making a memorable stay in NITK. Thanks to Jayaram Reddy MK, Yajunath Kaliyath and Muhammed Mansoor CB for their support and help. Special thanks to my labmates, Kiran Kumar Lad and Sreenivasulu Polineni for their help in circuit designing and in solving tool related issues. I also thank M.Tech. students-Sumit Kumar, Amaljith MK and Anuradha Patil who helped me in resolving technical issues.

I would like to thank Ministry of Electronics and Information Technology (MeitY), Govt. of India, for providing EDA tools support under SMDP-

VLSI project. Also, I express my gratitude to MeitY, for providing financial assistance under Visvesvaraya PhD Scheme for Electronics & IT (funded by Digital India Corporation).

My heartfelt thanks to my lovely wife Naga Jyothi for her support and help throughout. I recall with immense gratitude the unconditional love and support rendered by my family members and friends in my education and in my career throughout.

I am deeply indebted to all my teachers throughout the life, who have guided, encouraged and inspired me to grow in both technical and personal aspects. Finally, I would like to thank the God for giving me good health, strength and bliss during my research work. I would like to dedicate this thesis to my parents as a token of love and gratitude.

Dedicated to
My Dear Parents

Abstract

This research presents various designs of low voltage, low power continuous time filters for low frequency applications. Different filter topologies such as Transconductor-Capacitor ($G_m - C$), source follower (SF), voltage follower (VF) and log domain have been explored. UMC 180 nm and UMC 65 nm CMOS technologies are used to design these filters and simulations are carried out in Cadence Virtuoso tool.

Initial part of the thesis outlines three different proposed designs of bulk-driven transconductors (Transconductor I, II and III) operating with very low supply voltages. Transconductor I operates with a supply voltage of 0.5 V and its transconductance (G_m) can be tuned from 8 nS to 90 nS. A 2^{nd} order $G_m - C$ Butterworth low-pass filter (LPF) with cutoff frequency tunable from 74 Hz to 820 Hz is used as the test-vehicle for this Transconductor I. Transconductor II operates from a 0.8 V supply voltage. A 2^{nd} order $G_m - C$ Butterworth LPF with a cutoff frequency of 100 Hz is designed using this Transconductor II. It offers a dynamic (DR) of 55.1 dB while consuming a power of 47 nW. A low power proportional to absolute temperature (PTAT) current reference circuit is designed to make cutoff frequency of this filter independent of temperature. DR and Figure-of-Merit1 (FoM1) of these 2^{nd} order $G_m - C$ filters are comparable with many other filter designs reported in the literature. Transconductor III operates with an ultra low supply voltage of 0.3 V. A 4^{th} order $G_m - C$ Butterworth LPF is designed using Transconductor III. This filter consumes a power as low as 2.4 nW and offers a Figure-of-Merit2 (FoM2) of 6.2×10^{-15}.

Major area of filter circuits is occupied by capacitors. A simple technique to increase the time constant of a low frequency filter without using large capacitors is proposed. Using the proposed technique, 2^{nd} order SF and log domain LPFs are designed. The SF LPF offers a DR of 61.85 dB and consumes a power as low as 8 nW. The capacitance value is reduced by a factor of more than 40 times with the use of this time constant enhancement technique in the design of SF and log domain filters. In order to bias the SF LPF, a 5 nA constant current (temperature independent) reference circuit is proposed.

Further, an ultra low voltage bulk-driven VF is proposed. This VF architecture makes it possible to realize a fully differential circuit without the need of explicit common mode feed back (CMFB) circuit. A 4^{th} order LPF with cutoff frequency tunable from 50 Hz to 250 Hz is designed using this bulk-driven VF. The filter achieves the lowest FoM2 among the low frequency nW-class filter designs. The functionality of this VF LPF is demonstrated by testing an ECG signal.

The thesis also proposes a couple of designs of PTAT current reference circuits. A 0.8 V current reference circuit with improved supply voltage sensitivity is designed to generate a 5 nA current. In addition, a 1 nA switched capacitor based PTAT current reference circuit is designed with a supply voltage of 0.5 V.

Keywords: Low voltage; Low power; Bulk-driven; $G_m - C$ filter; Subthreshold region; Source follower; Voltage follower; Log domain filter; Time constant enhancement; PTAT current.

Contents

List of Figures

List of Tables

Abbreviations

$G_m - C$	Transconductor-Capacitor
Op-amp	Operational amplifier
OTA	Operational transconductance amplifier
CT	Continuous time
SC	Switched capacitor
SoC	System-on-chip
IC	Integrated circuit
EOG	Electrooculogram
EMG	Electromyogram
EEG	Electroencephalogram
ECG	Electrocardiogram
UMC	United Microelectronics Corporation
MOSFET	Metal oxide semiconductor field Effect transistor
CMOS	Complementary metal oxide semiconductor
NMOS	N-Channel metal oxide semiconductor
PMOS	P-Channel metal oxide semiconductor
LPF	Low-pass filter
BPF	Band-pass filter
HPF	high-pass filter
SF	Source follower
CMFB	Common mode feedback
UGB	Unity gain frequency
IRN	Input referred noise
THD	Total harmonic distortion
HD_2	Second harmonic distortion
HD_3	Third harmonic distortion
DR	Dynamic range
FoM	Figure of merit
PVT	Process, voltage and temperature

.

Notations

L	Channel length of the MOSFET
W	Channel width of the MOSFET
C_{ox}	Gate oxide capacitance per unit area
C	Capacitor
R	Resistor
V_{dd}	Supply voltage
V_{DS}	Drain-source voltage of the MOSFET
V_{BS}	Bulk-source voltage of the MOSFET
V_{GS}	Gate-source voltage of the MOSFET
V_{th}	Threshold voltage of the MOSFET
q	Electronic charge
k	Boltzmann constant
T	Absolute temperature
V_T	Voltage equivalent of temperature or thermal voltage
τ	Time constant
f_o	Cutoff frequency
f_p	Pole frequency
f_{-3dB}	-3dB cutoff frequency
μ	Mean
σ	Standard deviation
g_{mb}	Bulk transconductance
g_m	Gate transconductance
η	Sub-threshold slope factor

.

Chapter 1

INTRODUCTION

1.1 Motivation

The demand for battery operated wearable and implantable medical devices is increasing enormously for long term and continuous health monitoring. These devices are realized through integrated circuits (ICs) to perform various functions, including processing of biological signals. Major requirements of these devices are low power to increase the battery life and small size for better portability. Biological signals such as electrocardiogram (ECG), electroencephalogram (EEG), electromyogram (EMG), electrooculogram (EOG) etc., are small signals of low frequency, as shown in Table 1.1. Typical frequency range of these signals is approximately 10 mHz to 10 kHz (Webster 2009).

Table 1.1: Representative biological signals

Signal	Frequency Range (Hz)	Amplitude (mV)
ECG	0.01 - 250	0.5 - 4
EEG	0 - 150	0.005 - 0.3
EMG	0 - 10 k	0.1 - 5
EOG	0 - 50	0.05 - 3.5

A typical data acquisition system for biological signals is shown in Figure 1.1 (Solís-Bustos *et al.* 2000). The transducer converts biological signal into an equivalent electrical signal. Analog pre-processing blocks (pre-amplifier and continuous time filter) enhance the quality of the desired signal by reducing unwanted noise. The pre-

amplifier amplifies the electrical signal to a higher level. Continuous time (CT) filter is an essential building block to limit the frequency band and to eliminate the out of band noise. Further processing is normally done in digital domain.

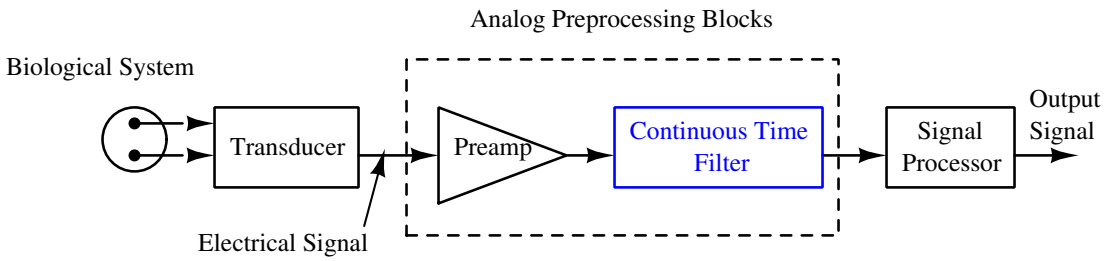


Figure 1.1: A general purpose biological data acquisition system

This research focuses on the design of CT filters for front-end processing of biological signals. Main design challenges of these filters are low voltage, low power and less silicon area as explained below.

- The technology scaling necessitates ICs to operate with low voltage to reduce the chip power density and increase the reliability. The supply voltage scaling is demanded by digital circuits as their dynamic power is proportional to square of the supply voltage. As the analog circuit blocks co-exist with digital blocks in a typical System-on-chip (SoC), they are also forced to work with low power supply. However, supply voltage scaling in analog circuits adversely affects the signal swing and dynamic range (DR). In order to process the biomedical signals, such as ECG and EEG, the filter should have a DR of 44 dB (Thanapitak and Sawigun 2018) and 40 dB (Krishna and Laxminidhi 2018) respectively. It is really a challenging task to design filters with DR $\geq$ 45 dB under low voltage conditions.

- In order to increase the battery life of implantable/portable medical devices and to conform to the safety aspects of human body, the power consumption of every building block of the system should be reduced as much as possible. To reduce the power consumption, MOS transistors in a circuit are operated in weak-inversion or sub-threshold region at very low bias currents (in the range of a few nAs down to a few tens of pAs) (Sawigun and Serdijn 2016). However,

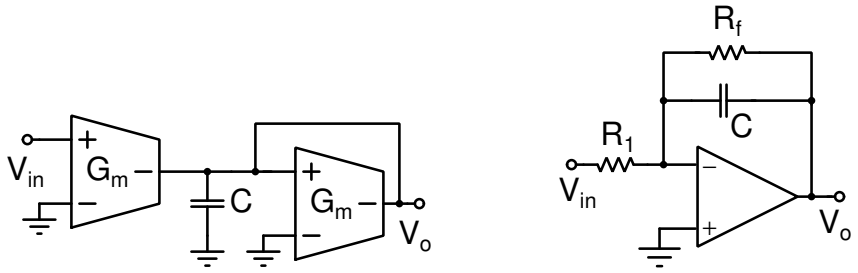
operating transistors in weak-inversion region with very low bias currents reduces the linearity of the circuit (Enz *et al.* 1995).

- As the biological signals are of low frequency, it is mandatory to design such filters with low cutoff frequency (large time constant). Large capacitors and large resistors are required to design filters with such large time constant, resulting in area overhead.

Designing CT filters with desired performance parameters, under the influence of above mentioned issues is quite challenging. Any further improvement in the low frequency filter design for low voltage operation either in terms of power or DR or area efficiency can be a significant contribution to the field of analog circuits. This research is the result of the efforts in this direction for realizing CT filters.

1.2 Basic Filter Topologies

Transconductor-Capacitor ($G_m - C$) and active-RC are the two basic approaches followed for realizing CT filters. Figure 1.2a shows 1^{st} order $G_m - C$ filter whose transfer



(a) $G_m - C$ **(b)** Active-RC

Figure 1.2: First order filters.

function and cutoff frequency are given by (1.1) and (1.2) respectively.

$$H(s) = \frac{-1}{1 + \frac{sC}{G_m}} \tag{1.1}$$

$$f_o = \frac{G_m}{2\pi C} \tag{1.2}$$

Figure 1.2b shows 1^{st} order active-RC filter whose transfer function and cutoff frequency are given by (1.3) and (1.4) respectively.

$$H(s) = \frac{-R_f/R_1}{1 + sR_fC} \tag{1.3}$$

$$f_o = \frac{1}{2\pi R_fC} \tag{1.4}$$

For a given power dissipation, active-RC filters are more linear when compared to $G_m - C$ filters because of their negative feedback structure. Cutoff frequency can be easily tuned in $G_m - C$ filters. To design active-RC filters with low cutoff frequencies, the resistor and capacitor should be very large. These large resistors and capacitors occupy more area on the chip. Also, very high gain operational amplifiers (op-amps) or operational transconductance amplifiers (OTAs) which consume lot of power are required to design active-RC filters. To design $G_m - C$ filters with low cutoff frequencies, either G_m should be low or capacitor should be large. Low G_m can be achieved by operating the transistors in sub-threshold region with currents in the range of a few nAs or by using G_m reduction techniques. Hence, $G_m - C$ filters are preferred over active-RC counterparts for low frequency applications.

In order to design compact and power-efficient filters, the recent trend is to replace transconductors in a $G_m - C$ topology with single MOSFETs (Sawigun and Thanapitak 2018). These type of filters are called as single branch filters. Source followers (SFs) and voltage followers (VFs) are widely used to implement these single branch filters.

Alternatively, log-companding (Adams 1979) is another approach to design low voltage and low power CT filters. Filters designed using this approach are called as log domain filters. The principle of log domain filter is shown in Figure 1.3. Here, input current signal (I_{in}) is converted to a compressed voltage signal (v_{in}) by using log function. This compressed voltage signal is processed through non-linear filter and converted back to current signal (I_{out}) by using exponential function. Hence, log domain filters are internally nonlinear and externally linear. As the magnitude of compressed voltage signals (v_{in} & v_{out}) is far less than the DC biasing voltage, the internal circuit need not be linearized. The input current signal can be as large as the DC bias current. This improves the signal swing and hence the DR.

Log domain filters are designed using MOS transistors biased in the sub-threshold

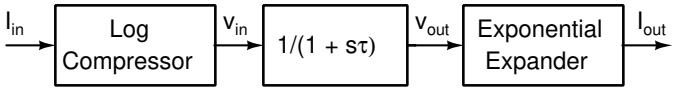


Figure 1.3: Principle of log domain filter

(weak-inversion) region in which current-voltage characteristics are exponential.

1.3 Prior Work

The literature explains few circuit techniques for designing low frequency active-RC filters. Low frequency $G_m - C$ filters, on the other hand, demand techniques to reduce G_m. Many such designs can be found in the literature as well. In addition to these, source follower (SF) and voltage follower (VF) based designs and log domain filter designs are also discussed in the literature.

Simple active-RC filters are generally not preferred for low power, low frequency applications as explained in section 1.2. However, by using current steering technique or by using pseudo resistors, low frequency active-RC filters can be designed.

A 1^{st} order active-RC LPF using current steering technique is shown in Figure 1.4 (Wong *et al.* 2005). A small fraction of input current (I_{D1}) is flowing through M_1 to charge and discharge the output capacitor (C_f) and most of the current (I_{D2}) is bypassed through M_2. Thus, the cutoff frequency can be reduced, compared to traditional active-RC filters, without employing very large capacitors and resistors.

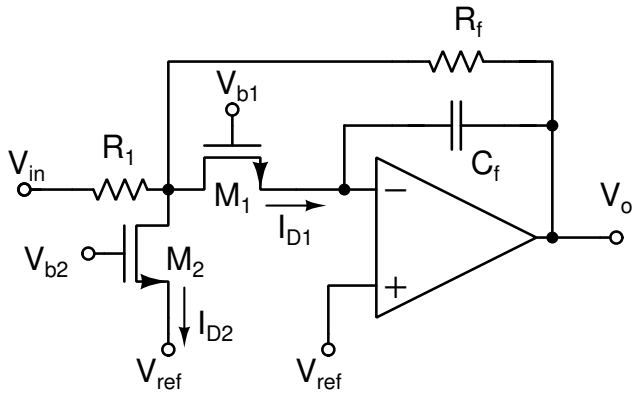


Figure 1.4: Current Steering

Transistors M_1 and M_2 are operating in triode region and act as resistors. The cutoff frequency of the filter can be tuned by varying V_{b1} or V_{b2}. M_1 and M_2 intro-

duce non-linearity as they are operating in triode region. The transfer function and the cutoff frequency of the circuit shown in Figure 1.4 are given by (1.5) and (1.6) respectively.

$$H(s) = \frac{-R_f/R_1}{1 + s\frac{R_f C_f}{\alpha}} \tag{1.5}$$

$$f_o = \frac{\alpha}{2\pi R_f C_f} \tag{1.6}$$

where $\alpha = \frac{I_{D1}}{I_{D2}} \ll 1$.

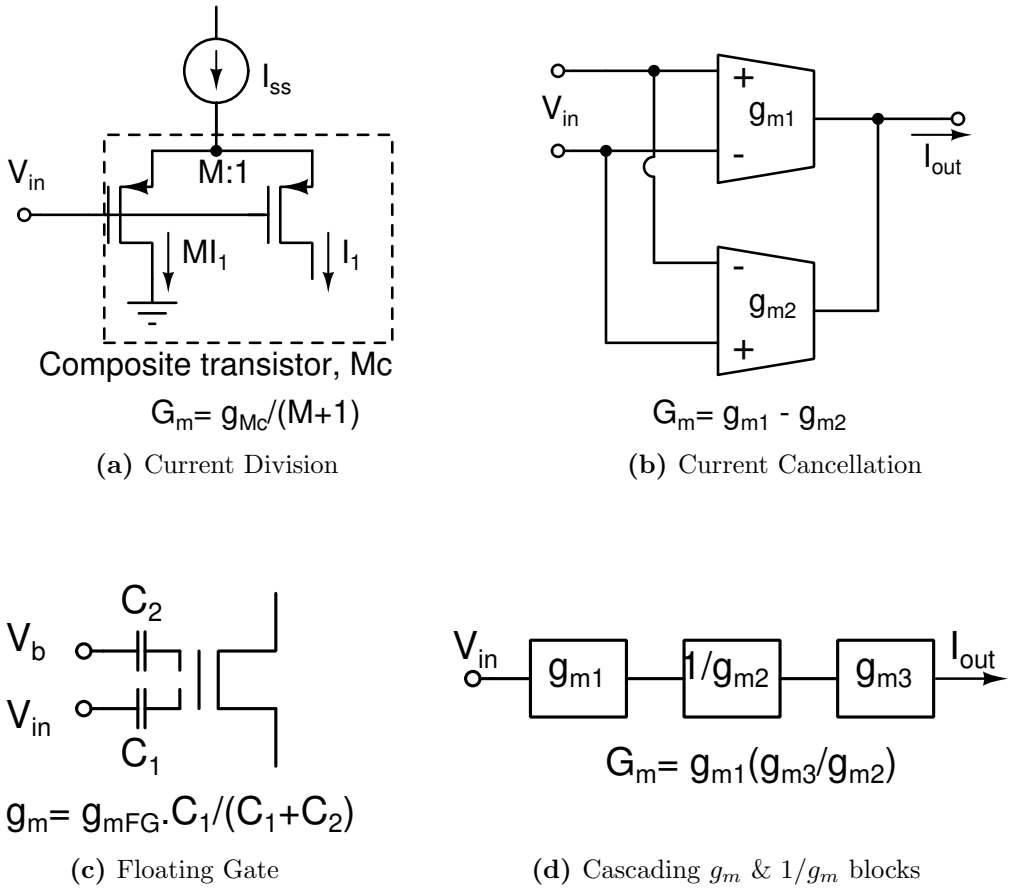
By using current steering technique, a low-pass filter (LPF) with cutoff frequency of 18 Hz and a high-pass filter (HPF) with cutoff frequency of 5 mHz are implemented in (Wong *et al.* 2005) and (Li *et al.* 2012) respectively. However, the power consumption of these circuits is on the higher side.

A resistance of the order of giga ohms can be realized through a MOSFET operating in weak-inversion triode region. This resistor is called as pseudo resistor. Resistance value can be controlled by varying V_{GS} of the transistor. Pseudo resistor based active-RC low frequency filters are implemented in (Shiue *et al.* 2011, Tajalli and Leblebici 2012). The main drawback of the pseudo resistor is that for a small change in control voltage (V_{GS}), the resistance value changes by a large value, which in turn changes the cutoff frequency of the filter. Hence both methods have their own limitations.

To design $G_m - C$ filters with low cutoff frequencies, either G_m should be low or capacitor should be large. Large capacitors occupy more area on the chip. A large equivalent capacitance can be achieved in a small chip area by using capacitor multiplier or impedance scaler circuits (Martínez and Vazquez-Gonzalez 1998, Solís-Bustos *et al.* 2000, Doménech-Asensi *et al.* 2014). But these circuits produce extra noise and unwanted poles. Reducing G_m is the better option compared to impedance scaler circuits. Some of the G_m reduction techniques (Veeravalli *et al.* 2002) found in the literature are outlined here.

- Current Division (CD)
- Current Cancellation (CC)
- Floating Gate (FG)
- Cascading transconductance and transimpedance amplifiers

- Bulk-Driven



(a) Current Division **(b)** Current Cancellation

(c) Floating Gate **(d)** Cascading g_m & $1/g_m$ blocks

Figure 1.5: G_m reduction techniques.

Figures 1.5a and 1.5b show the concepts of CD and CC techniques respectively. In CD technique, a small amount of current (I_1) is flowing to output and most of the current (MI_1) is bypassed to the ground, resulting in reduced G_m. In CC technique, two transconductors are connected in parallel to get a reduced G_m of $g_{m1} - g_{m2}$. Both CD and CC techniques consume more power. The combination of these two techniques with source degeneration can be used to reduce G_m further.

Floating-gate technique (shown in Figure 1.5c) (Yu and Geiger 1993, Veeravalli *et al.* 2002) has a natural attenuation due to the voltage division at the input capacitors. Hence, it is a natural choice for obtaining small G_m. CD and CC techniques can be implemented with FG transistors to further reduce G_m. Major drawbacks of the FG technique are increased area and additional process steps. G_m can be re-

duced by cascading transconductance and transimpedance amplifiers (g_m and $1/g_m$) as shown in Figure 1.5d (Yodprasit and Ngarmnil 1998). However, these additional blocks consume extra power.

In (Silva-Martinez and Salcedo-Suñer 1997), an OTA using CD and CC techniques is proposed. A third order LPF with cutoff frequency of 10 Hz is implemented with the designed OTA. The DR of the filter is 62 dB, but the power consumption is 15 μW. A sixth order LPF with cutoff frequency of 2.4 Hz for medical applications is implemented in (Solís-Bustos *et al.* 2000). In this design, CD and CC techniques along with impedance scaler circuit are used. The DR of the filter is 60 dB and the power consumption is 10 μW, which is considered to be large.

Bulk-driven technique is found to be useful for the design of low voltage and low power analog circuits (Guzinski *et al.* 1987). Here, the signal is applied to the bulk terminal of MOSFET and biasing is done through the gate terminal of the device. Advantage of bulk driven device over gate driven device is that it is not necessary to spend a part of the input voltage to turn the device on. This improves the input signal swing and hence the DR. The expression for bulk-transconductance (g_{mb}) in sub-threshold region is given by

$$g_{mb} = (\eta - 1)g_m = \frac{(\eta - 1)I_D}{\eta V_T} \tag{1.7}$$

where g_m, V_T and η are the gate-transconductance, thermal voltage and sub-threshold slope factor respectively. Typical value of η lies between 1.2 and 1.4 (Veeravalli *et al.* 2002). g_{mb} is typically around 0.2 - 0.4 times g_m. Due to their lower transconductance and compatibility with low voltage operation, bulk-driven transistors operating in sub-threshold region can be used to design low frequency filters.

Design of continuous time filters with power supply voltage of 0.5 V using bulk-driven technique is described in (Chatterjee *et al.* 2005). A 0.5 V CMOS inverter based tunable transconductor is proposed in (Vlassis 2012). A tunable 0.8 V class-AB bulk-driven transconductor is proposed in (Yodtean and Thanachayanont 2013) and an LPF with cutoff frequency tunable from 2.5 kHz to 12.5 kHz is designed with the proposed transconductor. The filter offers a DR of 67.4 dB and consumes a power of 34.4 μW.

Recently, 0.3 V and 0.25 V bulk-driven OTAs are reported in (Veldandi and Shaik 2018, Khateb *et al.* 2019) and (Ferreira and Sonkusale 2014, Akbari and Hashemipour

2017) respectively. However, these OTAs are designed to target very high DC gain and no significant low frequency filters are implemented using them.

Single branch low frequency filters based on SF and VF have become popular of late due to their compactness and power efficiency. The internal negative feedback available in SF and VF filters makes them more linear compared to simple $G_m - C$ filters (Zhang *et al.* 2013, Sawigun *et al.* 2012). In (Sawigun *et al.* 2014), a 4^{th} order BPF is realized by cascading SF bi-quads. In a similar fashion, 4^{th} order LPFs using flipped VFs for ECG signal processing are reported in (Sawigun and Thanapitak 2018, Sawigun and Thanapitak 2019). A 4^{th} order, sub-threshold buffer based LPF is presented in (Thanapitak and Sawigun 2018). All these designs employ supply voltage of 0.5 V or higher.

Along with the above mentioned filter designs, log domain filters are also found useful for low frequency applications. The idea of log domain filtering is first introduced in (Adams 1979) and thoroughly investigated in (Seevinck 1990, Frey 1993, Seevinck *et al.* 2000). In (Gerosa *et al.* 2004, La Croz-Blas *et al.* 2005, Zhang *et al.* 2017), low frequency log domain filters are implemented for biomedical applications. However, these filters employed very large capacitors, which occupy more area on the chip. In (Tsirimokou and Psychalinos 2014), a current mirror based filter of cutoff frequency of 9.6 Hz is proposed, where the current signal is linearly compressed along with DC current to increase the time constant. However, a large capacitance of 47.1 pF is used in this design. A second order sinh domain filter with 6.3 Hz cutoff frequency is proposed in (Kafe and Psychalinos 2014), which uses a capacitance as high as 190.28 pF.

1.4 Thesis Contributions

It is inferred from the above literature survey that bulk-driven transistors are more compatible with low voltage operation and offer lower transconductance (compared to gate transconductance), which are the major requirements for the design of low frequency filters. Hence, bulk-driven transistors operating in sub-threshold region are used in a couple of proposed designs in this thesis. It is also inferred that by suitably modifying the designs, SF, VF and log domain structures can be used to build low frequency filters with optimized power and area. Thus, an attempt is made in this work to design low frequency filters with low voltage ($\leq$ 0.8 V), low power (of the

order of nW), good DR ($\geq$ 45 dB) and less area.

Three designs of bulk-driven transconductors operating with supply voltages 0.3 V, 0.5 V and 0.8 V are proposed. To test the performance of these proposed designs, 2^{nd} order $G_m - C$ Butterworth LPFs are designed from 0.5 V and 0.8 V transconductors. A 4^{th} order $G_m - C$ Butterworth LPF is designed using the 0.3 V transconductor. DR and Figure-of-Merit1 (FoM1) (refer A.8) of all these filters are comparable with many other filter designs reported in the literature.

In addition, a simple technique to increase the time constant of a filter without using large capacitors is proposed. This technique reduces the capacitor value significantly in the design of low frequency filters and hence saves the area of the circuit. Using this technique, 2^{nd} order SF and log domain LPFs are designed. These filters use the lowest capacitance/pole among the similar designs given in the literature. A 0.3 V bulk-driven VF is proposed and a 4^{th} order LPF with cutoff frequency tunable from 50 Hz to 250 Hz is designed by cascading the proposed bulk-driven VFs. This 4^{th} order VF LPF offers the lowest Figure-of-Merit2 (FoM2) (refer A.9) compared to the state-of-the-art low frequency filters.

Current reference circuits are required for biasing filter circuits. The $G_m - C$ filters designed in this work require proportional to absolute temperature (PTAT) current to make cutoff frequency independent of the temperature, whereas the proposed SF and log domain filters require a constant current. Both PTAT and constant current reference circuits operating with supply voltages of 0.5 V and 0.8 V are designed for biasing the filter circuits.

Transistors in all the above mentioned proposed circuits are operated in subthreshold region with current in the range of a few nAs to reduce G_m as well as power consumption. All the circuits are designed and simulated using Cadence Virtuoso tool. To check the robustness of these proposed designs, Monte Carlo simulations (for process variations and device mismatch) and simulations across Process, Voltage and Temperature (PVT) variations are performed. All the designs are found to be robust across these variations.

1.5 Thesis Organization

The rest of the thesis is organized as follows.

- In chapter 2, three different designs of bulk-driven transconductors operating

with different supply voltages 0.3 V, 0.5 V and 0.8 V are proposed. 2^{nd} order $G_m - C$ Butterworth LPFs are designed using each of 0.5 V and 0.8 V transconductors. A 4^{th} order $G_m - C$ Butterworth LPF is designed using 0.3 V transconductor.

- In chapter 3, an area efficient time constant enhancement technique for filter design without using large capacitors is proposed. A 2^{nd} order SF LPF is designed using the proposed technique. Further, this chapter also discusses the design of a 4^{th} order bulk-driven VF LPF.

- Chapter 4 presents the design of an area efficient log domain filter using the time constant enhancement technique proposed in chapter 3.

- Chapter 5 presents a PTAT current reference circuit with improved supply voltage sensitivity and a switched-capacitor (SC) PTAT current reference circuit.

- Conclusions and future directions are given in chapter 6.

Chapter 2

DESIGN OF $G_m - C$ FILTERS USING BULK-DRIVEN TRANSCONDUCTORS

Low voltage and low power transconductors with low G_m are required to design low frequency $G_m - C$ filters. Due to their lower G_m and compatibility with low supply voltages, bulk-driven input transistors operating in sub-threshold region are used in the design of transconductors presented in this chapter.

Three different designs of bulk-driven transconductors (Transconductor I, II and III) are proposed. By using Transconductor I, a 2^{nd} order Butterworth LPF with cutoff frequency tunable from 74 Hz to 820 Hz is designed in UMC 180 nm CMOS technology with 0.5 V supply. Transconductor I suffers from leakage currents at higher temperatures ($> 50°$C) and this leads to deviation in parameters of the filter. To overcome this leakage current problem, Transconductor II is designed in UMC 65 nm LL (low-leakage) technology and Transconductor III is designed in UMC 180 nm with an ultra low supply voltage of 0.3 V.

By using Transconductor II, a 2^{nd} order Butterworth LPF with 100 Hz cutoff frequency is implemented in UMC 65 nm CMOS technology with 0.8 V supply. Along with Transconductor II, a low power PTAT current reference circuit is designed to make G_m independent of temperature. By using Transconductor III, a 4^{th} order Butterworth LPF with a tunable cutoff frequency from 50 Hz to 250 Hz is implemented in UMC 180 nm CMOS technology.

2.1 Transconductor I

The proposed Transconductor I is shown in Figure 2.1a. Input transistor M_1 is biased by a constant current of 10 nA that is mirrored by constant current source, I_{DC}. M_2 mirrors the current, I_{in} to M_3 through Variable Gain Current Mirror (VGCM) (Yodtean and Thanachayanont 2013) with a current gain of K.

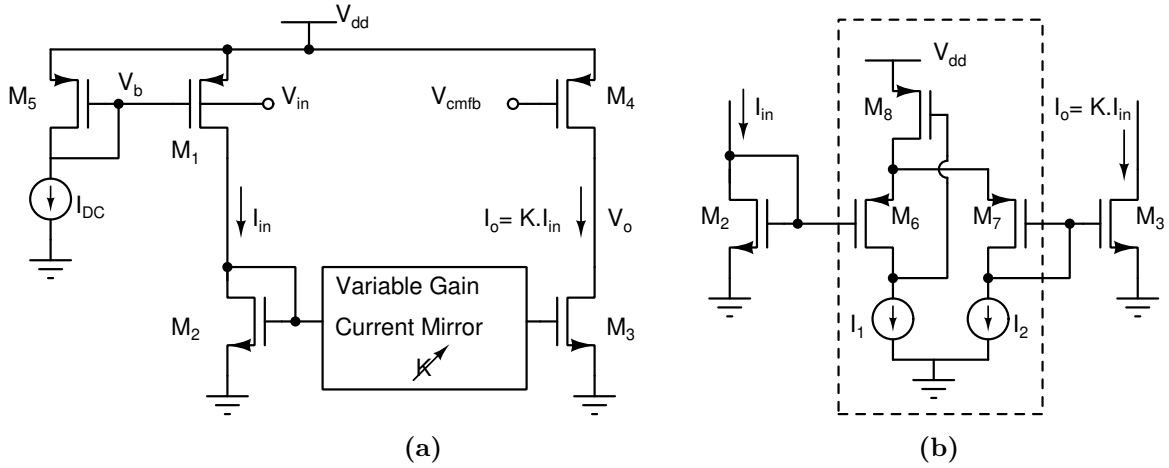


Figure 2.1: (a) Transconductor I, (b) VGCM.

The VGCM circuit is shown in Figure 2.1b. The currents I_1 and I_2 are generated from a reference current source (not shown in Figure). M_2, M_3, M_6 and M_7 form a trans-linear loop (Yodtean and Thanachayanont 2013) and the relation among the gate-source voltages of them can be expressed as in (2.1).

$$V_{GS2} + V_{SG6} = V_{SG7} + V_{GS3} \tag{2.1}$$

Drain current equations of NMOS and PMOS transistors operating in weak-inversion saturation region are given by (2.2) and (2.3) respectively (refer A.2).

$$I_{Dn} = I_{Dn0}(\frac{W}{L})_n e^{\frac{V_{GSn}-V_{tn}}{\eta V_T}} \tag{2.2}$$

$$I_{Dp} = I_{Dp0}(\frac{W}{L})_p e^{\frac{V_{SGp}-|V_{tp}|}{\eta V_T}} \tag{2.3}$$

From equations (2.2) and (2.3), V_{GSn} and V_{SGp} can be derived as in (2.4) and (2.5)

respectively.

$$V_{GSn} = \eta V_T \ln \left[\frac{I_{Dn}}{I_{Dn0}(\frac{W}{L})_n}\right] + V_{tn} \tag{2.4}$$

$$V_{SGp} = \eta V_T \ln \left[\frac{I_{Dp}}{I_{Dp0}(\frac{W}{L})_p}\right] + \mid V_{tp} \mid \tag{2.5}$$

It is assumed that M_2 & M_3 have equal threshold voltages and M_6 & M_7 have equal threshold voltages. It is also assumed that both nMOS and pMOS have same η value. By substituting (2.4) and (2.5) in (2.1), the relationship among the currents I_{in}, I_o, I_1 and I_2 can be derived as in (2.6)

$$I_o = K.I_{in} \tag{2.6}$$

where $K = \frac{I_1}{I_2}$ is the current gain.

When $I_1 = I_2$, the current gain is 1 as $V_{SG6} = V_{SG7}$, $V_{GS2} = V_{GS3}$. When $I_1 > I_2$, the current gain is >1 as $V_{SG6} > V_{SG7}$, $V_{GS2} < V_{GS3}$. When $I_1 < I_2$, the reverse is true and the current gain is <1. Therefore the output current of the transconductor can be scaled by varying the current I_1 or I_2.

Fully differential configuration of the Transconductor I is shown in Figure 2.2. Input transistors M_1 and M_2 are biased by using a current source of 10 nA (not shown in the Figure). M_5-M_{10} and current sources I_1, I_2 form VGCM circuit. C_c is used as compensating capacitor to improve the phase margin. The output differential current (i_{od}) is given by

$$i_{od} = K.g_{mb}.v_{id} \tag{2.7}$$

where $i_{od} = i_{op} - i_{om}$, g_{mb} is the bulk transconductance of the input transistor M_1 or M_2 and $v_{id} = v_{ip} - v_{im}$ is the input differential voltage. Therefore, the effective transconductance, G_m is given by

$$G_m = K.g_{mb} \tag{2.8}$$

The voltage gain of the transconductor is given by

$$A_v = K.g_{mb}.(r_{11} \parallel r_{13}) \tag{2.9}$$

where r_{11} and r_{13} are small signal output resistances of M_{11} and M_{13} respectively.

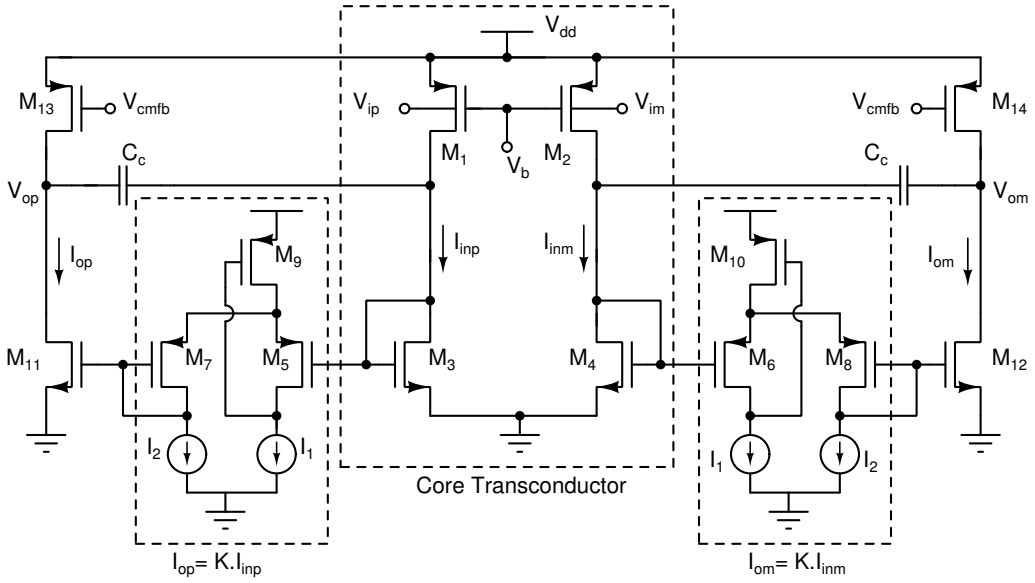
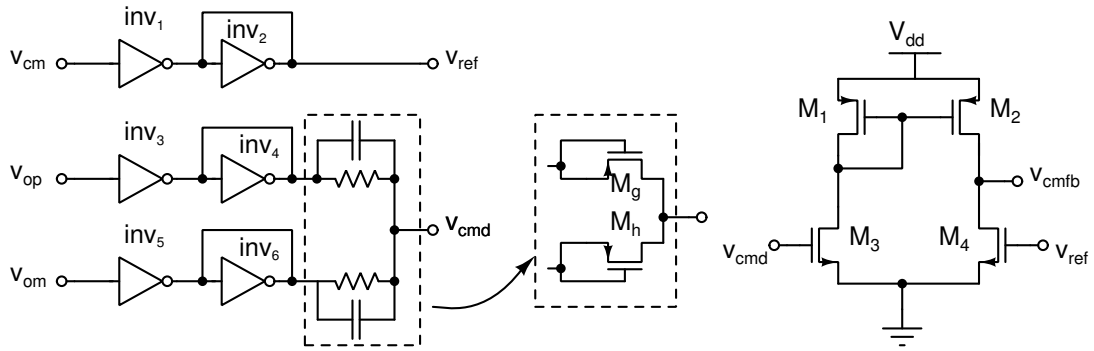


Figure 2.2: Fully differential configuration of the Transconductor I.

The transconductor operates with a supply voltage of 0.5 V and the input common mode voltage ($V_{in,cm}$) is fixed at 0.25 V. Gates of M_{13} and M_{14} are biased with a common mode feedback voltage (V_{cmfb}) which sets the output common mode voltage ($V_{o,cm}$) to 0.25 V. The CMFB circuit proposed in (Rekha and Laxminidhi 2016) (Figure 2.3) is used in this work. In Figure 2.3a, inverters 3 to 6 along with transistors M_g and M_h form the common mode detector. Inverters 3 and 5 sense the output voltages of the transconductor. Inverters 4 and 6 have their outputs shorted to inputs. This arrangement reduces the gain of sensing inverters, thus enhancing the linearity of the sensing inverters and entire CMFB circuit. Transistors M_g and M_h are connected such that they offer high resistance along with a capacitor. This arrangement gives the average (V_{cmd}) of the sensed output voltages of the transconductor. V_{ref} is generated from V_{cm} using the inverters 1 and 2. V_{cmd} is compared with V_{ref} using a simple error amplifier shown in Figure 2.3b. The error amplifier output voltage, V_{cmfb} is fed back to the transconductor to set the $V_{o,cm}$ to 0.25 V. The total power consumption of the CMFB circuit is 40 nW.

2.1.1 Simulation Results

G_m is found to be 48 nS for $I_1 = I_2 = 10$ nA. It can be tuned by varying I_1 and I_2. This varies the current gain, K and hence G_m. The simulated G_m against the input



(a) Common mode detector **(b)** Error amplifier

Figure 2.3: CMFB circuit for the Transconductor I.

differential voltage for different I_1 values is shown in Figure 2.4. G_m is tuned from 8 nS to 90 nS by fixing I_2 at 10 nA and varying I_1 from 2 nA to 18 nA in steps of 4 nA. It is observed from Figure 2.4 that equal increments in I_1, give equal increment in G_m. Hence, the G_m is linearly tuned by varying I_1.

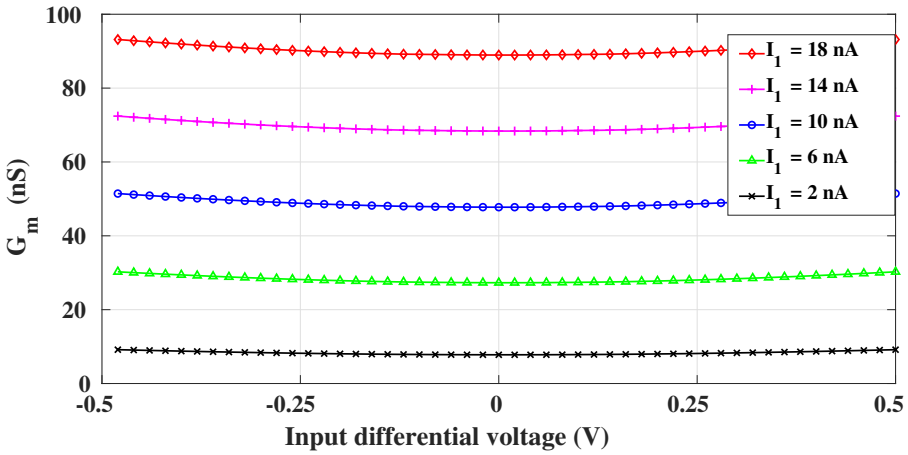


Figure 2.4: G_m tuning.

The magnitude and phase responses of the transconductor are shown in Figures 2.5a and 2.5b respectively. Transconductor provides an open loop DC gain of 28 dB and a unity gain frequency (UGB) of 3.7 kHz under no load condition. The phase margin is 83°. Table 2.1 lists the parameters of the proposed transconductor.

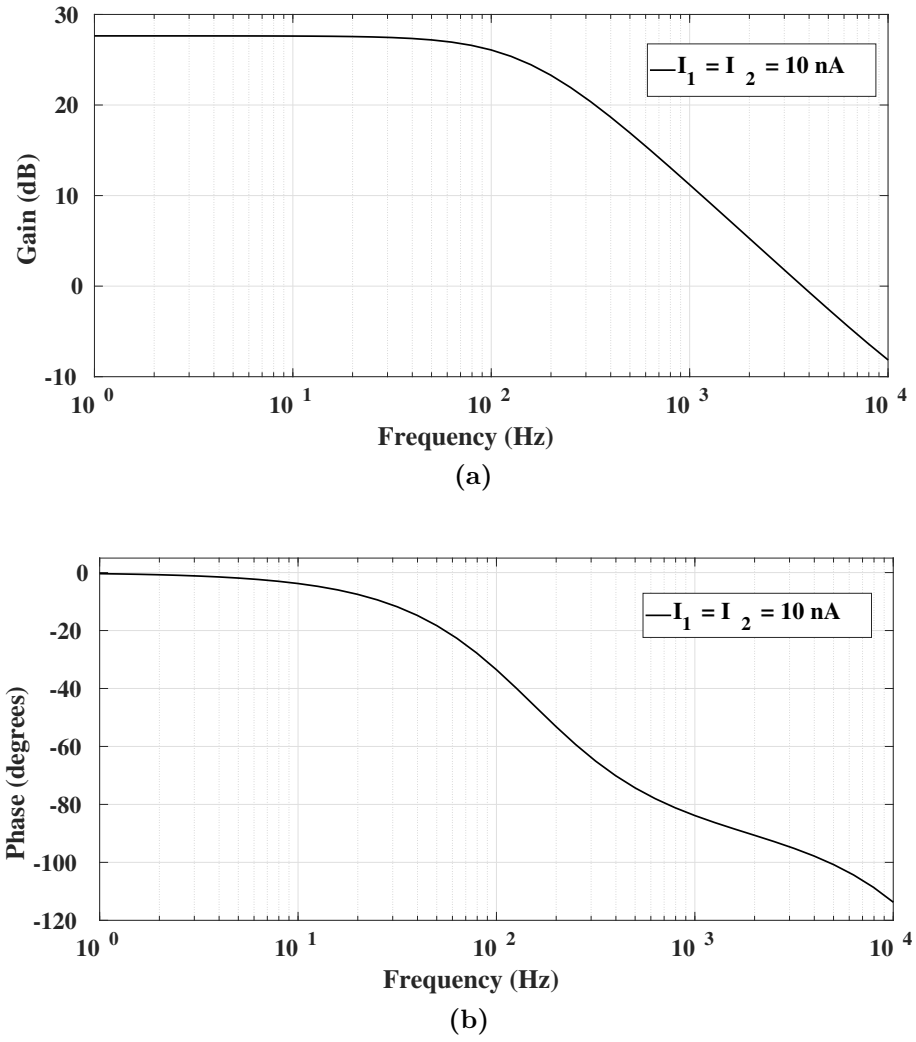


Figure 2.5: (a) Magnitude, (b) Phase responses of the Transconductor I.

2.1.1.1 G_m variation with process corners & temperature

Simulations are carried out to observe the effect of process corners (tt, ff, ss, fnsp and snfp) and temperature on G_m. The variation in G_m is found to be $< 1\%$ across all the corners. The variation in G_m is found to be ± 6.3 % for a temperature range of 0-70°C as shown in Table 2.2. It is observed that as the temperature increases, G_m decreases. This variation in G_m can be compensated by using a constant-G_m bias circuit or by biasing the transconductor with PTAT current reference.

Table 2.1: Parameters of Transconductor I.

Parameter	**Simulated values** (Schematic)
Technology	0.18 μm
V_{dd}	0.5 V
G_m	8 - 90 nS
DC Gain	28 dB
UGB	3.7 kHz
Phase margin	83°
IRN (40 Hz - 4 kHz)	47 μV RMS
Power(nW)	86 nW†

† At $I_1 = I_2 = 10$ nA, including CMFB circuit.

Table 2.2: G_m variation with temperature

Temperature (^0C)	0	27	50	70
$\boldsymbol{G_m}$ **(nS)**	50	48	46	44.6

2.2 LPF Realization Using Transconductor I

Figure 2.6 shows a standard fully differential $G_m - C$ biquad (Schaumann *et al.* 2009). It gives a 2^{nd} order LPF characteristics at V_{op} (or V_{om}). Transfer function of this 2^{nd}

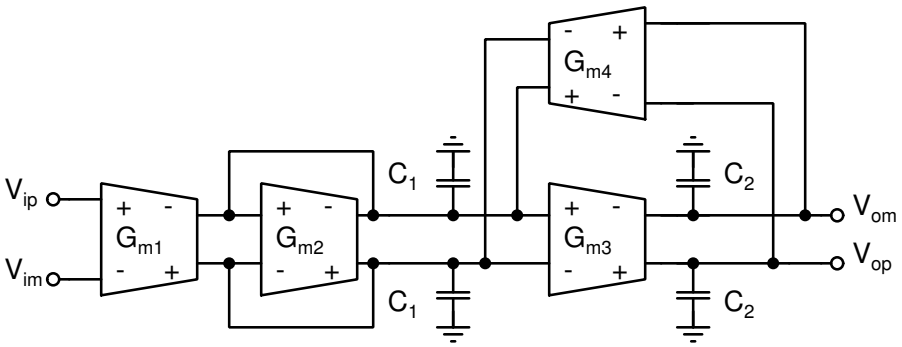


Figure 2.6: $G_m - C$ biquad

order LPF can be derived as in (2.10).

$$H(s) = \frac{G_{m1}/G_{m4}}{(s^2 C_1 C_2/G_{m3}G_{m4}) + (sG_{m2}C_2/G_{m3}G_{m4}) + 1} \tag{2.10}$$

Transfer function of the 2^{nd} order LPF prototype is given by (2.11)

$$H(s) = \frac{A_o}{(s^2/\omega_o^2) + (s/\omega_o Q) + 1} \tag{2.11}$$

By comparing (2.10) with (2.11), the expressions for DC gain, cutoff frequency and quality factor of LPF are given by (2.12), (2.13) and (2.14) respectively.

$$A_o = \frac{G_{m1}}{G_{m4}} \tag{2.12}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{G_{m3}G_{m4}}{C_1C_2}} \tag{2.13}$$

$$Q = \sqrt{\frac{C_1}{C_2}}\frac{\sqrt{G_{m3}G_{m4}}}{G_{m2}} \tag{2.14}$$

The expressions for DC gain, cutoff frequency and quality factor are modified to (2.15), (2.16) and (2.17) respectively if the input, output parasitic capacitances (C_i, C_o) and input, output conductances (g_i, g_o) of the transconductor are taken into account.

$$A_o' = \frac{G_{m1}G_{m3}}{(g_o + g_i)(G_{m2} + 2g_i + 3g_o) + G_{m3}G_{m4}} \tag{2.15}$$

$$f_o' = \frac{1}{2\pi}\sqrt{\frac{(g_o + g_i)(G_{m2} + 2g_i + 3g_o) + G_{m3}G_{m4}}{C_1'C_2'}} \tag{2.16}$$

$$Q' = \sqrt{C_1'C_2'}\frac{\sqrt{(g_o + g_i)(G_{m2} + 2g_i + 3g_o) + G_{m3}G_{m4}}}{(3g_o + 2g_i)C_2' + (g_o + g_i)C_1' + G_{m2}C_2'} \tag{2.17}$$

where, $C_1' = C_1 + 3C_o + 2C_i$ and $C_2' = C_2 + C_o + C_i$. Hence, it can be seen that when the parasitic capacitances and input/output conductances are taken into account, actual frequency response deviates from the expected one. Simulations are carried out to estimate C_i, C_o, g_i and g_o. C_o and C_i are found to be 1.67 pF and 70 fF respectively. g_i and g_o are found to be 75 pS and 2 nS respectively.

A 2^{nd} order Butterworth LPF is designed using the proposed transconductor. In this design, all transconductances are taken to be equal. C_1 and C_2 are chosen to be 10 pF and 20 pF respectively to get the quality factor of $\frac{1}{\sqrt{2}}$. Two CMFB circuits are used for this filter to maintain a common-mode voltage of 0.25 V at each node. As output nodes of G_{m1}, G_{m2} and G_{m4} blocks connected together, only one CMFB circuit is used for these blocks. Second CMFB circuit is used for the G_{m3} block.

2.2.1 Simulation Results

The cutoff frequency of the filter is 456 Hz for $I_1 = I_2 = 10$ nA as shown in Figure 2.7. Figure 2.8 shows output noise of the filter. At low frequencies it is dominated by flicker $(1/f)$ noise, around the cutoff frequency thermal noise dominates and it follows the filter response at higher frequencies. The total input-referred noise (IRN) integrated over the frequency range 5-500 Hz is 160 μV_{RMS}. A sinusoidal input signal of frequency 100 Hz is applied to measure the total harmonic distortion (THD) of the filter. THD of the output differential signal is found to be -40 dB for an input differential peak-peak voltage of 180 mV. DR of the filter is calculated to be 52 dB.

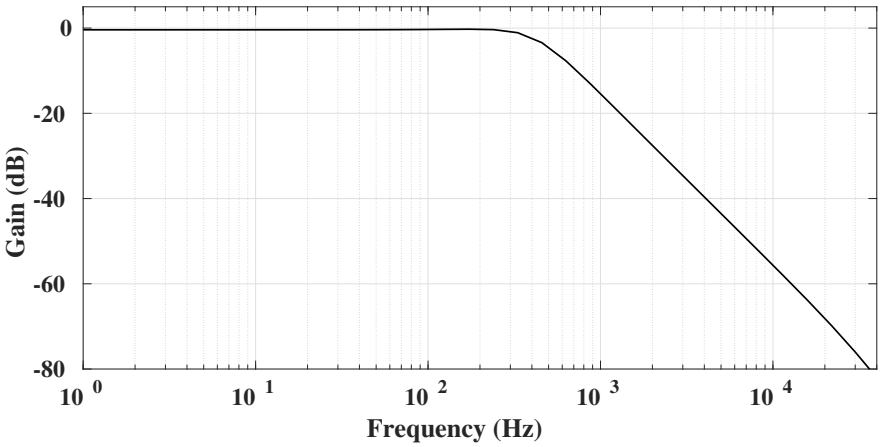


Figure 2.7: Frequency response of the filter.

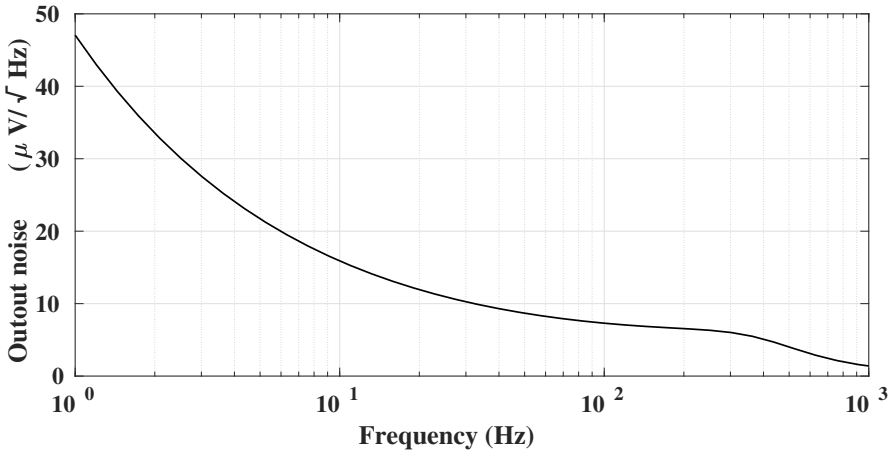


Figure 2.8: Output noise.

The cutoff frequency can be tuned from 74 Hz to 820 Hz by varying the current I_1 from 2 nA to 18 nA while keeping I_2 at 10 nA as shown in Figure 2.9. It can be tuned to the required value by controlling the currents I_1 and I_2 in the transconductor, so that it fits into the desired frequency range of different bio-potentials such as EMG, EEG, ECG etc. Table 2.3 lists the parameters of the filter.

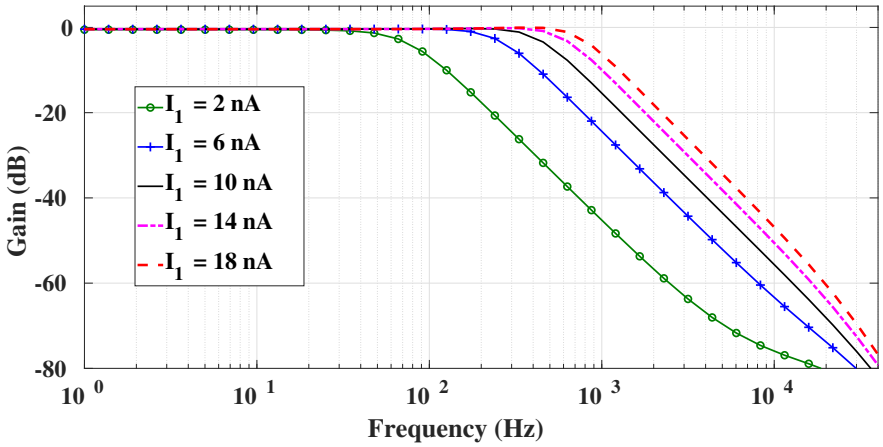


Figure 2.9: Cutoff frequency tuning with $I_2 = 10$ nA.

Table 2.3: Parameters of 2^{nd} order Butterwoth LPF for $I_1 = I_2 = 10$ nA.

Parameter	**Simulated values (Schematic)**
Cutoff frequency	456 Hz
Power	248 nW
V_{inpp} @ 100 Hz for 1% THD	180 mV
IRN (5 - 500 Hz)	160 μV RMS
DR	52 dB
Cutoff frequency tuning range	74 - 820† Hz

†For $I_2 = 10$ nA, $I_1 = 2$ - 18 nA.

A performance comparison of the designed filter with other similar works found in the literature is given in Table 2.4. Figure-of-Merit1 (FoM1) (refer A.8) is used as the performance measure. Lower value of FoM1 indicates better performance. The filter designed using the proposed transconductor achieves an FoM1 of 6.8×10^{-13} J, which

is better than the FoM1 values quoted in (Bruschi *et al.* 2007, Doménech-Asensi *et al.* 2014, Arya and Oliveira 2016, Alzaher and Algamdi 2014). In (Rodriguez-Villegas *et al.* 2004), floating-gate transistors are used to improve the DR and FoM1, but these transistors occupy more silicon area and need extra processing steps.

Table 2.4: Comparison of the designed filter (using Transconductor I) with other similar works

Parameters	Rodriguez-Villegas *et al.* 2004	Veeravalli *et al.* 2002	Bruschi *et al.* 2007	Alzaher and Algamdi 2014	Doménech-Asensi *et al.* 2014	Arya and Oliveira 2016	**This work**
Technology (μm)	0.8	1.2	0.35	0.18	0.35	0.13	**0.18**
V_{dd} (V)	1.25	$\pm$1.35	3.3	$\pm$0.9	3	0.9	**0.5**
Bandwidth (Hz)	0.1 - 2 k	0.3	1.5 - 15	1.5	1.95	25 - 225	**74 - 820**
Filter Order	2	2	2	2	2	2	**2**
V_{inpp} for 1% THD (mV)	1000	150	1000	300	762	7	**180**
IRN (μV RMS)	178	15.6	318	114	791	17	**160**
DR (dB)	78 - 62	-	60	60	50.65	43.8	**52**
Power (μW)	2.5	8.18	165	0.936	6.31	0.8	**0.248**
FoM1 (J) ($\times 10^{-13}$)	4.96	-	55 k	312 k	47 k	114.8	**6.8**

2.2.1.1 Performance over PVT variations

Simulations are carried out across process corners (tt, ff, ss, fnsp and snfp) and $\pm$10 % V_{dd} variations (450 mV & 550 mV) and the effect of them on cutoff frequency of the filter are analyzed. Worst case deviation in cutoff frequency is observed in fnsp corner with V_{dd}= 0.55 V and in ss corner with V_{dd}= 0.45 V and are plotted in Figure 2.10. The observed variation in cutoff frequency is as low as $\pm$2.4 %.

Figure 2.11 shows the normalized frequency response of the filter for a temperature variation in the range 0$-$70°C. It can be seen that the deviation in the cutoff frequency of the filter is $\pm$8 % up to 50°C.

It is observed that, when the temperature increases beyond 50°C, the variation in the cutoff frequency is more due to finite input impedance of the bulk-driven transcon-

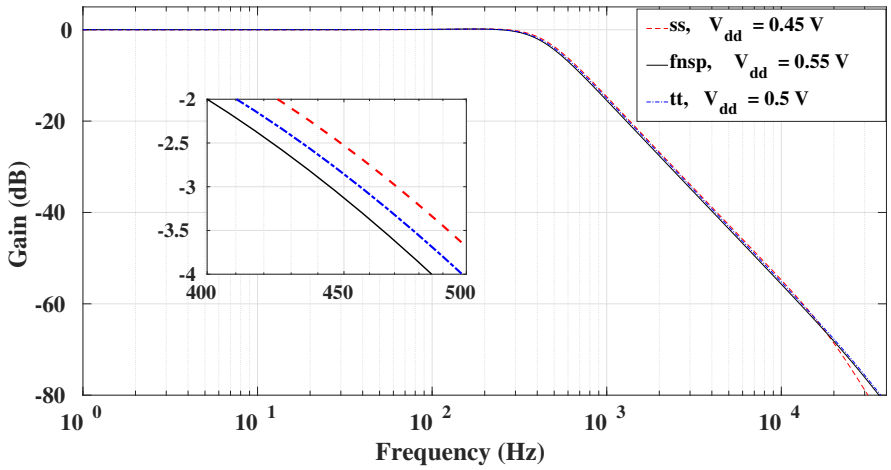


Figure 2.10: Cutoff frequency variation (worst case) for various corners and supply voltages

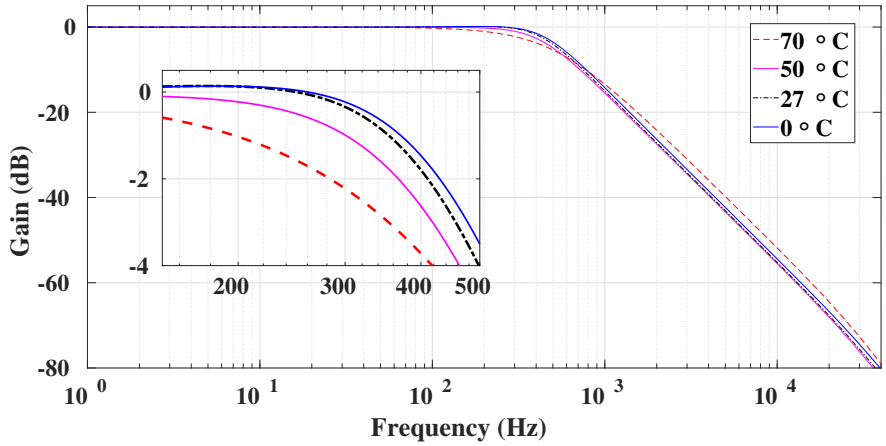


Figure 2.11: Cutoff frequency variation for various temperatures.

ductor. To strengthen this argument, the variation in the bulk-leakage current of the input bulk-driven transistor is plotted in Figure 2.12 with respect to temperature. W and V_{SB} of the input bulk-driven transistor in Transconductor I are 1 μm and 0.25 V respectively. The leakage current is insignificant till about 50°C. Beyond 50°C, it increases drastically. At 70°C, it is found to be 0.55 nA. Due to this leakage current, input impedance of the transconductor reduces and hence g_i increases. Till about 50°C, g_i is low. At 70°C, g_i is found to be 18.6 nS, which is comparable to G_m of 44.6 nS (Table 2.2). As G_m of the transconductor reduces with temperature (Table 2.2), cutoff frequency of the filter is expected to be reduced. But, it is observed that the

cutoff frequency increases by +17 % at 70°C. This can be justified by (2.16), which shows the effect of g_i on the cutoff frequency. At 70°C, DC gain and quality factor

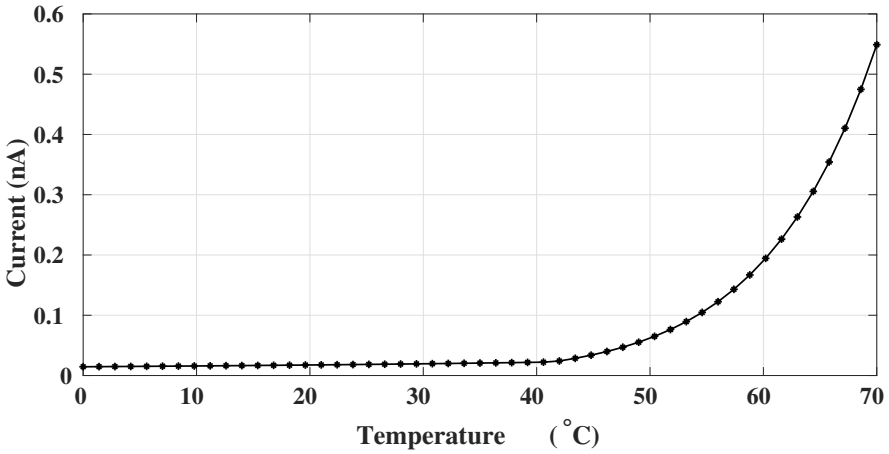


Figure 2.12: Bulk leakage current of input transistor.

are reduced to 0.5 (-6 dB) and 0.52 respectively. However, the frequency response at 70°C in Figure 2.11 is normalized to 0 dB for comparison purpose.

Hence, it can be inferred that at temperatures beyond 50°C, the deviation in the frequency response is more. This can be attributed to the increased bulk-leakage current of the input bulk-driven transistors, which results in decreased input resistance (increased g_i), there by affecting the cutoff frequency, quality factor and DC gain.

The bulk leakage current in UMC 180 nm is further investigated by plotting it for different W and V_{SB} values as shown in Figure 2.13. It is observed from Figures 2.13a and 2.13b that at higher temperatures the bulk leakage current increases with W and V_{SB}. The bulk leakage current can be reduced by reducing W or V_{SB} of the input transistor. It can also be reduced by using low leakage technology such as UMC 65 nm.

Figure 2.14 shows the variation of bulk leakage current of the transistors with varying W and V_{SB} in UMC 65 nm technology. It is observed that the leakage current is of the order of pAs and hence the input impedance will not get affected when the temperature increases as in the previous case. In view of this, Transconductor II is designed in UMC 65 nm LL technology and Transconductor III is designed in UMC 180 nm technology with $V_{SB} = 0.15$ V ($V_{dd} = 0.3$ V).

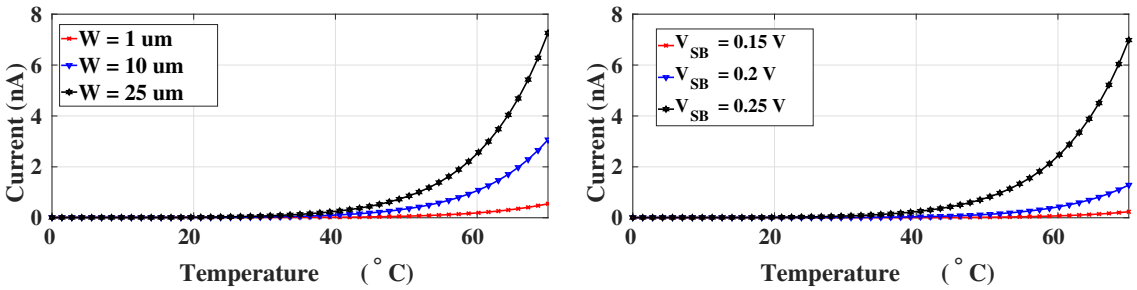


Figure 2.13: UMC 180 nm bulk leakage current (a) for $V_{SB} = 0.25$ V, (b) for W = 25 μm.

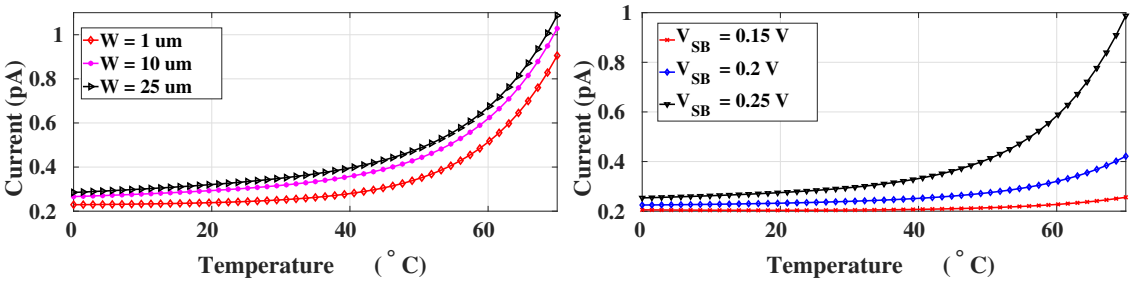


Figure 2.14: UMC 65 nm bulk leakage current (a) for $V_{SB} = 0.25$ V, (b) for W = 25 μm.

2.3 Transconductor II

Transconductor II is designed in UMC 65 nm LL technology with a supply voltage of 0.8 V.

In $G_m - C$ filter design, finite output resistance of the transconductor leads to reduction in the filter DC gain as well as deviation in the cutoff frequency and quality factor. This is justified by equations given in section 2.2. Hence, output resistance of the transconductor $(1/g_o)$ should be as high as possible ($g_o \ll G_m$). Cascode transistors can be used to achieve this. However, these cascode transistors reduce the signal swing. Composite transistor (Ferreira *et al.* 2008) shown in Figure 2.15 can be used to reduce g_o without reducing the signal swing. It can be treated as a single transistor (M_1) with transconductance, g_{m1} and increased output resistance given as in (2.18) (Ferreira *et al.* 2008). Hence, the composite transistors can be used in the

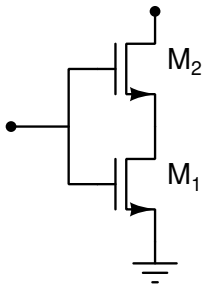


Figure 2.15: Composite transistor.

output stage of the transconductor block to reduce g_o without consuming extra power.

$$r_{comp} = g_{m2} r_{o2} r_{o1} \tag{2.18}$$

A fully differential configuration of the Transconductor II is shown in Figure 2.16a. The circuit is biased by a PTAT current source (explained in section 2.3.2) through transistor M_{13}. Here, gate terminals of input transistors, M_1 and M_3 are connected to their respective drain terminals (gate degeneration) (Sarpeshkar *et al.* 1997). Composite transistors ($M_5 - M_6$, $M_7 - M_8$, $M_9 - M_{10}$ and $M_{11} - M_{12}$) are used in the output stage to increase the output resistance of the transconductor.

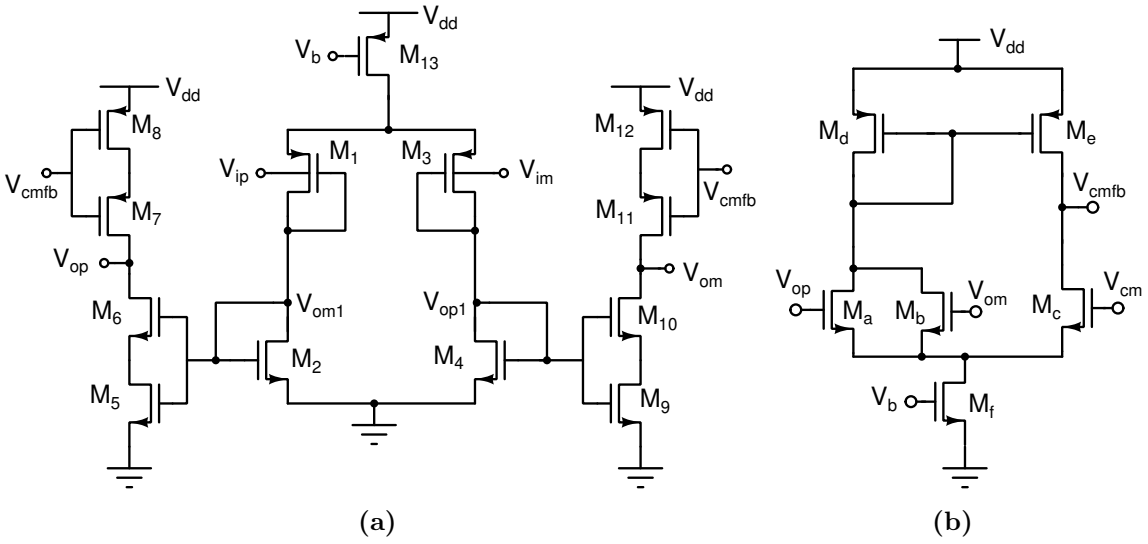


Figure 2.16: (a) Transconductor II, (b) CMFB circuit for Transconductor II

$V_{in,cm}$ is fixed at 0.4 V and $V_{o,cm}$ is set to 0.4 V by using CMFB circuit shown in Figure 2.16b. This CMFB circuit is based on the circuit given in (Rekha and Laxminidhi 2016), where PMOS input transistors are used. A PTAT current of 4.5

nA, generated from the proposed PTAT current reference circuit, is mirrored to the transistor, M_f. Difference of currents in the two legs of the CMFB circuit generates a voltage (V_{cmfb}) which in turn controls the currents in the transconductor thereby closing the negative feedback loop.

2.3.1 Small signal analysis

The small signal equivalent of left-half of the Transconductor II is shown in Figure 2.17, where r_x ($= g_{m6}r_{o6}r_{o5}$) and r_y ($= g_{m7}r_{o7}r_{o8}$) are output resistances of the composite transistors $M_5 - M_6$ and $M_7 - M_8$ respectively. The effective transconductance, G_m

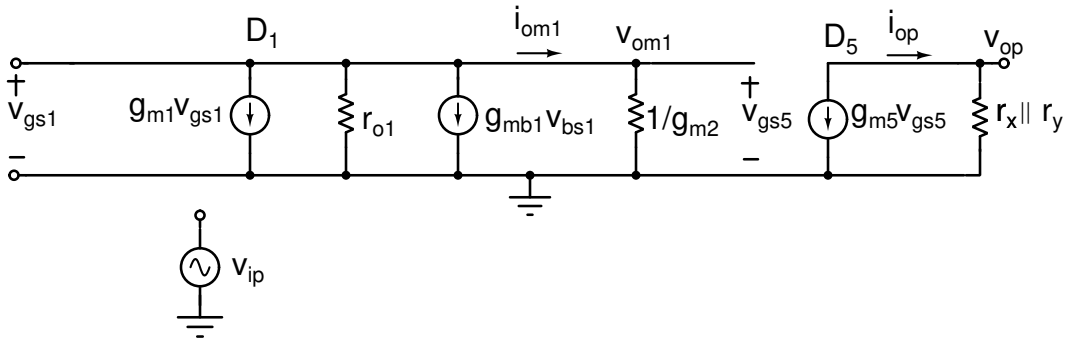


Figure 2.17: Small signal equivalent of the Transconductor II (left half).

can be derived as

$$G_m = \frac{i_{op}}{v_{ip}} = \frac{\frac{g_{m5}}{g_{m2}}g_{mb1}}{1 + \frac{1}{g_{m2}r_{o1}} + \frac{g_{m1}}{g_{m2}}} \tag{2.19}$$

As $g_{m2}r_{o1} \gg 1$, $g_{m1} = g_{m2}$ (by assuming both NMOS and PMOS have same η) and $g_{m2} = g_{m5}$, (2.19) is simplified to (2.20).

$$G_m \approx \frac{g_{mb1}}{2} \tag{2.20}$$

The expressions for the output resistance (r_{out}) and DC gain (A_V) of the transconductor are given by (2.21) and (2.22) respectively.

$$r_{out} = \frac{1}{g_o} = r_x \parallel r_y = (g_{m6}r_{o6}r_{o5}) \parallel (g_{m7}r_{o7}r_{o8}) \tag{2.21}$$

$$A_V = G_m r_{out} = \frac{g_{mb1}}{2}[(g_{m6}r_{o6}r_{o5}) \parallel (g_{m7}r_{o7}r_{o8})] \tag{2.22}$$

From (2.21) and (2.22), it can be seen that the output resistance and the DC gain

of the proposed transconductor have been increased by $g_m r_o$ times compared to a simple transconductor where single transistor is used in the output stage.

2.3.2 PTAT current reference circuit

Thermal voltage, V_T $(= \frac{kT}{q})$ is directly proportional to the temperature. For a constant drain current, g_{mb} is inversely proportional to the temperature as per (1.7). As the temperature increases, g_{mb} reduces and vice versa. This can be compensated by biasing the transconductor with a PTAT current source. With this, the current generated is directly proportional to the temperature and hence, makes G_m of the transconductor independent of temperature. This makes cutoff frequency of the filter independent of the temperature.

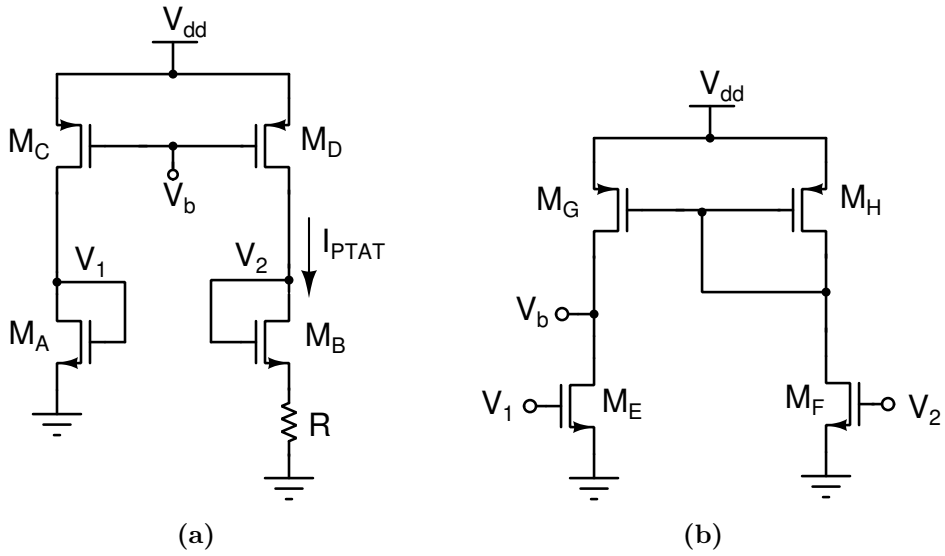


Figure 2.18: (a) PTAT current reference, (b) Error amplifier.

The PTAT current reference circuit shown Figure 2.18a is based on the beta-multiplier circuit (Razavi 2002, Baker and Boyce 2005). Gates of M_A and M_B are connected to their drains and given as inputs to the error amplifier shown in Figure 2.18b. The error amplifier output drives the gates of M_C and M_D. This makes the drain voltages of both M_A and M_B equal and hence currents through M_A and M_B are equal. This arrangement will also reduce the dependency of I_{PTAT} on V_{dd}. The expression for I_{PTAT} including the body effect of M_B is given by (2.23) (Razavi 2002,

Baker and Boyce 2005).

$$I_{PTAT} = \frac{V_T ln(p)}{R} \tag{2.23}$$

where $p = \frac{(W/L)_B}{(W/L)_A}$.

In this design, 'p' is chosen as 1.5. It can be seen from (2.23) that the current is directly proportional to temperature for a fixed resistor, R. This PTAT circuit can be used to compensate for the change in G_m across the temperature variations. Transistor sizes are adjusted to generate an I_{PTAT} of 4.5 nA and this current is mirrored as the bias current to the transconductor (Figure 2.16a) as well as to the CMFB circuit (Figure 2.16b) through transistors M_{13} and M_f respectively.

2.3.3 Post-layout Results

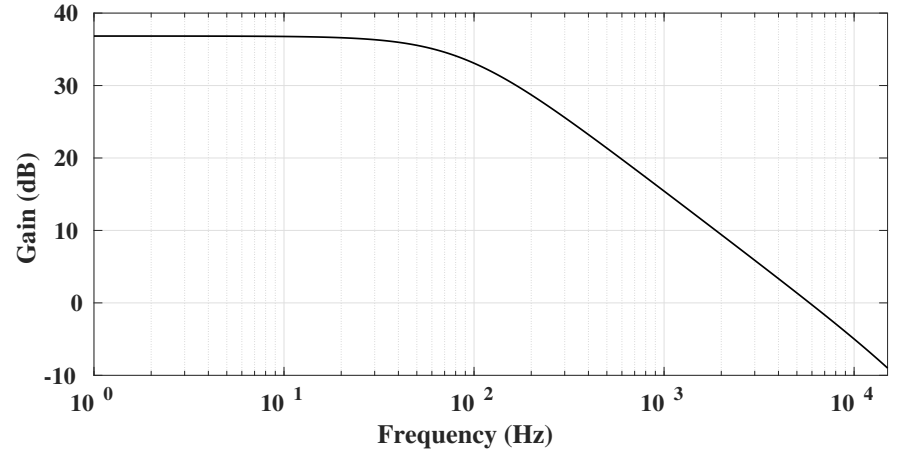
Fully differential Transconductor II is laid out along with CMFB circuit and PTAT current reference using Cadence Virtuoso. Figures 2.19a and 2.19b show the magnitude and phase responses of the transconductor respectively. Transconductor offers a DC gain of 36.8 dB and UGB of 5.8 kHz under no load condition. Observed phase margin is 72°. Table 2.5 presents various parameters of the proposed transconductor. It offers a G_m of 5.85 nS for an I_{PTAT} of 4.5 nA. The power consumption of the transconductor is as low as 7.2 nW.

Table 2.5: Parameters of Transconductor II.

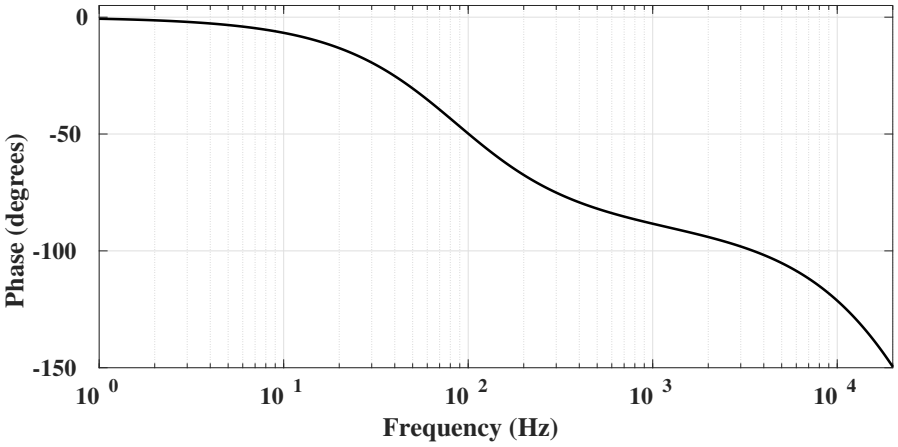
Parameters	**Simulated values**
Technology	UMC 65 nm
V_{dd}	0.8 V
DC gain	36.8 dB
UGB	5.8 kHz
Phase margin	72°
G_m	5.85 nS
Power Consumption	7.2 nW †

† Excluding CMFB and PTAT current reference.

Input/Output parasitic capacitances (C_i and C_o) and conductances (g_i and g_o) of the transconductor are given in Table 2.6. It can be seen that g_i and g_o values are negligible compared to G_m value. g_o is reduced to 50 pS (from 3.3 nS in the



(a)



(b)

Figure 2.19: (a) Magnitude, (b) Phase responses of the Transconductor II.

case of single transistor in the output stage of the transconductor) due to composite transistors in the output stage of the transconductor. Hence, these g_i and g_o values will not reduce the DC gain of the filter as explained in section 2.4.

Table 2.6: Input/output parasitics of Transconductor II.

g_i	g_o	C_i	C_o
0.01 nS	0.05 nS	0.04 pF	0.11 pF

The designed PTAT current reference circuit offers a current of 4.5 nA at room temperature (27°C) for an off chip resistor, R = 3 MΩ. In Figure 2.20a, I_{PTAT} is plotted against the temperature and it can be seen that the current varies linearly

with temperature in the range of -20°C to 70°C. Figure 2.20b shows the current variation with supply voltage. It can be seen that I_{PTAT} is constant in the supply voltage range of 0.4 - 1.2 V. The designed PTAT circuit can be operated down to a supply voltage of 0.4 V.

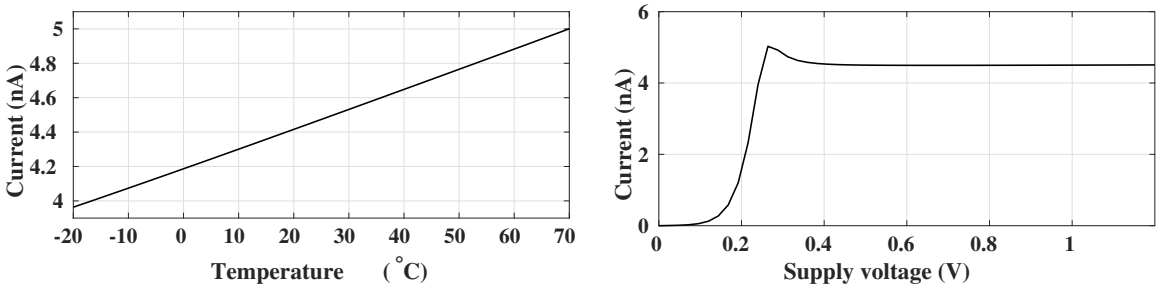


Figure 2.20: (a) I_{PTAT} versus temperature, (b) I_{PTAT} versus supply voltage.

Figure 2.21 shows the G_m variation with temperature when the transconductor is biased by constant current and designed PTAT current sources. With the constant current, G_m reduces almost linearly as the temperature increases. G_m is 6.4 nS and 5.5 nS at -20°C and 70°C respectively. This leads to a deviation of +9.4 % and -6 % at -20°C and 70°C respectively. With the PTAT current, G_m is almost independent of temperature up to about 50°C. The maximum deviation of +1.8 % occurs at 70°C. This deviation is due to the deviation of I_{PTAT} current from its PTAT characteristics. The total power consumption of the PTAT current reference circuit is 11.4 nW at room temperature.

2.4 LPF Realization Using Transconductor II

A 2^{nd} order Butterworth LPF of cutoff frequency of 100 Hz is implemented using the proposed transconductor. Filter architecture shown in Figure 2.6 has been used here.

As g_i and g_o values (Table 2.6) are very small compared to G_m (5.85 nS), they can be neglected in (2.15), (2.16) and (2.17). C_i and C_o can be accommodated along with C_1 and C_2. The expressions for DC gain, cutoff frequency and quality factor of the LPF, if all the transconductors have equal G_m values, are given by (2.24), (2.25) and (2.26) respectively.

$$A_o = 1 \tag{2.24}$$

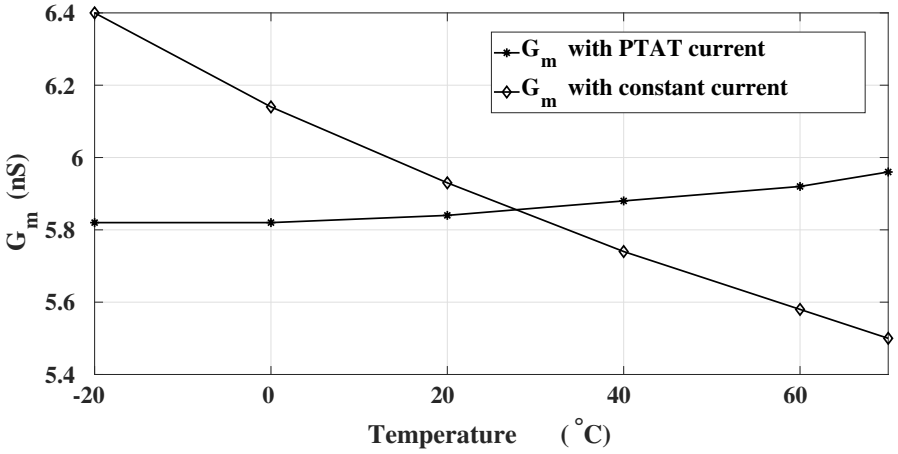


Figure 2.21: G_m variation with constant and PTAT currents.

$$f_o = \frac{G_m}{2\pi\sqrt{C_1' C_2'}} \tag{2.25}$$

$$Q = \sqrt{\frac{C_1'}{C_2'}} \tag{2.26}$$

C_1 and C_2 are taken as 6 pF and 12.6 pF to get a Butterworth response ($Q_o = 1/\sqrt{2}$). Two CMFB circuits, one for G_{m1}, G_{m2} and G_{m4} blocks and second one for G_{m3} block are used in the filter circuit to set output common mode levels.

2.4.1 Post-layout Simulation Results & Discussion

The layout of the filter is shown in Figure 2.22 employing MIM capacitors. It takes an area of 0.065 mm^2 (278 μm $\times$ 235 μm). The magnitude response of the filter for an I_{PTAT} of 4.5 nA is shown in Figure 2.23. DC gain and cutoff frequency are -0.14 dB and 100 Hz respectively. The roll-off rate of the filter is -40 dB/decade as expected.

As shown in Figure 2.24, cutoff frequency can be linearly tuned from 10 Hz to 1 kHz by varying I_{PTAT} from 0.45 nA to 45 nA. Hence, it can be fit into the required bandwidth of different biological signals. I_{PTAT} can be varied by using the off chip resistor, R.

A sinusoidal signal of frequency 25 Hz is fed into the filter to test its linearity. Figure 2.25a shows the harmonics in the output of the filter. THD is found to be 1 % (-40 dB) for an input voltage of 580 mVpp. Third order harmonic distortion (HD_3) of -42 dB is observed for the same input voltage. Two input signals with

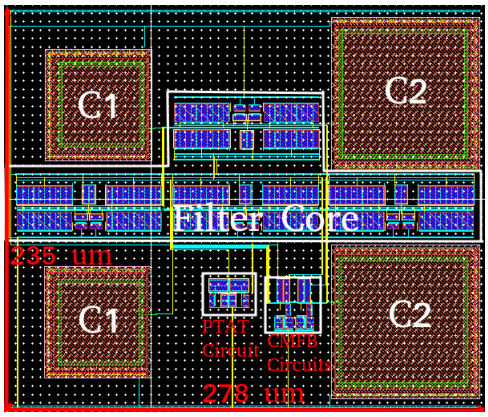


Figure 2.22: Layout of the filter with CMFB and PTAT circuits.

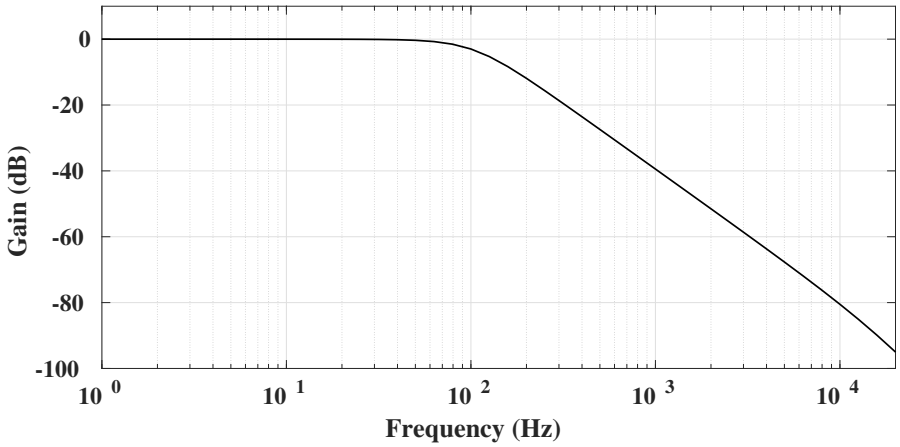


Figure 2.23: Magnitude response of the filter.

same amplitude and different frequencies, 20 Hz and 30 Hz are applied to the filter to check its intermodulation behavior. For an input voltage of 280 mVpp, third order intermodulation distortion (IMD_3) of -40 dBc is observed as shown in Figure 2.25b. Noise plot is shown in Figure 2.25c. IRN integrated over the frequency range 1-100 Hz is found to be 360 μVrms. The DR and FoM1 of the filter are calculated as 55.1 dB and 4.12×10^{-13} J respectively.

The comparison of the proposed filter with other similar designs is given in Table 2.7. It can be seen that FoM1 of the proposed filter is better than the FoM1 of the $G_m - C$ filters in (Lee and Cheng 2009, Liu *et al.* 2012, Mahmoud *et al.* 2013, Arya and Oliveira 2016, Rao and Rekha 2018, Sun and Lee 2018). Filters in (Sawigun and Thanapitak 2018, Thanapitak and Sawigun 2018, Sawigun and Thanapitak 2019) are

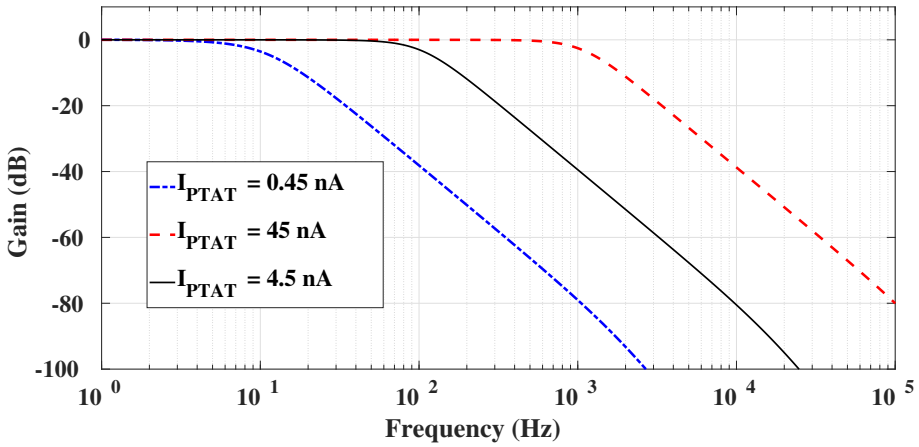


Figure 2.24: Cutoff frequency tuning of the filter.

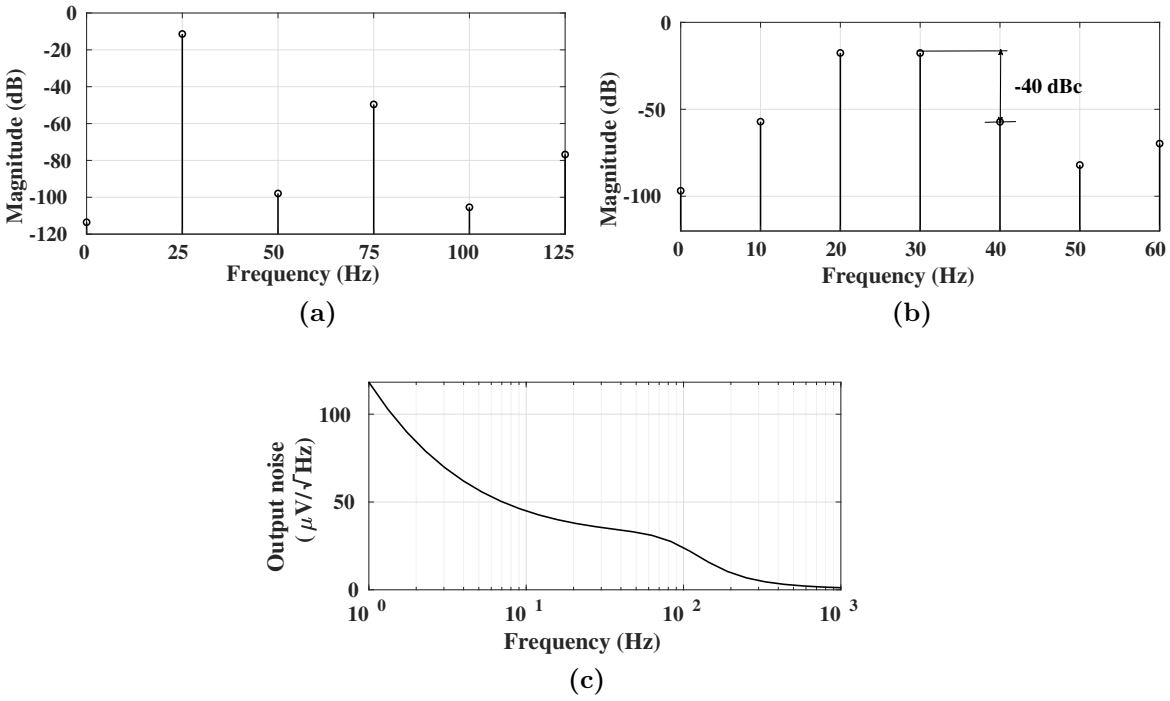


Figure 2.25: (a) Harmonics, (b) Intermodulation distortion, (c) Output noise of the filter.

based on SF or VF. They generally consume very low power compared to $G_m - C$ filters. However, the input signal swing of the filters in (Sawigun and Thanapitak 2018, Thanapitak and Sawigun 2018, Sawigun and Thanapitak 2019) is less than that of the proposed filter. Even with the supply voltage of 0.8 V, the proposed filter is

better in terms of input signal swing compared to all, except (Liu *et al.* 2012) ((Liu *et al.* 2012) uses a supply voltage of 3 V). The DR of the filter is better compared to all, except (Mahmoud *et al.* 2013, Sawigun and Thanapitak 2019). However, the design in (Mahmoud *et al.* 2013) consumes more power. The DC gain of the proposed filter is almost 0 dB, thanks to the composite transistors. The DC gain of the filters in (Lee and Cheng 2009, Liu *et al.* 2012, Mahmoud *et al.* 2013, Sun and Lee 2018) is less than 0 dB due to finite output resistance of the transconductors used in these designs.

IRN of the proposed filter is more compared to filters listed in Table 2.7. However, it is within the limit as explained below in connection with ECG signal processing. The limit on IRN is calculated by using (2.27) (Lee and Cheng 2009).

$$IRN_{max} = \frac{V_{in,rms}}{10^{SNR(dB)/20}} \tag{2.27}$$

The maximum and minimum signal levels of ECG are 4 mV and 100 μV (Webster 2009) respectively. For ECG signal, the SNR must be more than 38 dB (Lee and Cheng 2009). For the proposed design, $V_{in,rms}$ is 205 mVrms ($580/2\sqrt{2}$). By using (2.27), IRN_{max} allowed for the filter is calculated as 2580 μVrms. But IRN of the proposed filter is only 360 μVrms which is very much less than IRN_{max} (2580 μVrms). Hence this filter can be satisfactorily used for front-end processing of ECG signals.

2.4.1.1 Effect of PVT variations on cutoff frequency

The frequency response of the filter across process corners is shown in Figure 2.26. Gain is normalized to 0 dB to compare the results. Cutoff frequency is 96 Hz and 105 Hz in 'ss' and 'ff' corners respectively. Worst case deviation occurs in 'ss' and 'ff' corners. Hence, the deviation in cutoff frequency is < 5 %. For a ± 10 % variations in V_{dd}, cutoff frequency variation is only ± 1 % as shown in Figure 2.27. The frequency response of the filter for different temperatures is shown in Figure 2.28. Cutoff frequency is 99.8 Hz and 102 Hz at -20°C and 70°C respectively. The deviation of 2 Hz at 70°C is due to the deviation of PTAT current from its actual value. These results show the robustness of the design across PVT variations.

To check the deviation in filter parameters (cutoff frequency and DC gain) across transistor process and mismatch variations, Monte Carlo simulations are performed for 100 runs. As shown in Figure 2.29a, the mean and standard deviation of cutoff

Table 2.7: Comparison of the proposed work with other designs from the literature.

Parameters	Tech. (nm)	V_{dd} (V)	Filter Order	DC Gain (dB)	Cutoff frequency (Hz)	Power (nW)	V_{inpp} for 1% THD (mV)	IRN (μV_{rms})	DR (dB)	Active area (mm^2)	FoM1 (J) ($\times 10^{-13}$)
Lee and Cheng 2009*	180	1	5	-10.5	250	453	100	≈300**	50	0.13	11.5
Liu *et al.* 2012†	350	3	4	≈-7	40	750	735	500	54	–	93.5
Mahmoud *et al.* 2013†	250	± 0.8	5	≈-4	243	3×10^4	100	36	65	0.09	138
Arya and Oliveira 2016‡	130	0.9	2	5.99	48	800	7	17.38**	43.8	–	538
Rao and Rekha 2018‡	180	0.5	2	≈0	456	248	180	160**	52	–	6.83
Sun and Lee 2018*	180	1	5	-8	50	350	86	97	49.9	0.12	44.8
Sawigun and Thanapitak 2018*	350	0.6	4	-2.77	101	0.9	130	46.27††	47	0.168	0.1
Thanapitak and Sawigun 2018*	350	0.9	4	-0.05	100	4.26	70	80.5††	48.2	0.11	0.4
Sawigun and Thanapitak 2019*	350	1.5	4	-0.09	100	5.25	110	39.38††	56.9	0.1	0.19
This work†	65	0.8	2	-0.14	100	47	580	360**	55.1	0.065	4.12

*measured, †post-layout simulation, ‡schematic simulation. **integrated over 1 - f_o, ††integrated over 1 - $2f_o$.

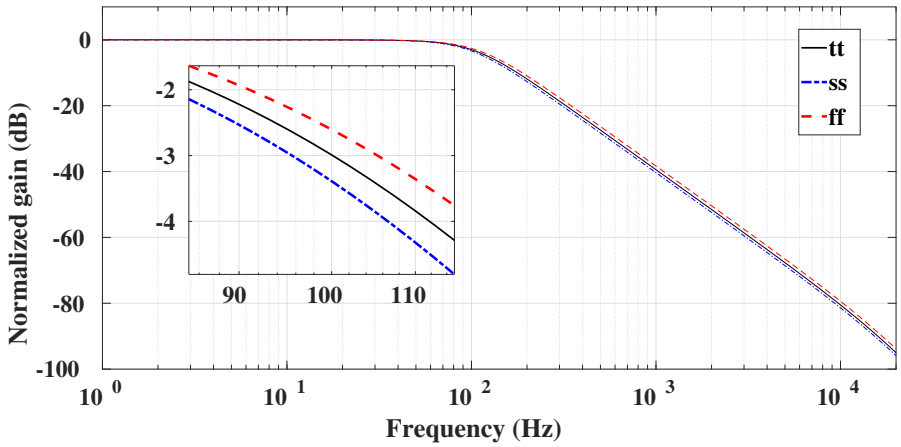


Figure 2.26: Frequency response for different process corners showing worst case deviation.

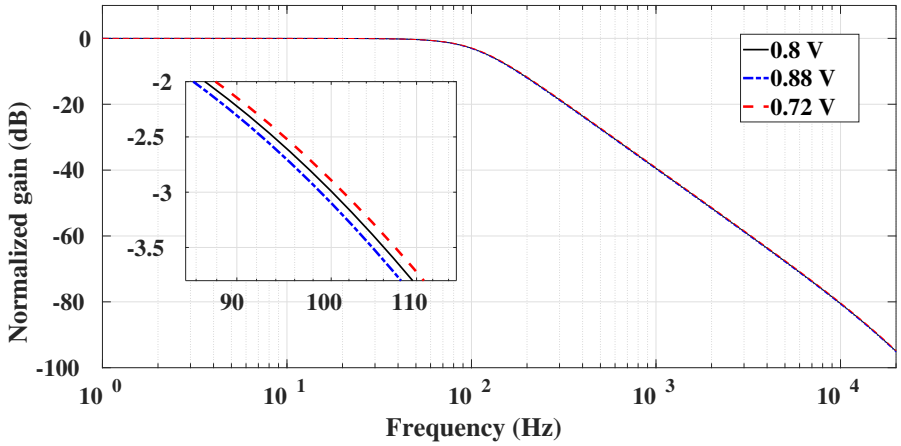


Figure 2.27: Frequency response for ± 10 % variations in V_{dd}.

frequency are 100.5 Hz and 5.4 Hz respectively. The mean value of DC gain is -0.16 dB with 0.26 dB standard deviation as shown in Figure 2.29b. These results show that the design is robust.

2.5 Transconductor III

In order to avoid the bulk leakage current, Transconductor III is designed in UMC 180 nm technology with $V_{SB} = 0.15$ V ($V_{dd} = 0.3$ V) for input bulk-driven transistors.

The proposed transconductor is shown in Figure 2.30. It is biased by a DC current,

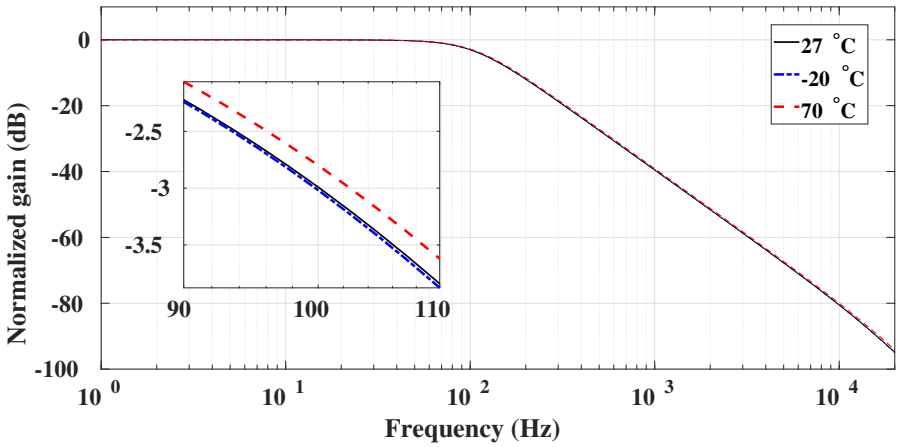


Figure 2.28: Frequency response for different temperatures.

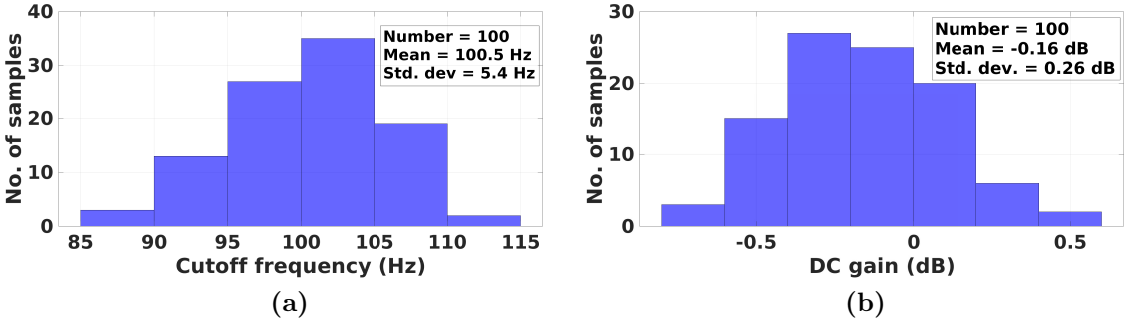


Figure 2.29: Monte Carlo simulations of (a) cutoff frequency, (b) DC gain.

I_o which is mirrored from M_5 to M_3 and M_4. Inputs (V_{ip} and V_{im}) are applied to the bulk-terminals of the transistors M_1 and M_2 respectively. Small signal current in M_1 is mirrored to M_2 through their gate terminals and the single ended positive output is obtained at V_o. The dimensions of all the transistors are given in Table 2.8.

Table 2.8: Dimensions of transistors

Transistors	M_1 & M_2	M_3, M_4 & M_5
$\frac{W}{L}$ $(\frac{\mu m}{\mu m})$	$\frac{10}{1}$	$\frac{5}{10}$

The transconductor operates from 0.3 V supply and $V_{in,cm}$ is fixed at 0.15 V. The effective transconductance (G_m) of the transconductor is equal to input transistor's bulk-transconductance (g_{mb1} or g_{mb2}). For $I_o = 1$ nA, the transconductor offers a G_m

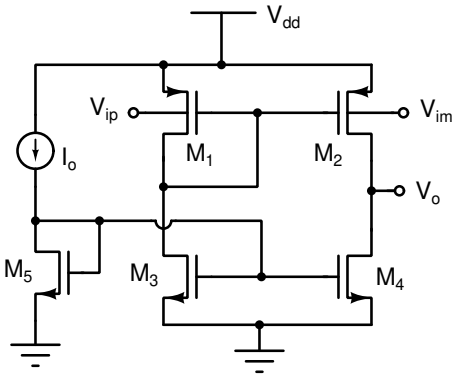


Figure 2.30: Transconductor III.

of 7.8 nS.

The expression for input referred voltage noise is obtained by adding all current noise components at the output and divide it by the transconductance. By doing that, the power spectral density (PSD) of input referred thermal noise voltage can be derived as

$$\overline{v_{in,th}^2} = \frac{16kT}{3(\eta-1)^2 g_{m1}}\left[1+\frac{g_{m3}}{g_{m1}}\right] \tag{2.28}$$

Similarly, PSD of input referred flicker noise voltage can be derived as

$$\overline{v_{on,1/f}^2} = \frac{2}{C_{ox}(\eta-1)^2 f}.\left[\frac{K_{fp}}{(WL)_1}+\frac{K_{fn}}{(WL)_3}\frac{g_{m3}^2}{g_{m1}^2}\right] \tag{2.29}$$

where K_{fn} and K_{fp} are flicker noise parameters for NMOS and PMOS transistors respectively. The dimensions of all the transistors are chosen to reduce flicker noise and to ensure sub-threshold saturation region of operation.

2.6 Fourth Order LPF Using Transconductor III

A simple $G_m - C$ low-pass biquad (Geiger and Sanchez-Sinencio 1985) is shown in Figure 2.31. Its transfer function can be written as in (2.30). From (2.30), cutoff frequency (f_o) and quality factor (Q) can be written as in (2.31) and (2.32) respectively.

$$H(s) = \frac{1}{(s^2 C_1 C_2/G_{m1}G_{m2}) + (sC_1/G_{m1}) + 1} \tag{2.30}$$

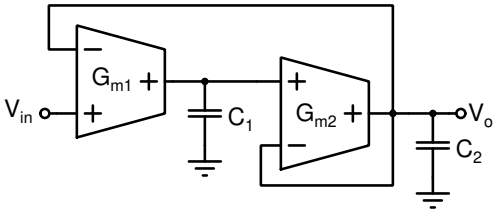


Figure 2.31: $G_m - C$ biquad.

$$f_o = \frac{1}{2\pi}\sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} \tag{2.31}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{2.32}$$

A fourth order Butterwoth LPF is designed by cascading two biquads (Figure 2.31) as shown in Figure 2.32. The Q values are taken as 0.54 and 1.3 for the first and second biquads respectively for a Butterworth response. All the four transconductors have the same G_m of 7.8 nS. Capacitor values are chosen to get required Q and f_o values by taking parasitic capacitances into account.

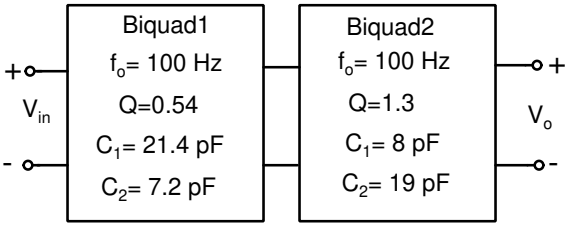


Figure 2.32: Fourth order LPF.

2.6.1 Post-layout Simulation Results

The layout of fourth order LPF is shown in Figure 2.33. It occupies an area of 0.07 mm^2 . Figure 2.34 shows the magnitude response of the filter for I_o =1 nA. DC gain is -1.3 dB and cutoff frequency is 100 Hz.

Linearity of the filter is tested by applying an input sinusoidal signal of 20 Hz frequency. For 50 mVpp input, the obtained THD in the output is 1 %. Further, output voltage spectrum for the same input is plotted in Fig. 2.35. The second order harmonic distortion (HD_2) is found to be -40 dB.

The output voltage noise spectral density is shown in Figure 2.36. Integrated IRN

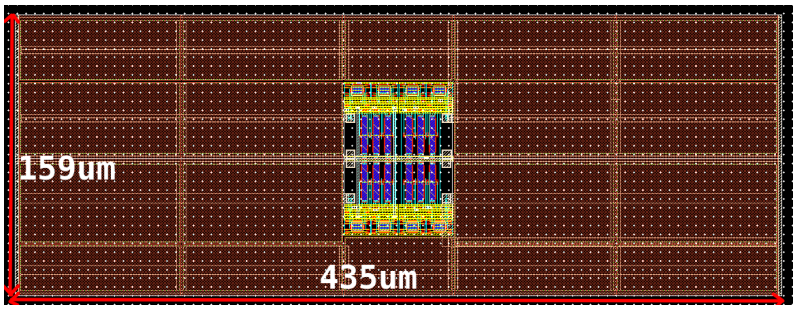


Figure 2.33: Layout of the filter.

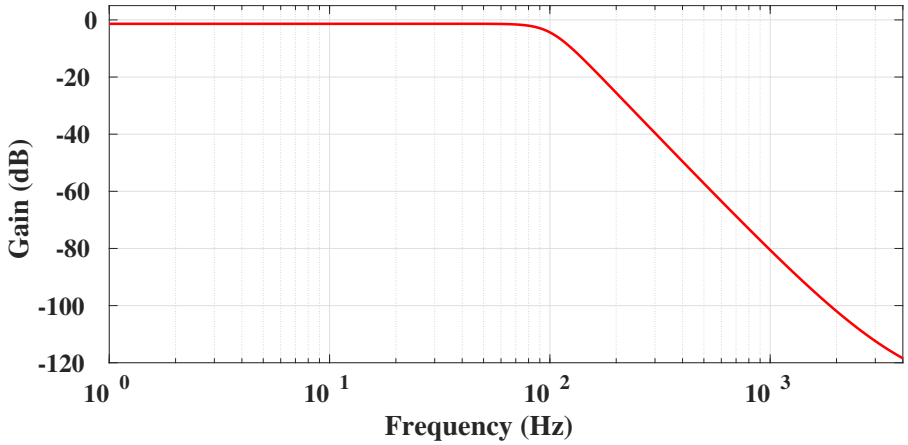


Figure 2.34: Magnitude response of the filter.

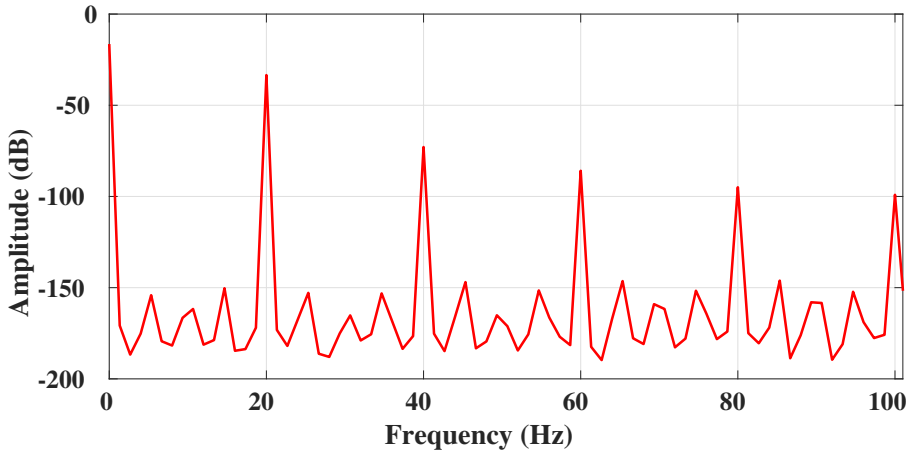


Figure 2.35: Harmonic components.

over the frequency range, 1 - 100 Hz is found to be 60.56 μVrms. From the values of input voltage for 1 % THD and IRN, the DR of the filter is calculated as 49.3 dB.

FoM2 for the proposed filter is found to be 6.2×10^{-15}.

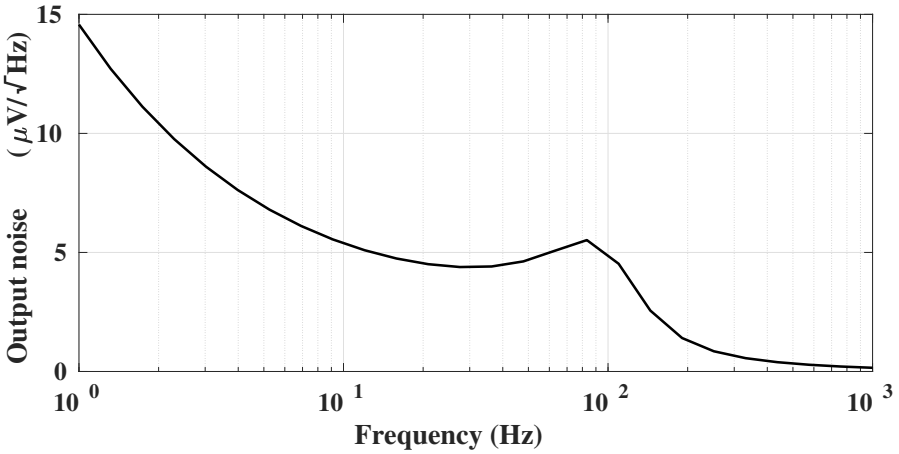


Figure 2.36: Output voltage noise spectral density.

As shown in Figure 2.37, the cutoff frequency of the filter can be tuned from 50 Hz to 250 Hz by changing I_o from 0.5 nA to 2.6 nA.

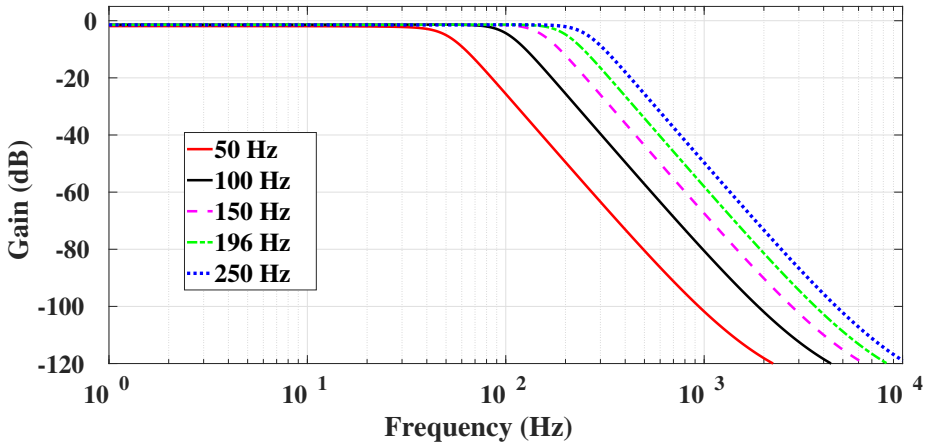


Figure 2.37: Cutoff frequency tuning. [I_o (nA), f_o (Hz)]: [0.5, 50], [1, 100], [1.5, 150], [2, 196] and [2.6, 250].

Table 2.9 shows the performance summary and comparison of the results with other LPF designs of the same cutoff frequency range. The proposed filter operates from 0.3 V supply, which is extremely low. It shows superior performance as far as FoM2 and power consumption are considered. The DR of the proposed filter (49.3 dB) is less compared to the DR of the designs in (Zhang *et al.* 2013, Rao and Rekha

2019, Hanumantha Rao and Rekha 2019, Krishna and Laxminidhi 2018, Sawigun and Thanapitak 2019). However, it is sufficient to process ECG signal as discussed in section 2.4.1.

Table 2.9: Results summary and Performance comparison.

Parameter	Zhang *et al.* 2013†	Arya and Oliveira 2016⋆	Thanapitak and Sawigun 2018†	Krishna and Laxminidhi 2018⋆⋆	Hanumantha Rao and Rekha 2019⋆⋆	Rao and Rekha 2019⋆⋆	Sawigun and Thanapitak 2019†	**This Work⋆⋆**
V_{dd} (V)	3	0.9	0.9	1.8	0.8	0.8	1.5	**0.3**
Technology (nm)	350	130	350	180	65	65	350	**180**
Filter order	4	2	4	4	2	2	4	**4**
Cutoff frequency (Hz)	100	48	100	50	100	100	100	**100**
DC gain (dB)	-3.7	5.99	-0.05	0	-0.14	-2.47	-0.09	**-1.3**
Power (nW)	15	800	4.26	570	47	8	5.25	**2.4**
V_{inpp} @ 1 % THD (mV)	50	7	70	196	580	140	110	**50**
IRN_{rms} (μV)	36	17.38	80.5	109	360	40	39.38	**60.56**
DR (dB)	66.7	43.8	48.2	56.1	55.1	61.85	56.9	**49.3**
Active area (mm^2)	0.11	–	0.11	0.74	0.065	0.008	0.1	**0.07**
FoM ($\times 10^{-15}$)	51.9	48.4 k	37.3	7.9k	329	25.8	28	**6.2**

⋆⋆post-layout simulations; ⋆schematic simulations; †measured;.

2.6.1.1 PVT and Monte Carlo simulations

The deviation in the cutoff frequency of the filter is less than 1 % across all process corners (tt, ss, ff, snfp and fnsp) and ±10 % V_{dd} variations. For 0 -70°C temperature range, the cutoff frequency deviation is about 6 %, which can be reduced by using PTAT current. Figure 2.38 shows the histogram of cutoff frequency for 200 runs. Its mean and standard deviation are 98.8 Hz and 3.5 Hz respectively. Hence, the design is found to be robust across PVT variations and suitable for ECG signal processing.

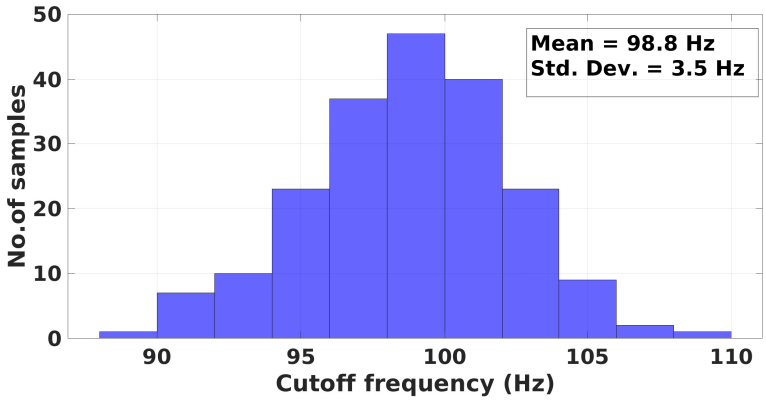


Figure 2.38: Histogram of the cutoff frequency for 200 runs.

Chapter 3

DESIGN OF SOURCE FOLLOWER AND VOLTAGE FOLLOWER BASED FILTERS

In recent years, SF and VF filters have become popular for low power and low frequency applications. These filters are more linear and power efficient when compared to regular $G_m - C$ filters. They offer more DR even under low supply conditions. In (Sawigun and Serdijn 2016), an LPF is implemented by cascading simple VFs.

This chapter discusses an area efficient time constant enhancement technique for a SF LPF. As an application of the proposed technique, a 2^{nd} order SF LPF is realized in UMC 65 nm technology with a 0.8 V supply voltage. A 5 nA constant current reference circuit is also designed to bias the SF LPF. Further, a bulk-driven VF operating with an ultra low supply voltage of 0.3 V is proposed. A 4^{th} order LPF is realized in UMC 180 nm technology by cascading the proposed bulk-driven VFs.

3.1 Basic SF LPF

A simple SF circuit (Razavi 2002) with load capacitor, C is shown in Figure 3.1. Its transfer function including the body effect can be derived as in (3.1). Output resistance of current source (I_o) is assumed to be very high compared to small signal resistance of M_1.

$$H(s) = \frac{\frac{g_{m1}r_{o1}}{1+(g_{m1}+g_{mb1})r_{o1}}}{1+\frac{sCr_{o1}}{1+(g_{m1}+g_{mb1})r_{o1}}} \tag{3.1}$$

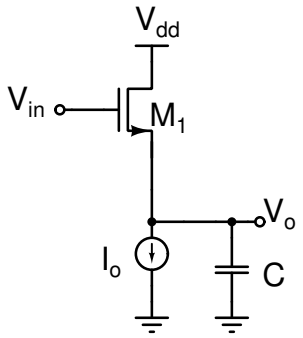


Figure 3.1: Basic SF LPF.

where, g_{m1} is the gate transconductance, g_{mb1} is the bulk transconductance and r_{o1} is the small signal resistance of M_1. From (3.1), it can be seen that the SF circuit shown in Figure 3.1 resembles a first order LPF characteristics. By comparing (3.1) with the transfer function of ideal first order LPF, $\frac{A_o}{1+s\tau}$, the DC gain (A_o) and time constant (τ) can be written as in (3.2) and (3.3) respectively.

$$A_o = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1}} \tag{3.2}$$

$$\tau = \frac{r_{o1}C}{1 + (g_{m1} + g_{mb1})r_{o1}} \tag{3.3}$$

As $(g_{m1} + g_{mb1})r_{o1} \gg 1$, $A_o \approx 1$ and (3.3) is simplified to (3.4).

$$\tau = C/(g_{m1} + g_{mb1}) \tag{3.4}$$

Hence, cutoff frequency can be written as in (3.5).

$$f_c = \frac{1}{2\pi\tau} = \frac{(g_{m1} + g_{mb1})}{2\pi C} \tag{3.5}$$

From (3.4), it can be seen that the time constant depends on the capacitor charging path. In basic SF LPF (Figure 3.1), the capacitor (C) charges through M_1. Its time constant is the product of resistance offered by M_1 (looking into the source) and C. For example, to design a basic SF LPF with $f_c = 100$ Hz and $I_o = 5$ nA, the required capacitance (C) can be calculated from (3.5). Through simulations, it is verified that in UMC 65 nm technology, with $I_o = 5$ nA, $g_{m1}(= \frac{I_o}{\eta V_T})$ is 157 nS. Required capacitance (C) is 250 pF which takes an area of approximately 0.125 mm^2.

Instead of using large capacitors, the time constant can be increased by adding a large resistor (of the order of 100s of MΩ to GΩ to get a cutoff frequency of the order of 100 Hz) in the capacitor charging path. However, implementing large passive resistors occupies large area on the chip.

3.2 Area efficient SF LPF

In this work, an active resistor of high resistance value, implemented by a transistor operating in sub-threshold linear region ($V_{GS} < V_{th}$ and $V_{DS} < 3V_T$), is added in the capacitor charging path to increase the time constant. The proposed SF LPF is shown in Figure 3.2a. An extra transistor, M_2 operating in sub-threshold linear region is connected in between source of M_1 and the capacitor. M_1 is operating in sub-threshold saturation region ($V_{GS} < V_{th}$ and $V_{DS} \geq 3V_T$). The small signal equivalent circuit of the proposed SF LPF is shown in Figure 3.2b. As M_2 is operating in sub-threshold linear region, it is represented by a resistor, R_{o2} and its transconductance can be neglected. In Figure 3.2b, g_{m1} is the transconductance and r_{o1} is the small signal output resistance of M_1. Output resistance of the current source (I_o) is assumed to be very high compared to r_{o1}.

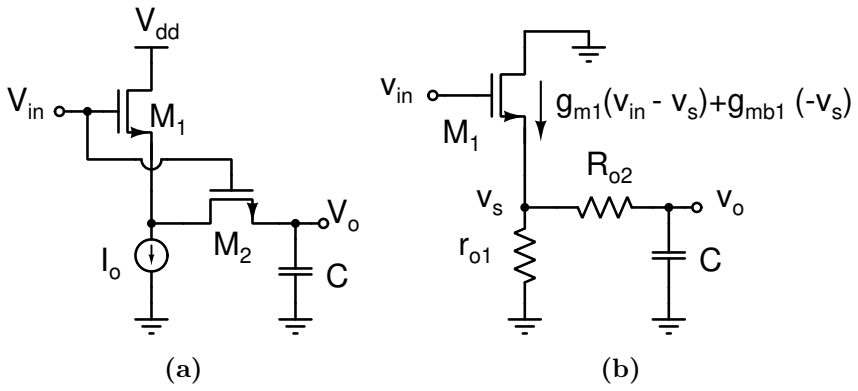


Figure 3.2: (a) Proposed SF LPF, (b) Small signal equivalent circuit.

Now, the transfer function for the proposed SF LPF can be derived from its small signal equivalent (Figure 3.2b) as follows. By applying KCL at node v_s,

$$v_s\left(\frac{1}{r_{o1}} + \frac{1}{R_{o2}} + g_{m1} + g_{mb1}\right) - v_{in}g_{m1} - \frac{v_o}{R_{o2}} = 0 \tag{3.6}$$

By applying KCL at node v_o,

$$v_o(sC) + \frac{v_o - v_s}{R_{o2}} = 0 \tag{3.7}$$

$$\Rightarrow v_s = v_o R_{o2}(sC + \frac{1}{R_{o2}}) \tag{3.8}$$

By substituting (3.8) in (3.6), we obtain the transfer function,

$$H_1(s) = \frac{v_o}{v_{in}} = \frac{\frac{g_{m1}r_{o1}}{1+(g_{m1}+g_{mb1})r_{o1}}}{1 + \frac{sC[r_{o1}+R_{o2}+(g_{m1}+g_{mb1})r_{o1}R_{o2}]}{1+(g_{m1}+g_{mb1})r_{o1}}} \tag{3.9}$$

As $(g_{m1} + g_{mb1})r_{o1} \gg 1$, (3.9) can be simplified to (3.10).

$$H_1(s) \approx \frac{1}{1 + sC[R_{o2} + 1/(g_{m1} + g_{mb1})]} \tag{3.10}$$

From (3.10), the time constant of the proposed SF LPF can be expressed as in (3.11).

$$\tau_1 = [R_{o2} + 1/(g_{m1} + g_{mb1})]C \tag{3.11}$$

Hence, cutoff frequency for the proposed SF LPF can be written as in (3.12).

$$f_{c1} = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi[R_{o2} + 1/(g_{m1} + g_{mb1})]C} \tag{3.12}$$

As M_2 is operating in sub-threshold linear region, its resistance R_{o2} is $\gg 1/(g_{m1}+g_{mb1})$. This is confirmed by simulation results given in section 3.2.4. For a fixed capacitor value, f_{c1} depends mainly on R_{o2}.

3.2.1 Derivation for R_{o2}

The drain current equation of M_2 is given by (3.13) (refer A.1).

$$I_{D2} = I_{D0}(\frac{W}{L})_2 \, e^{\frac{V_{GS2}-V_{th2}}{\eta V_T}}(1 - e^{\frac{-V_{DS2}}{V_T}}) \tag{3.13}$$

Differentiating I_{D2} with respect to V_{DS2},

$$\frac{dI_{D2}}{dV_{DS2}} = \frac{I_{D0}}{V_T}(\frac{W}{L})_2 \, e^{\frac{V_{GS2}-V_{th2}}{\eta V_T}} e^{\frac{-V_{DS2}}{V_T}} \tag{3.14}$$

$$\Rightarrow R_{o2} = \frac{1}{\frac{dI_{D2}}{dV_{DS2}}} = \frac{V_T.e^{\frac{V_{DS2}}{V_T}}}{I_{D0}(\frac{W}{L})_2\ e^{\frac{V_{GS2}-V_{th2}}{\eta V_T}}} \tag{3.15}$$

From (3.15), it is evident that R_{o2} depends on V_{GS2}, which in turn depends on I_o chosen. As $V_{DS2} \ll V_T$, $e^{\frac{-V_{DS5}}{V_T}} \approx 1$. As $V_{GS2} \approx V_{GS1}$, (3.15) can be further simplified to (3.16) by substituting V_{GS1} (from A.2) in place of V_{GS2} and expressing in terms of I_o.

$$R_{o2} = \frac{aV_T(W/L)_1}{I_o(W/L)_2} \tag{3.16}$$

where $a = e^{\frac{V_{th2}-V_{th1}}{\eta V_T}}$. Hence, linear tuning of R_{o2} is possible by varying I_o.

3.2.2 Second order SF LPF

A 2^{nd} order LPF as shown in Figure 3.3a is designed by cascading two complementary circuits of proposed SF LPF (NMOS and PMOS SF LPFs). Hence, roll off rate can be increased to -40 dB/decade. A bias current of 5 nA is mirrored to both NMOS and PMOS SF LPFs. As the bias current is in the range of nA, self-cascode or composite transistors (Ferreira *et al.* 2008) are used to mirror bias currents. These composite transistors offer higher output impedance (compared to single transistors) which improves the mirroring accuracy without reducing signal swing. The output impedance (R_{comp}) of composite transistor $M_5 - M_6$ is given as in (3.17) including the body effect of M_6.

$$R_{comp} = r_{o5} + r_{o6} + (g_{m6} + g_{mb6})r_{o5}r_{o6} \tag{3.17}$$

In Figure 3.3a, composite transistors $M_5 - M_6$ and $M_7 - M_8$ are used to mirror the bias current to NMOS and PMOS SF LPFs respectively. Current mirror circuit shown in Figure 3.3b is used to mirror these bias currents. Transistors $M_5 - M_{14}$ (in Figure 3.3a and Figure 3.3b) are sized in such a way that a bias current of 5 nA flows in both NMOS and PMOS SF LPFs. M_{15} is biased by a biasing circuit shown in Figure 3.4 to provide this 5 nA bias current. The aspect ratios of transistors and values of all components in Figure 3.3 are given in Table 3.1.

-3 dB frequency (f_{-3dB}) is considered as cutoff frequency for the 2^{nd} order LPF. If the cutoff frequency of NMOS and PMOS SF LPFs is f_{c1}, then f_{-3dB} of the 2^{nd} order

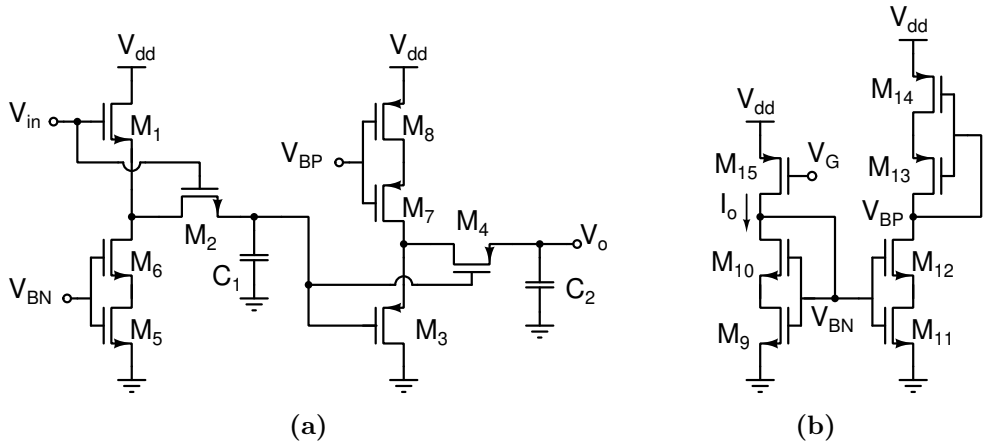


Figure 3.3: (a) 2^{nd} order LPF, (b) Current mirror for biasing filter circuit.

Table 3.1: Aspect ratios of transistors and values of all components in Figure 3.3.

Transistors	$\boldsymbol{W/L(\mu m/\mu m)}$	**Capacitors**	**pF**
M_1, M_6, M_{10}, M_{12}	20/3		
M_2, M_5, M_9, M_{11}	1/3		
M_3	80/3	C_1, C_2	4
M_4, M_8, M_{14}	2/3		
M_7, M_{13}	40/3		
M_{15}	10/3		

LPF is given by (3.18) (Sawigun and Serdijn 2016).

$$f_{-3dB} = f_{c1}\sqrt{\sqrt{2}-1} \tag{3.18}$$

For f_{-3dB} of 100 Hz, f_{c1} is calculated as 155.4 Hz. Therefore, sizes of transistors are chosen in such a way that both NMOS and PMOS LPFs offer the same f_c of 155.4 Hz. C_1 and C_2 are calculated as 4 pF.

3.2.3 Biasing Circuit

Constant current of 5 nA is generated from the biasing circuit shown in Figure 3.4. In this, a PTAT, I_2 of value 5 nA is subtracted from another PTAT current, I_1 of value 10 nA to get a constant current, I_o of 5 nA. This biasing circuit is based on the constant current generator circuit given in (Amaljith *et al.* 2018). The aspect ratios

of transistors and values of all components of Figure 3.4 are given in Table 3.2.

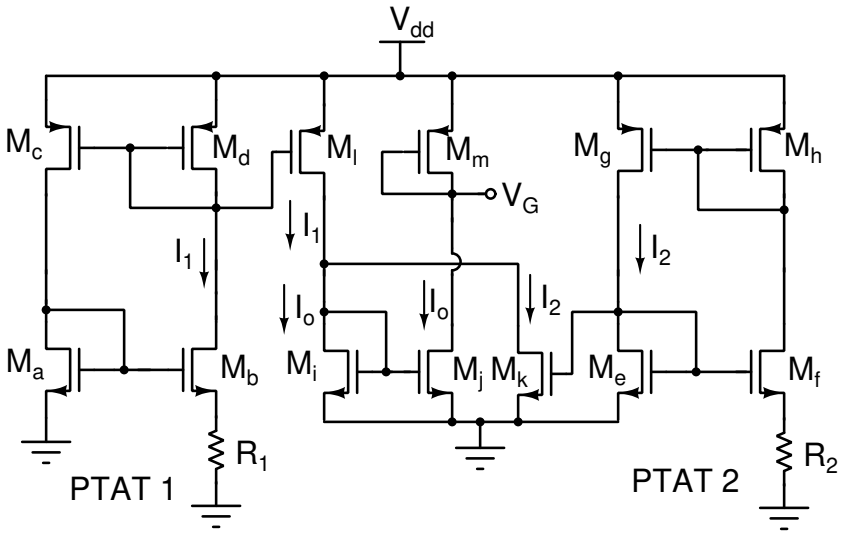


Figure 3.4: Biasing circuit.

Table 3.2: Aspect ratios of transistors and values of all components in Figure 3.4.

Transistors	$W/L(\mu m/\mu m)$	**Resistors**	**MΩ**
M_a, M_e, M_{i-k}	2/1		
$M_{c-d}, M_{l-m}, M_{g-h}$	10/1	R_1	5.6
M_b	8.5/1	R_2	2
M_f	2.4/1		

3.2.4 Post-layout Simulation Results

The frequency response of the basic SF LPF (Figure 3.1) and the proposed SF LPF (Figure 3.2a) are shown in Figure 3.5. The DC gain of both the filters is -1.2 dB. For $I_o = 5$ nA and $C = 4$ pF, cutoff frequency of basic SF LPF and proposed SF LPF are 7 kHz and 155 Hz respectively. For the same I_o and C values, cutoff frequency of the proposed SF LPF is reduced by more than 1.65 decades. Hence, using the proposed design of LPF, low frequency filters can be designed without requiring large area trade-off of capacitors.

Table 3.3 lists the simulated values of R_{o2}, g_{m1} and g_{mb1} for different bias currents. It is observed that $R_{o2} \gg 1/(g_{m1}+g_{mb1})$. As I_o increases, $R_{o2}+1/(g_{m1}+g_{mb1})$ reduces

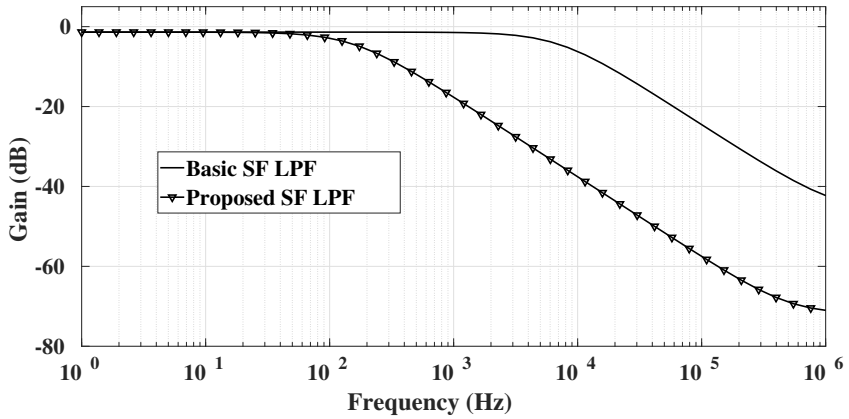


Figure 3.5: Frequency response of the circuits in Figure 3.1 and Figure 3.2a.

almost linearly. Therefore, the cutoff frequency of the filter can be tuned linearly by varying I_o (refer 3.12).

Table 3.3: R_{o2}, g_{m1} and g_{mb1} values for the proposed SF LPF (Figure 3.2a)

$\boldsymbol{I_o}$ (nA)	$\boldsymbol{R_{o2}}$ (MΩ)	$\boldsymbol{g_{m1}}$ (nS)	$\boldsymbol{g_{mb1}}$ (nS)	$\boldsymbol{1/(g_{m1}+g_{mb1})}$ (MΩ)	$\boldsymbol{R_{o2}+1/(g_{m1}+g_{mb1})}$ (MΩ)
0.5	2423.5	16.2	2.6	53.2	2476.7
5	242.2	157.66	26	5.44	247.64
50	23.69	1458	247	0.586	24.3

Table 3.4 lists the simulated values of R_{o2} for different temperatures. It is observed that the variation in R_{o2} is less than ± 2.1 % in the temperature range of 0 - 70°C from the value at room temperature. Hence, variation in the cut-off frequency of the filter will be small as temperature varies. Whereas, in the basic SF filter (Figure 1), cutoff frequency is inversely proportional to temperature and hence, a PTAT current reference circuit is required to make it independent of temperature.

Table 3.4: R_{o2} variation with temperature for $I_o = 5$ nA

Temperature (°C)	0	27	70
$\boldsymbol{R_{o2}}$ (MΩ)	247.4	242.2	237.4

Figure 3.6 shows the working principle of the biasing circuit (Figure 3.4). A constant current (I_o) of 5 nA is generated by two PTAT current sources (I_1 and I_2) of 10

nA and 5 nA. It is observed that I_o is constant in the temperature range of 0 - 70°C. Figure 3.7 shows the variation of I_o with the supply voltage. I_o is almost constant in the supply voltage range of 0.6 - 1 V.

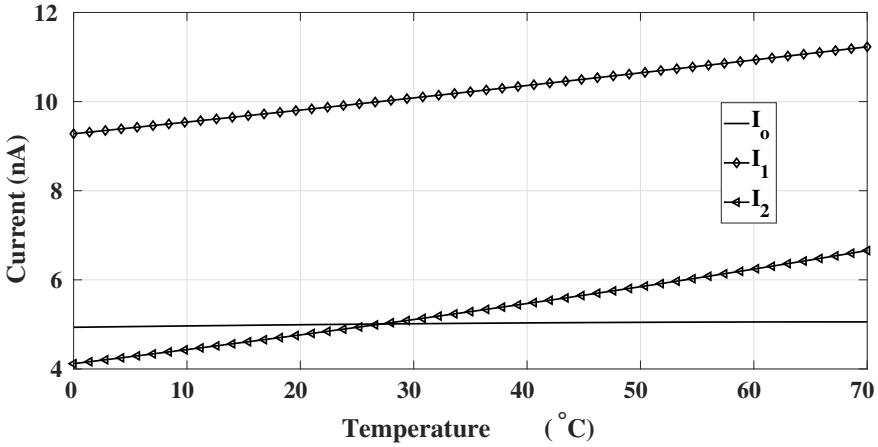


Figure 3.6: I_o variation with temperature

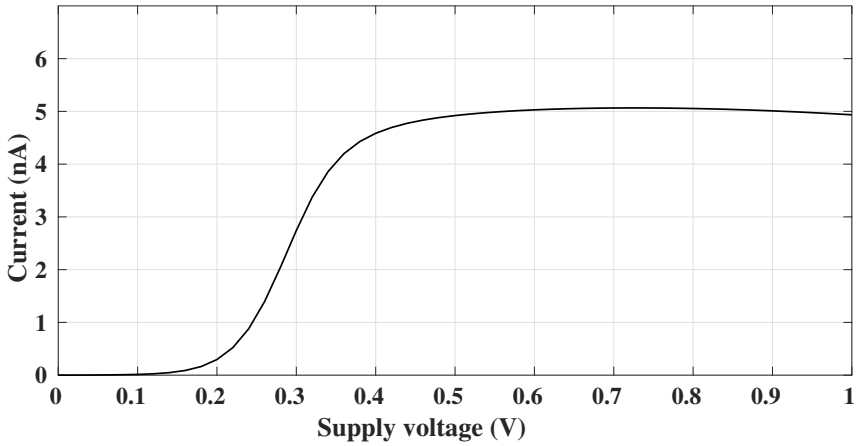


Figure 3.7: I_o variation with supply voltage

The 2^{nd} order LPF circuit is laid out (shown in Figure 3.8) and post layout simulations are performed. It takes an area of 0.0081 mm^2. MIM (metal insulator metal) capacitors are used in the layout. The frequency response of the 2^{nd} order LPF (Figure 3.3a) is shown in Figure 3.9. The DC gain and f_{-3dB} are -2.47 dB and 100 Hz respectively. Input common mode voltage is fixed at 0.4 V. Output common mode voltage is observed as 0.43 V. It changes by ±5 mV across all the process corners.

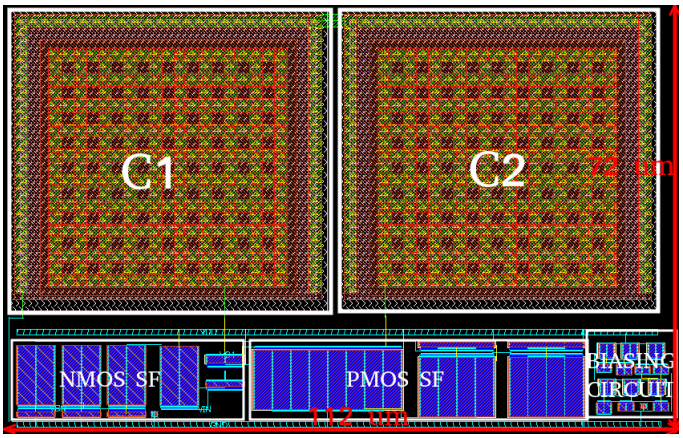


Figure 3.8: Layout of the 2^{nd} order SF LPF with biasing circuit

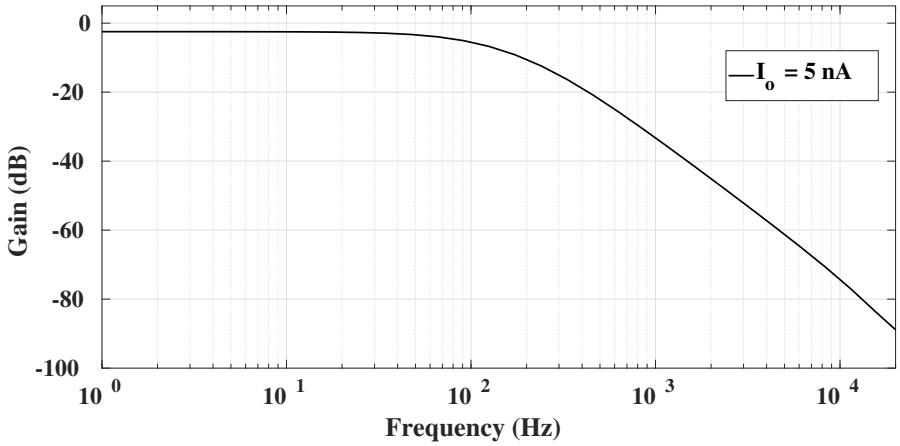


Figure 3.9: Frequency response of the 2^{nd} order SF LPF

Linearity is checked with an input sinusoidal signal of frequency 20 Hz. Total harmonic distortion (THD) of 1 % is observed for an input voltage 140 mVpp. The output noise is shown in Figure 3.10. At lower frequencies flicker noise is more dominant and after 10 Hz, thermal noise dominates. IRN integrated over 1 - 110 Hz is found to be 40 μV RMS. The DR is calculated as 61.85 dB.

FoM1 of the proposed 2^{nd} order LPF is calculated to be 3.23×10^{-14} J. f_{-3dB} can be tuned from 10 Hz to 1 kHz by varying I_o from 0.5 nA to 50 nA as shown in Figure 3.11. I_o can be varied by varying R_1 and R_2 (off chip resistors) in the biasing circuit (Figure 3.4). It can be seen that f_{-3dB} is linearly increasing with I_o as shown in Figure 3.12. f_{-3dB} can be tuned to the required value by controlling the bias current I_o.

Parameters of the proposed 2^{nd} order LPF are summarized in Table 3.5. The power

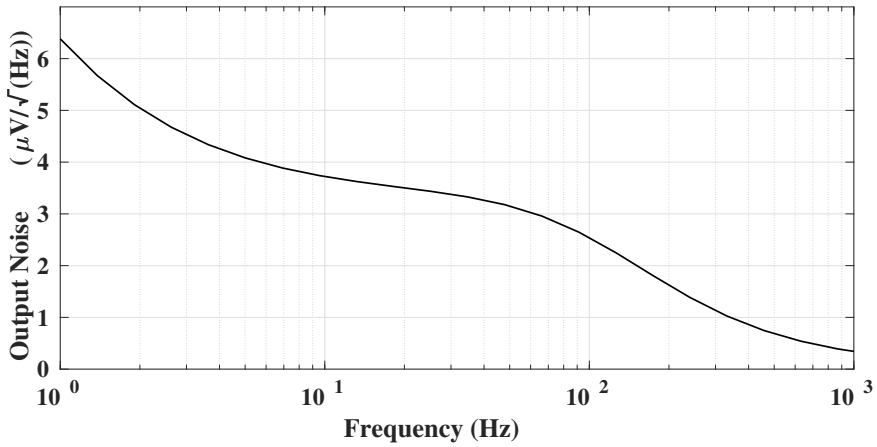


Figure 3.10: Output noise of the 2^{nd} order SF LPF

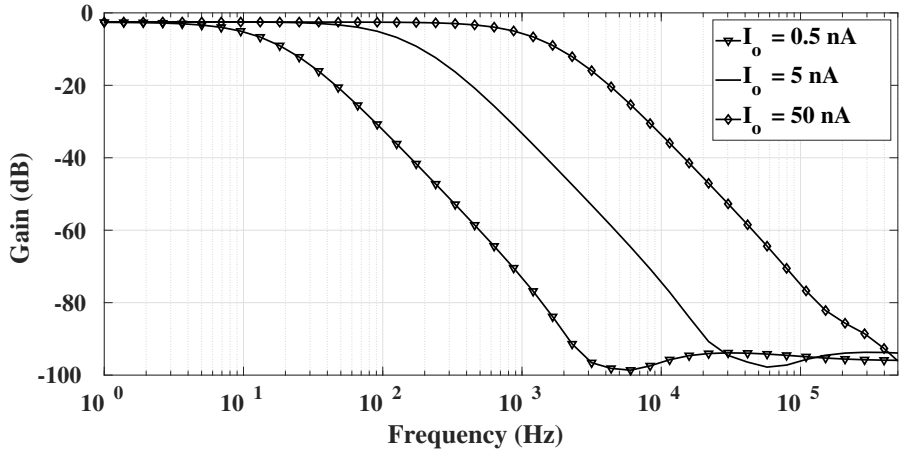


Figure 3.11: Frequency response of the 2^{nd} order SF LPF for different bias currents

consumption of the filter is as low as 8 nW for an f_{-3dB} of 100 Hz. The comparison of the proposed design with other similar designs is given in Table 3.6. Major area of the filter circuit is occupied by capacitors. So, capacitance/pole is used as one of the performance-measures in the state-of-the-art filters with different orders. It can be seen that the proposed filter has the lowest FoM1 and capacitance/pole of all the filters listed. Input peak-to-peak voltage for 1 % THD of the proposed circuit is more compared to (Zhang *et al.* 2013, Mahmoud *et al.* 2013, Arya and Oliveira 2016) even though those circuits use higher supply voltages. In addition, DR offered by the proposed circuit is comparable to other listed references in Table 3.6.

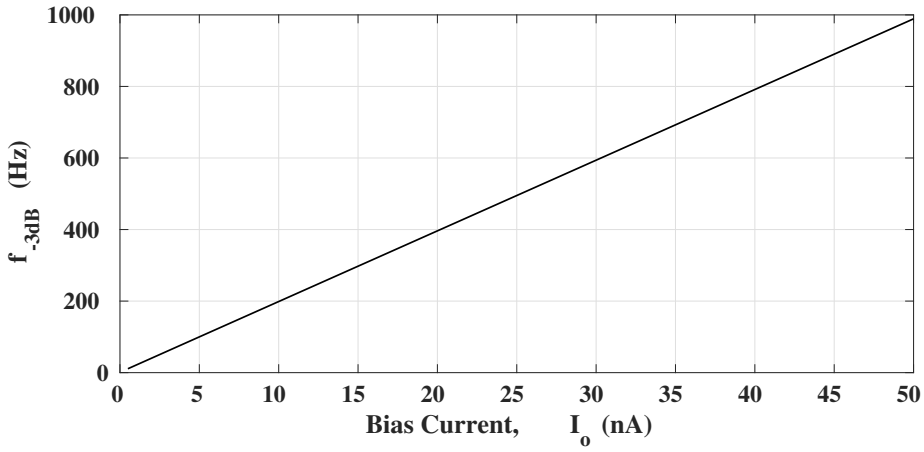


Figure 3.12: f_{-3dB} versus I_o

Table 3.5: Parameters of the 2^{nd} order SF LPF.

Parameters	**Simulated values**
Technology	UMC 65 nm
V_{dd}	0.8 V
DC gain	-2.47 dB
f_{-3dB}	100 Hz
V_{inpp} for 1% THD	140 mVpp
IRN	40 μV RMS
DR	61.85 dB
Power Consumption	8 nW †
FoM1	$3.23 * 10^{-14}$ J
f_{-3dB} tuning range	10 Hz to 1 kHz
Total Capacitance	8 pF
Active area	0.0081 mm^2

† Excluding the power of biasing circuit.

3.2.4.1 Effect of PVT variations on f_{-3dB}

Figure 3.13 shows the histogram of f_{-3dB} obtained for 200 runs. The mean (μ) of about 100.3 Hz and standard deviation (σ) of about 7.5 Hz are observed.

For a $\pm$ 10 % variation in V_{dd}, f_{-3dB} variation is only $\pm$ 1 % as shown in Figure 3.14. The deviation of < 5 % in f_{-3dB} is observed for a temperature range of $0 - 70°C$

Table 3.6: Comparison of the proposed 2^{nd} order LPF with other similar designs.

Parameter	Rodriguez-Villegas *et al.* 2011	Liu *et al.* 2012	Mahmoud *et al.* 2013	Zhang *et al.* 2013	Arya and Oliveira 2016	Rao and Rekha 2018	**This Work**
Technology (nm)	350	350	250	350	130	180	**65**
V_{dd} (V)	1	3	± 0.8	3	0.9	0.5	**0.8**
Filter order	1	4	5	4	2	2	**2**
Cutoff frequency (Hz)	1	40	243	100	48	456	**100**
Power (nW)	5	750	3X10^4	15	800	248	**8**
V_{inpp} for 1 % THD (mV)	140	735	100	50	7	180	**140**
IRN (μV RMS)	32	500	36	29	17.38	160	**40**
DR (dB)	63.8	54	65	64.8	43.8	52	**61.85**
Capacitance / pole (pF)	40	–	4.16	27.2	69.4	30	**4**
Active area (mm^2)	0.07	–	0.09	0.08	–	–	**0.0081**
FoM1 (J) (X10^{-14})	323	935	1388	57.9	5380	68.3	**3.23**

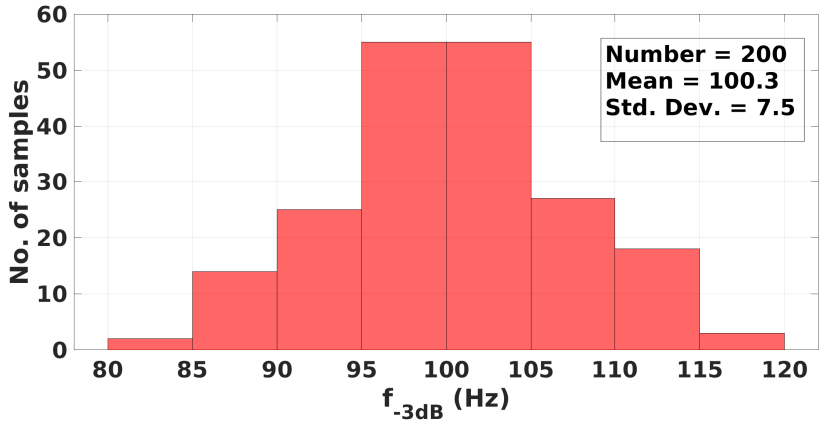


Figure 3.13: Histogram of f_{-3dB} using Monte Carlo simulation with 200 runs.

as shown in Figure 3.15. This deviation is due to the variation of R_{o2} with temperature as given in Table 3.4. The deviation in f_{-3dB} across PVT variations is summarized in Table 3.7. Results show that the design is robust across PVT variations. f_{-3dB} can

be tuned back to its nominal value of 100 Hz by adjusting I_o.

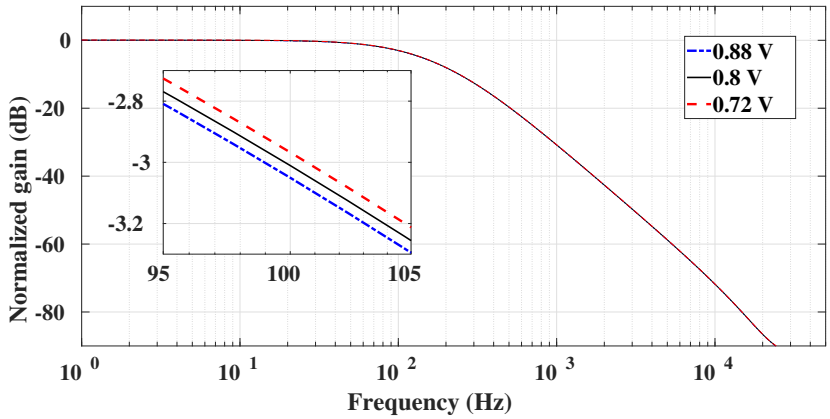


Figure 3.14: f_{-3dB} variation for various supply voltages.

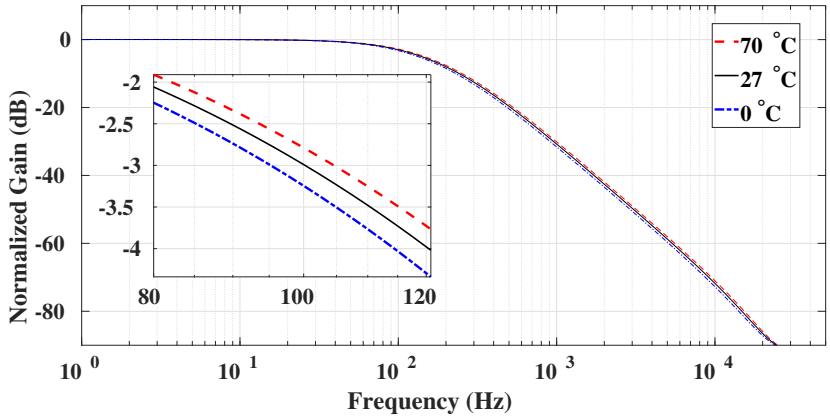


Figure 3.15: f_{-3dB} variation for various temperatures.

Table 3.7: f_{-3dB} across PVT variations.

	Process & Mismatch (Monte Carlo 200 runs)	V_{dd} ($\pm$ 10 %)	Temperature ($0 - 70°C$)
f_{-3dB}	100 $\pm$ 7.5 Hz	100 $\pm$ 1 Hz	95 - 104 Hz

3.3 Ultra Low-voltage VF LPF

The proposed bulk-driven voltage follower (BD-VF) is shown in Figure 3.16a. The input signal is applied to the bulk terminal of M_1. The bulk, drain terminals of M_2 and drain of M_1 are shorted together. Transistor M_2 (with bulk connected to drain terminal) makes the gain of the circuit approximately equal to unity as explained later in this section. An integrating capacitor (C) connected at the output node makes the circuit a first order LPF.

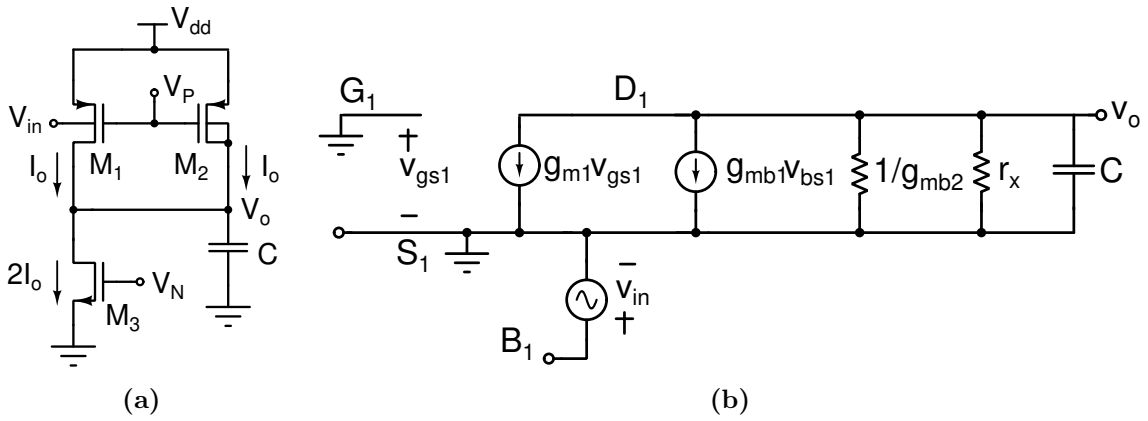


Figure 3.16: (a) Proposed BD-VF, (b) Small signal equivalent circuit.

Figure 3.16b shows the small signal equivalent of the proposed BD-VF. Here, $r_x = r_{o1} \parallel r_{o2} \parallel r_{o3}$. All the terms have their usual meanings. The expression for the transfer function can be derived as follows. By applying KCL at node D_1,

$$g_{m1}v_{gs1} + g_{mb1}v_{bs1} + v_o(g_{mb2} + \frac{1}{r_x} + Cs) = 0 \tag{3.19}$$

By substituting $v_{gs1} = 0$, $v_{bs1} = v_{in}$ in (3.19) and simplifying, we get the transfer function, $H(s)$.

$$H(s) = -\frac{\frac{g_{mb1}r_x}{1+g_{mb2}r_x}}{1 + \frac{r_x}{1+g_{mb2}r_x}Cs} \tag{3.20}$$

From (3.20), the DC gain (A_o) and the time constant (τ) can be expressed as

$$A_o = -\frac{g_{mb1}r_x}{1 + g_{mb2}r_x} \tag{3.21}$$

$$\tau = \frac{r_x C}{1 + g_{mb2}r_x} \tag{3.22}$$

As $g_{mb2}r_x \gg 1$, (3.22) is simplified to (3.23) and the cutoff frequency is given by (3.24).

$$\tau \approx \frac{C}{g_{mb2}} \tag{3.23}$$

$$f_c = \frac{1}{2\pi\tau} = \frac{g_{mb2}}{2\pi C} \tag{3.24}$$

From Figure 3.16b, the output resistance (R_{out}) by considering $g_{mb2}r_x \gg 1$, can be written as

$$R_{out} = \frac{1}{g_{mb2}} \tag{3.25}$$

In (3.21), DC gain can be made unity, by making g_{mb1} slightly greater than g_{mb2}. Hence, sizes of M_1 and M_2 are chosen in such a way that slightly more bias current flows through M_1 than M_2.

A fully differential configuration of the proposed BD-VF is shown in Figure 3.17a. It is biased by a current mirror circuit shown in Figure 3.17b. A bias current of I_o flows through M_1, M_2, M_4 & M_5 and $2I_o$ flows through M_3 & M_6. Sizes of transistors (shown in Table 3.8) are chosen to ensure the sub-threshold saturation operation and for proper current mirroring. Integrating capacitance, $C/2$ is connected between output nodes V_{op} and V_{om}.

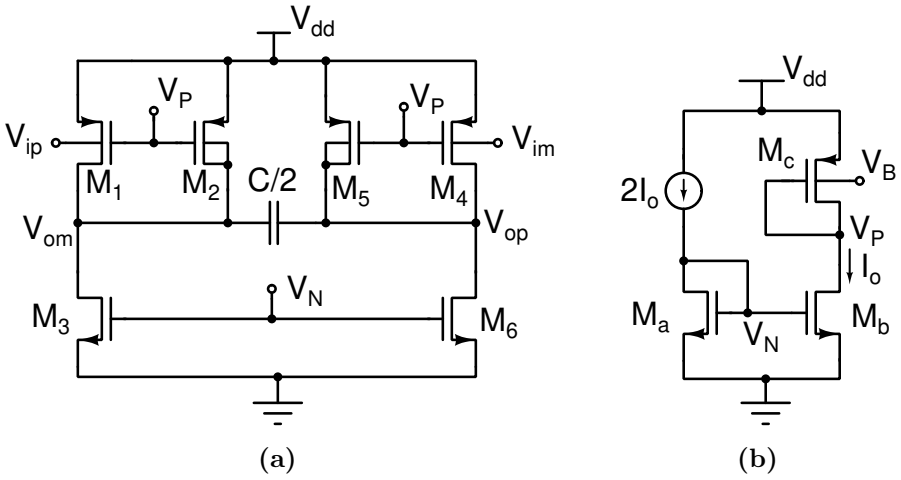


Figure 3.17: (a) Fully differential configuration of the proposed BD-VF, (b) Current mirror for biasing.

The proposed BD-VF operates from 0.3 V supply voltage. Bulk voltages of M_c and M_1 are at input common mode of 150 mV. Since the source-gate as well as bulk

Table 3.8: Transistor sizes in Figure 3.17

Transistors	W/L (μm/μm)
M_1, M_4	24/1
M_2, M_5	21.2/1
M_3, M_6, M_a	10.6/15
M_b	5.3/15
M_c	22.6/1

voltages of M_c and M_1 are same, the current I_o is mirrored to M_1. This forces the remaining current I_o to flow through M_2. As source-gate voltages as well as drain currents of M_c and M_2 are same, and bulk and drain of M_2 are shorted together, output common mode is set to 150 mV. This circumvents the need for common mode feedback (CMFB) circuit, which is mandatory in most of the differential-in differential-out configurations.

3.3.1 Noise analysis

Figure 3.18 shows the noise equivalent of the proposed BD-VF. It shows all the transistors along with their noise sources. The power spectral density (PSD) of output voltage noise is given by

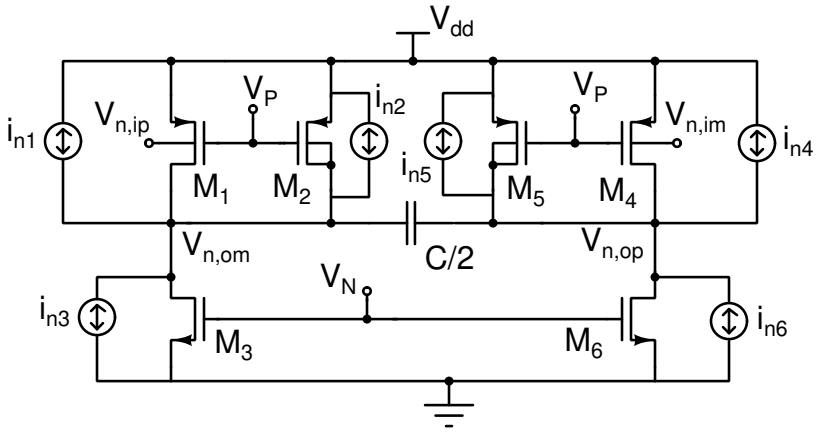


Figure 3.18: Noise equivalent of proposed BD-VF

$$\overline{v_{on}^2} = \sum_{i=1}^{6} \overline{i_{ni}^2} R_{out}^2 \tag{3.26}$$

where $\overline{i_{ni}^2}$ is the current noise PSD of i^{th} transistor. The PSDs of thermal noise and flicker noise $(1/f)$ of a transistor are given by (3.27) and (3.28) respectively (Razavi 2002).

$$\overline{i_{n,th}^2} = \frac{8}{3}kTg_m \tag{3.27}$$

$$\overline{i_{n,1/f}^2} = \frac{K_f}{C_{ox}WL}.\frac{1}{f}.g_m^2 \tag{3.28}$$

where k is the Boltzmann constant and K_f is the flicker noise parameter. By substituting (3.27) in (3.26), the PSD of output thermal noise voltage is given by

$$\overline{v_{on,th}^2} = \frac{8}{3}kTR_{out}^2\sum_{i=1}^{6} g_{mi} \tag{3.29}$$

where g_{mi} is the transconductance of i^{th} transistor. To make the analysis easier, the transconductances of the transistors M_1, M_2, M_4 and M_5 can be considered to be equal to g_{m2} as approximately same bias current (I_o) flows through them. Similarly, transconductance of M_3 and M_6 is considered to be equal to g_{m3}. By substituting $R_{out} = 1/g_{mb2}$ in (3.29),

$$\overline{v_{on,th}^2} = \frac{16kT}{3}\frac{g_{m2}}{g_{mb2}^2}\Big[2 + \frac{g_{m3}}{g_{m2}}\Big] \tag{3.30}$$

By simplifying (3.30),

$$\overline{v_{on,th}^2} = \frac{16kT}{3}\frac{1}{(\eta_p - 1)g_{mb2}}\Big[2 + \frac{2\eta_p}{\eta_n}\Big] \tag{3.31}$$

where η_n and η_p are the sub-threshold slope factors of NMOS and PMOS respectively. Output thermal noise power integrated over the frequency range, 0 to f_o is given by

$$P_{on,th} = \frac{32kT}{3}\frac{1}{(\eta_p - 1)g_{mb2}}\Big[1 + \frac{\eta_p}{\eta_n}\Big]\int_0^{f_o} |\frac{1}{1 + j(\frac{f}{f_o})}|^2\, df \tag{3.32}$$

$$\Rightarrow P_{on,th} = \frac{4kT}{3(\eta_p - 1)C}\Big[1 + \frac{\eta_p}{\eta_n}\Big] \tag{3.33}$$

Similarly, the PSD of output flicker noise voltage can be written as

$$\overline{v_{on,1/f}^2} = \frac{4}{C_{ox}(\eta_p - 1)^2 f}.\Big[\frac{K_{fp}}{(WL)_2} + \frac{K_{fn}}{(WL)_3}.\frac{2\eta_p^2}{\eta_n^2}\Big] \tag{3.34}$$

where K_{fp} and K_{fn} are flicker noise parameters for PMOS and NMOS transistors respectively. From (3.34), it can be seen that the flicker noise can be reduced by increasing WL of the transistors. Hence, for the proposed design, W and L are chosen sufficiently large as given in Table 3.8.

3.3.2 4^{th} order VF LPF

A 4^{th} order LPF is designed by cascading four proposed BD-VFs with same cutoff frequency. Figure 3.19 shows the block diagram of the 4^{th} order LPF whose transfer function can be written as

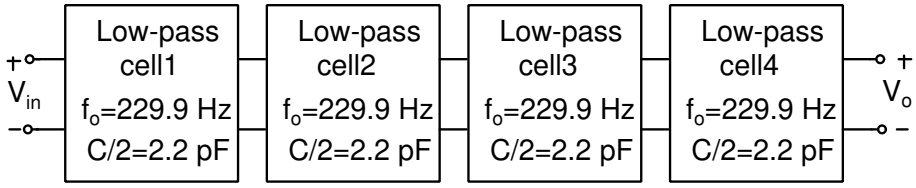


Figure 3.19: 4^{th} order VF LPF

$$H_4(s) = \frac{1}{(1 + j(\frac{f}{f_c}))^4} \tag{3.35}$$

where, f_c is the cutoff frequency of the first order LPF. -3 dB frequency (f_{-3dB}) of 100 Hz for the 4^{th} order LPF translates into an f_c of 229.9 Hz for individual stages according to (3.36).

$$f_{-3dB} = f_c\sqrt{2^{\frac{1}{4}} - 1} \tag{3.36}$$

3.3.3 Post-layout Simulation Results

The 4^{th} order filter is implemented using UMC 180 nm CMOS technology. The layout of the filter is shown in Figure 3.20. It takes an area of 0.03 mm^2. Frequency response of the filter is shown in Figure 3.21. The cutoff frequency and DC gain of the filter are 100 Hz and 0 dB respectively.

A 20 Hz sinusoidal signal is applied to the filter to check its linearity. The observed THD is 1 % for 130 mVpp input. Further, THD is plotted against input frequency (f_{in}) as shown in Figure 3.22a. It is observed that THD is almost 1 % upto an f_{in} of 50 Hz. At 100 Hz, the THD is only 0.53 % as the higher order harmonics are

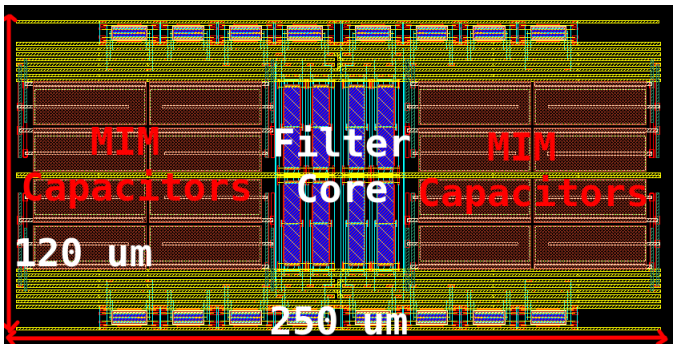


Figure 3.20: Layout of VF LPF.

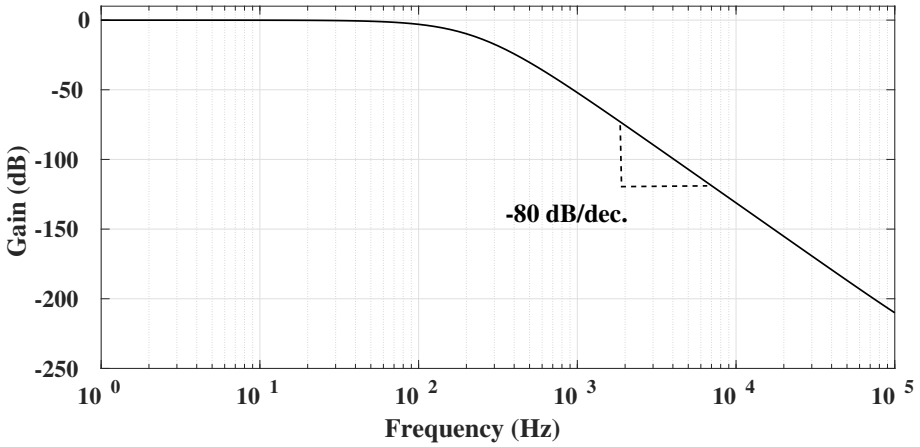


Figure 3.21: Frequency response of VF LPF.

attenuated in the stop band. Figure 3.22b shows the output spectrum of the filter for an input signal of 130 mVpp amplitude and 20 Hz frequency. As the proposed filter is a differential structure, even harmonics are almost eliminated and only odd harmonics are present. The observed HD_3 is approximately -40 dB. Figure 3.22c shows output noise of the filter. IRN integrated over the frequency range, 1 - 100 Hz is 73.5 μVrms. The DR and FoM2 of the filter are calculated to be 56 dB and 5.7×10^{-15} respectively.

Figure 3.23 shows the frequency response of the filter for various bias currents. The cutoff frequency can be tuned from 50 Hz to 250 Hz by varying the bias current, I_o from 0.48 nA to 2.6 nA. Table 3.9 shows the parameters of the 4^{th} order LPF. Performance of the proposed filter is compared with other benchmark designs from literature as shown in Table 3.10. The proposed filter achieves a DR of 56 dB while operating with an extremely low supply voltage of 0.3 V. Further, it shows very good

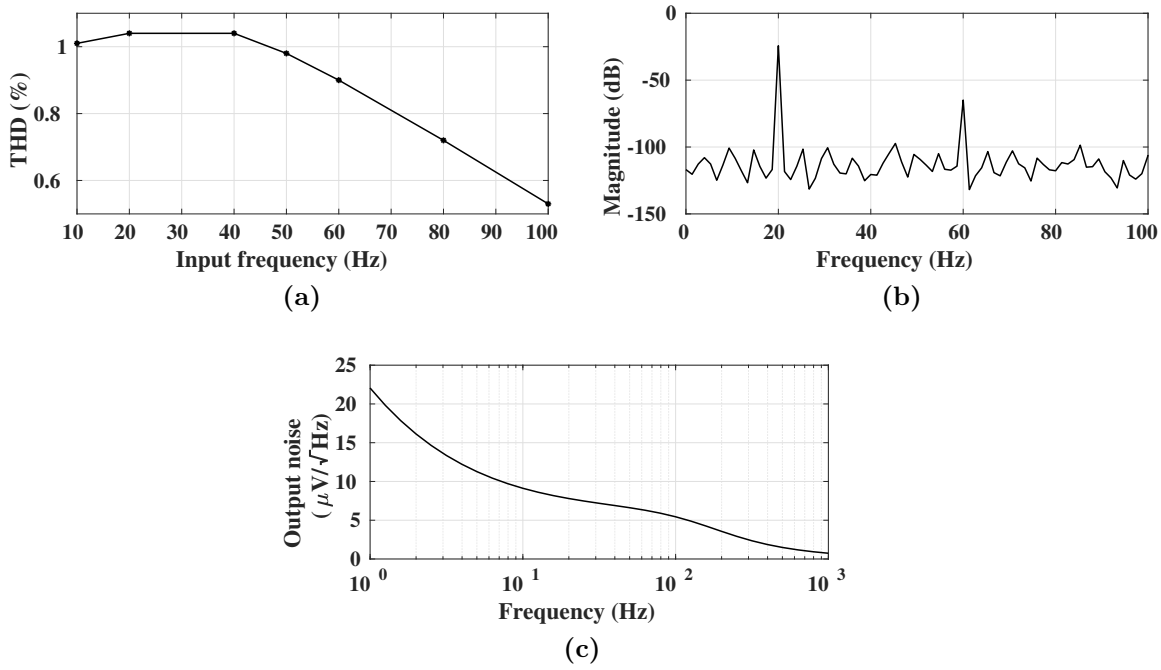


Figure 3.22: VF LPF (a) THD versus f_{in}, (b) Harmonics, (c) Output noise.

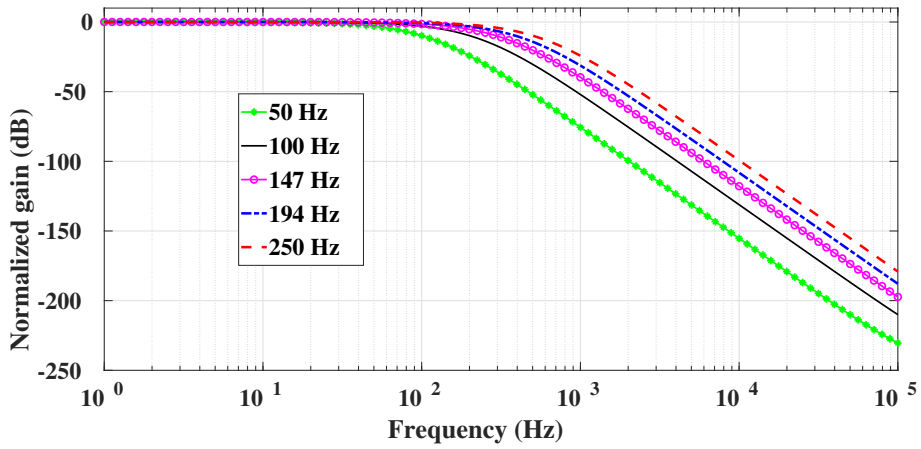


Figure 3.23: f_{-3dB} tuning of the filter. The results are in the format [I_o, f_{-3dB}]: [0.48 nA, 50 Hz], [1 nA, 100 Hz], [1.5 nA, 147 Hz], [2 nA, 194 Hz] and [2.6 nA, 250 Hz].

performance as far as power dissipation, FoM2 and capacitance/pole are concerned. Power consumption is as less as 4.8 nW. FoM2 of the proposed filter is the least among other designs listed. Filter requires very less capacitance/pole (2.2 pF) and hence is area efficient too.

Table 3.9: Parameters of the 4^{th} order VF LPF for $I_o = 1$ nA.

Parameter	Value
Technology	UMC 180 nm
V_{dd}	0.3 V
f_{-3dB}	100 Hz
DC gain	0 dB
Tuning range of f_{-3dB}	50 - 250 Hz
V_{inpp} @ 1% THD	130 mVpp
IRN	73 μV RMS
DR	56 dB
Power	4.8 nW
FoM2	5.7×10^{-15}
Total Capacitance	8.8 pF
Active area	0.03 mm^2

3.3.4 PVT and Monte Carlo simulations

Figure 3.24 shows the frequency response of the filter across process corners ('ss', 'tt' and 'ff'). f_{-3dB} is 100.4 Hz and 99.6 Hz in 'ss' and 'ff' corners respectively, which are the worst case deviations. For ±10 % V_{dd} variations, the deviation in f_{-3dB} is less than ±2.8 % as shown in Figure 3.25. f_{-3dB} is 106 Hz and 95 Hz at 0°C and 70°C respectively as shown in Figure 3.26. The summary of PVT variations is given in Table 3.11.

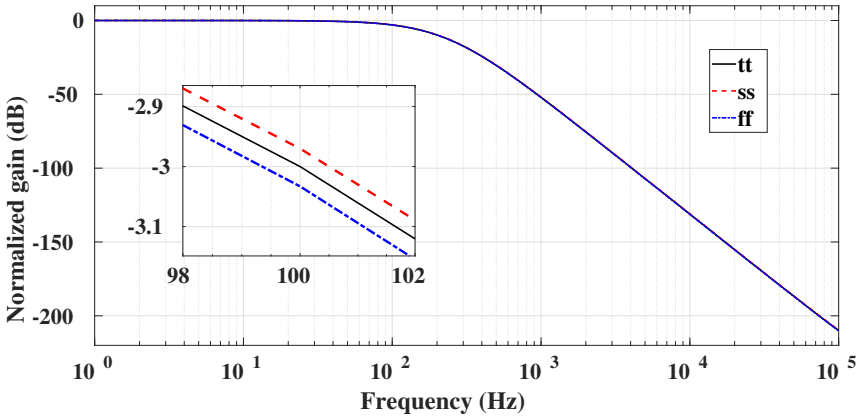


Figure 3.24: Frequency response of the filter across process corners.

Further, Monte Carlo simulations are carried out to observe the deviation in f_{-3dB}

Table 3.10: Performance comparison of 4^{th} order VF LPF with other similar designs.

Parameter	Lee and Cheng 2009†	Sawigun and Serdijn 2012**	Zhang *et al.* 2013†	Arya and Oliveira 2016*	Rao and Rekha 2018*	Sun and Lee 2018†	Krishna and Laxminidhi 2018**	Thanapitak and Sawigun 2018†	Sawigun and Thanapitak 2019†	**This Work****
Technology (nm)	180	180	350	130	180	180	180	350	350	**180**
V_{dd} (V)	1	1	3	0.9	0.5	1	1.8	0.9	1.5	**0.3**
Filter order	5	2	4	2	2	5	4	4	4	**4**
DC gain (dB)	-10.5	0	-3.7	5.99	≈0	-7	0	-0.05	-0.09	**0**
Cutoff frequency (Hz)	250	76	100	48	456	250	50	100	100	**100**
Power (nW)	453	900	15	800	248	41	570	4.26	5.25	**4.8**
V_{inpp} for 1 % THD (mV)	100	1220	50	7	180	100	196	70	110	**130**
IRN_{rms} (μV)	≈300	266	36	17.38	160	134	109	80.5	39.38	**73.5**
DR (dB)	50	64	66.7	43.8	52	61.2	56.1	48.2	56.9	**56**
Capacitance / pole (pF)	1.4	39	27.2	139	30	3.9	35.6	9.6	11.8	**2.2**
Active area (mm^2)	0.13	0.034	0.11	–	–	0.24	0.74	0.11	0.1	**0.03**
FoM2 ($\times 10^{-15}$)	1146	3.7 k	51.9	48.4 k	341.5	28.6	7.9 k	37.3	28	**5.7**

† measured; * schematic simulations; ** post-layout simulations.

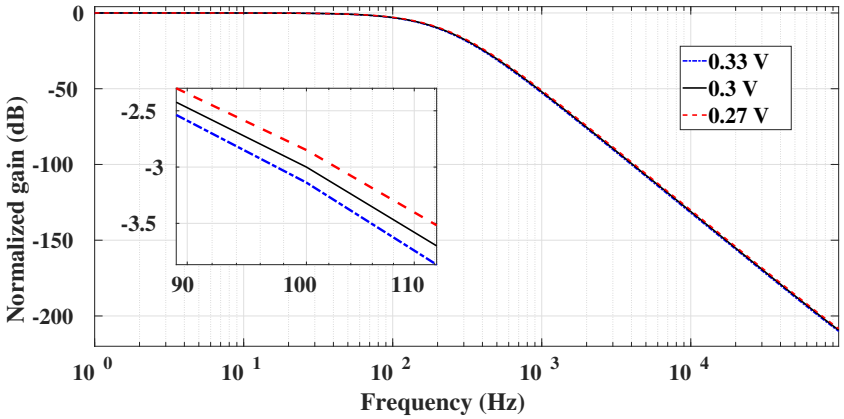


Figure 3.25: Frequency response of the filter across V_{dd} variations.

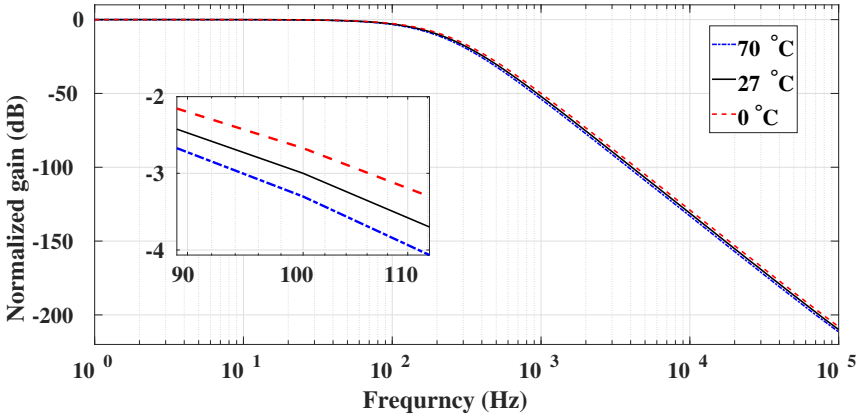


Figure 3.26: Frequency response of the filter across temperature variations.

Table 3.11: Summary of PVT variations

	Process corners					V_{dd}	Temperature
	tt	ss	ff	fnsp	snfp	(±10 %)	0 - 70°C
f_{-3dB} (Hz)	100	100.4	99.6	99.9	100.1	100 ± 2.8	106 - 95

and DC gain across process variations and device mismatch. Figure 3.27a and Figure 3.27b show the histogram of f_{-3dB} and DC gain respectively for 200 runs of Monte Carlo simulations. The mean of f_{-3dB} is 100.5 Hz with standard deviation of 3.5 Hz. The mean and standard deviation of DC gain are -0.24 dB and 0.64 dB respectively.

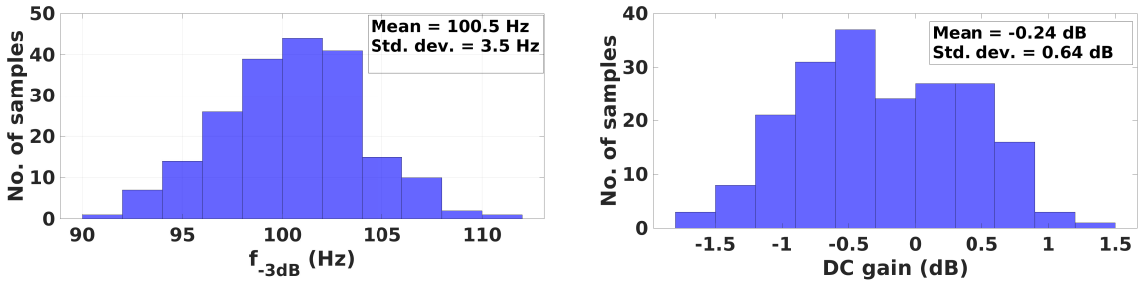
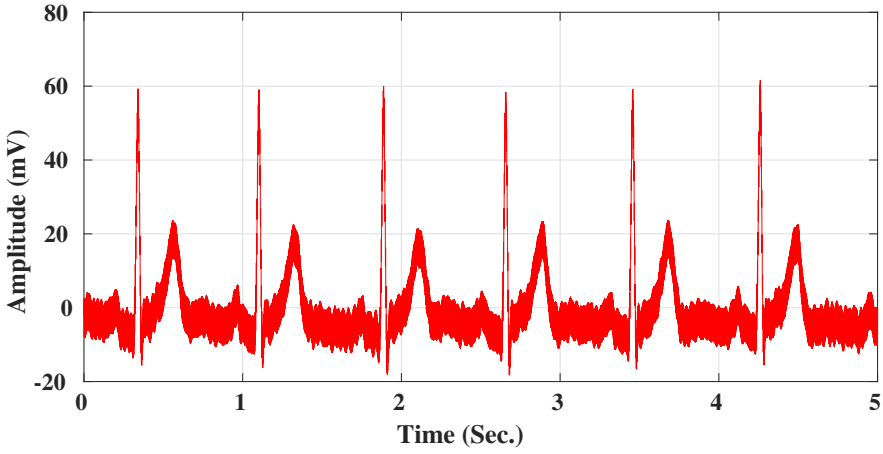


Figure 3.27: Monte Carlo simulations of (a) f_{-3dB}, (b) DC gain.

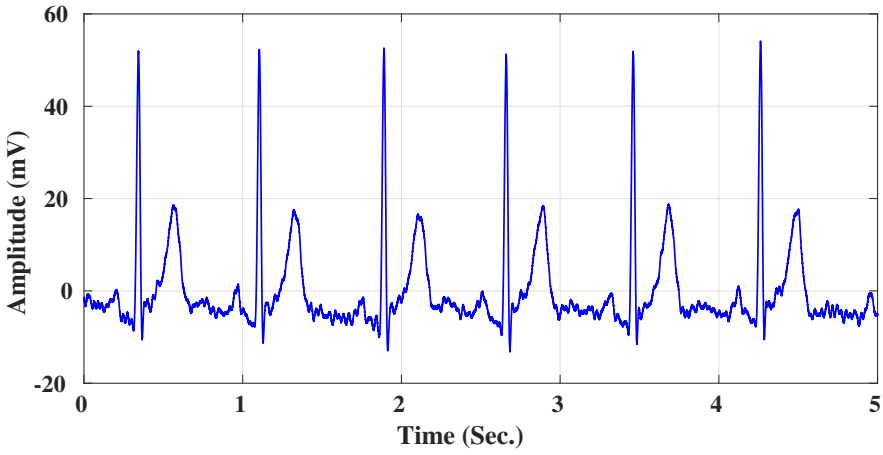
3.3.5 ECG signal testing

The highest frequency component of the ECG signal lies in the range, 100 Hz to 250 Hz (Thanapitak and Sawigun 2018). Therefore, the LPF has to have a tunable cutoff frequency of the same range and the DR of at least 44 dB (Thanapitak and Sawigun 2018). The proposed filter has a tunable cutoff frequency from 50 Hz to 250 Hz and a DR of 56 dB. Hence, it can be used in the pre-processing of the ECG signal.

The functionality of the proposed filter is demonstrated by filtering out-of-band noise from a noisy ECG signal as shown in Figure 3.28. The noisy ECG signal (Figure 3.28a) is generated by adding an out-of-band noise (10 mVpp, 400 Hz sinusoidal) to an ECG signal obtained from (Goldberger *et al.* 2000). The out-of-band noise is removed by the filter as shown in Figure 3.28b.



(a)



(b)

Figure 3.28: ECG signal (a) before filtering, (b) after filtering.

Chapter 4

AREA EFFICIENT LOG DOMAIN FILTER DESIGN

The area efficient time constant enhancement technique proposed in section 3.2 has been applied to log domain filter. Using this technique, a 2^{nd} order log domain LPF is implemented using UMC 65 nm CMOS technology.

The basic first order log domain filter (Frey 2000) is shown in Figure 4.1. All the transistors ($M_1 - M_4$) are operating in sub-threshold region and form a translinear loop. Here, the current sources, $I_1 - I_3$ are used to bias the circuit. i_{in}, i_{out} are the input and output signal currents and v_{in}, v_c are the internal compressed voltages. i_{in} is compressed to v_{in} by M_1 and M_2. The signal current in M_3 (due to v_{in}) is integrated by the capacitor, C to produce v_c. Finally, v_c is expanded by M_4 to produce i_{out}. By neglecting the second order effects of all the transistors, the transfer function and time constant of the basic log domain filter are given by (4.1) and (4.2) respectively (Frey 2000).

$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{I_2/I_3}{1 + s(\frac{\eta V_T C}{I_3})} \tag{4.1}$$

$$\tau = \frac{\eta V_T C}{I_3} \tag{4.2}$$

By substituting $\frac{I_3}{\eta V_T} = g_{m3}$, (4.2) can be written as in (4.3).

$$\tau = \frac{C}{g_{m3}} \tag{4.3}$$

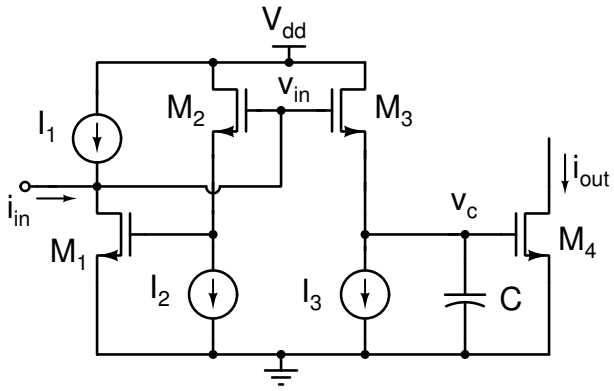


Figure 4.1: Basic log domain filter.

The cutoff frequency of the basic log domain filter can be written as

$$f_c = \frac{1}{2\pi\tau} = \frac{g_{m3}}{2\pi C} \tag{4.4}$$

(4.4) is modified to (4.5) if the body effect of the transistor M_3 is considered.

$$f_c = \frac{g_{m3} + g_{mb3}}{2\pi C} \tag{4.5}$$

Referring to Figure 4.1 and (4.3), the time constant depends on $1/g_{m3}$ (resistance of M_3 looking into its source terminal) and capacitor (C). In UMC 65 nm technology, $g_{m3} + g_{mb3}$ is found to be 39.3 nS for I_3 =1 nA. To design a basic log domain LPF with a cutoff frequency of 100 Hz, the required C calculated from (4.5) is 62 pF, which occupies an area of 0.04 mm^2. Without employing large capacitors, the time constant of the basic log domain filter can be increased by introducing a large active resistor in the charging path of the capacitor.

4.1 Proposed log domain filter

The proposed log domain filter is shown in Figure 4.2a. A large resistance is obtained through a transistor, M_5 added in the charging path of C. As M_5 is connected between source of M_3 and gate of M_4, a very small DC current (of the order of fA) flows through it. As a result, drain and source voltages of M_5 are almost equal. Hence, M_5 operates in sub-threshold triode region and offers very high resistance. Also, it does not disturb the trans-linear loop formed by the transistors, $M_1 - M_4$ and all these transistors are

operating in sub-threshold saturation region. Current mirror shown in Figure 4.2b mirrors the bias current, I_o to the transistors, $M_7 - M_9$. Hence, all the DC currents flowing through the transistors, $M_1 - M_4$ ($I_1 - I_4$) are equal to I_o. The sizes of all the transistors are given in Table 4.1.

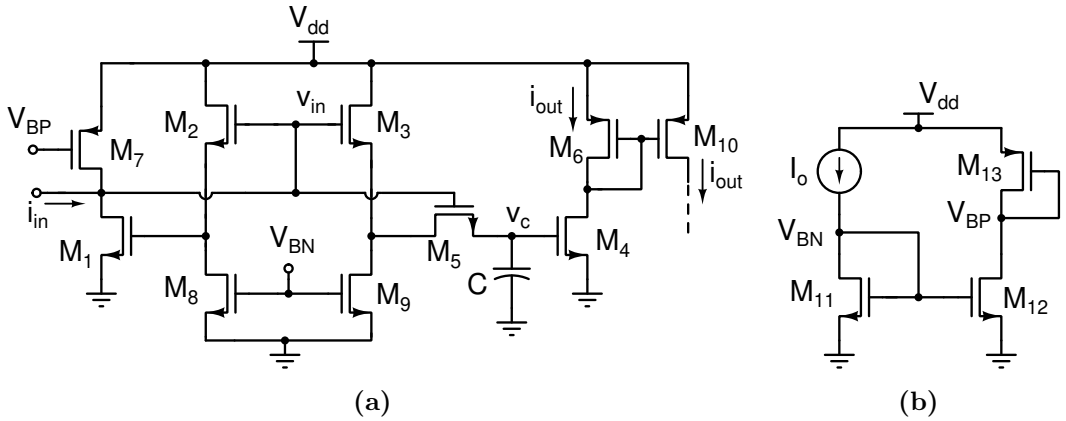


Figure 4.2: (a) Proposed log domain filter, (b) Current mirror to bias the filter.

Table 4.1: Sizes of the transistors in Figure 4.2.

Transistors	$\boldsymbol{W(\mu m)}$ $\boldsymbol{L = 3\mu m}$ for all transistors
M_1, M_4	1
M_2, M_3	60
M_8, M_9, M_{11}, M_{12}	2
M_6, M_7, M_{13}	2
M_5	2.5

The transfer function of the proposed circuit is derived as follows. In sub-threshold saturation region, the drain current equation of an NMOS transistor is given by (4.6) (refer A.2).

$$I_D = I_{D0}(\frac{W}{L})e^{\frac{V_{GS}-V_{th}}{\eta V_T}} \tag{4.6}$$

By assuming $K = I_{D0}(\frac{W}{L})e^{\frac{-V_{th}}{\eta V_T}}$, (4.6) can be written as

$$I_D = Ke^{\frac{V_{GS}}{\eta V_T}} \tag{4.7}$$

From (4.7), V_{GS} can be expressed as

$$V_{GS} = \eta V_T \ln\left(\frac{I_D}{K}\right) \tag{4.8}$$

By using (4.7), the sum of DC and signal currents in M_3 can be written as

$$I_3 + i_c = K_3 e^{\frac{V_{GS1}+V_{GS2}+v_{in}-i_c R_{o5}-v_c-V_{GS4}}{\eta V_T}} = K_3 . e^{\frac{V_{GS1}+v_{in}}{\eta V_T}} . e^{\frac{V_{GS2}}{\eta V_T}} . e^{\frac{-i_c R_{o5}}{\eta V_T}} . e^{\frac{-v_c-V_{GS4}}{\eta V_T}} \tag{4.9}$$

where R_{o5} is the resistance offered by M_5, which is operating in sub-threshold triode region. Exponential terms in the right hand side of (4.9) can be replaced by their respective currents and K values using (4.7).

$$I_3 + i_c = K_3 . \frac{I_1 + i_{in}}{K_1} . \frac{I_2}{K_2} . e^{\frac{-i_c R_{o5}}{\eta V_T}} . \frac{K_4}{i_{out} + I_4} \tag{4.10}$$

Threshold voltages of $M_1 - M_4$ are assumed to be equal. By referring to Table 4.1, we can write $K_3 K_4 = K_1 K_2$. The value of $\frac{i_c R_{o5}}{\eta V_T}$ found from simulations is approximately 0.25 (peak value of $i_c R_{o5} = 7.5$ mV and $\eta V_T = 30$ mV for $\eta = 1.2$). Hence, $e^{\frac{i_c R_{o5}}{\eta V_T}}$ can be approximated to $1 + \frac{i_c R_{o5}}{\eta V_T}$ and (4.10) is simplified to (4.11).

$$(I_3 + i_c)(1 + \frac{i_c R_{o5}}{\eta V_T}) = \frac{(I_1 + i_{in}).I_2}{i_{out} + I_4} \tag{4.11}$$

$$\Rightarrow I_3 + i_c + I_3 . \frac{i_c R_{o5}}{\eta V_T} + \frac{i_c^2 R_{o5}}{\eta V_T} = \frac{(I_1 + i_{in}).I_2}{i_{out} + I_4} \tag{4.12}$$

As $i_c R_{o5} < \eta V_T$, $\frac{i_c^2 R_{o5}}{\eta V_T}$ can be neglected.

$$I_3 + i_c + I_3 . \frac{i_c R_{o5}}{\eta V_T} = \frac{(I_1 + i_{in}).I_2}{i_{out} + I_4} \tag{4.13}$$

By using (4.8), gate voltage of M_4 is written as

$$v_c + V_{GS4} = \eta V_T \ln\left(\frac{i_{out} + I_4}{K_4}\right) \tag{4.14}$$

$$\Rightarrow \frac{dv_c}{dt} = \frac{\eta V_T}{i_{out} + I_4} \frac{di_{out}}{dt} \tag{4.15}$$

The signal current flowing through the capacitor can be written as

$$i_c = C\frac{dv_c}{dt} = \frac{C\eta V_T}{i_{out} + I_4}\frac{di_{out}}{dt} \tag{4.16}$$

By substituting (4.16) in (4.13) and simplifying, we get

$$I_3 i_{out} + I_3 I_4 + C\eta V_T . \frac{di_{out}}{dt} + CR_{o5} I_3 . \frac{di_{out}}{dt} . = I_1 I_2 + i_{in} I_2 \tag{4.17}$$

As the transistors $M_1 - M_4$ form translinear loop, $I_1 I_2 = I_3 I_4$. By applying Laplace transform, we get

$$I_{out}(s)\Big[1 + sC\big(\frac{\eta V_T}{I_3} + R_{o5}\big)\Big] = \frac{I_2}{I_3} . I_{in}(s) \tag{4.18}$$

$$\Rightarrow H_1(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{I_2/I_3}{1 + sC\big(\frac{\eta V_T}{I_3} + R_{o5}\big)} \tag{4.19}$$

Comparing (4.1) and (4.19), we can say that the proposed circuit is still a log domain filter and externally linear. The time constant now is increased as given in (4.20).

$$\tau_1 = \big(R_{o5} + \frac{\eta V_T}{I_3}\big)C = [R_{o5} + 1/g_{m3}]C \tag{4.20}$$

The cutoff frequency (by including the body effect of M_3) can be written as

$$f_{c1} = \frac{1}{2\pi[R_{o5} + 1/(g_{m3} + g_{mb3})]C} \tag{4.21}$$

As M_5 is operating in sub-threshold triode region, we can write $R_{o5} \gg 1/(g_{m3} + g_{mb3})$, which is confirmed by the results given later in this chapter (Table 4.2). Hence, the pole frequency of the proposed filter depends mainly on R_{o5} for a given capacitor value.

The expression for R_{o5} can be derived as follows. I_{D5} can be written as in (4.22) (refer A.1).

$$I_{D5} = I_{D0}(\frac{W}{L})_5 e^{\frac{V_{GS5} - V_{th5}}{\eta V_T}}(1 - e^{\frac{-V_{DS5}}{V_T}}) \tag{4.22}$$

By differentiating I_{D5} with respect to V_{DS5},

$$\frac{dI_{D5}}{dV_{DS5}} = \frac{I_{D0}(\frac{W}{L})_5}{V_T} e^{\frac{V_{GS5} - Vth5}{\eta V_T}} e^{\frac{-V_{DS5}}{V_T}} \tag{4.23}$$

As $V_{DS5} \approx 0$, $e^{\frac{-V_{DS5}}{V_T}} \approx 1$. Hence, R_{o5} can be written as

$$R_{o5} = \frac{1}{\frac{dI_{D5}}{dV_{DS5}}} = \frac{V_T}{I_{D0}(\frac{W}{L})_5 e^{\frac{V_{GS5}-V_{th5}}{\eta V_T}}} \tag{4.24}$$

This equation implies that R_{o5} is a voltage controlled resistor, which depends on V_{GS5}. V_{GS5} in turn depends on I_3 chosen. As $V_{GS5} \approx V_{GS3}$, (4.24) can be further simplified to (4.25) by substituting V_{GS3} (from (4.7)) in place of V_{GS5} and expressing in terms of I_3.

$$R_{o5} = \frac{aV_T(W/L)_3}{I_3(W/L)_5} \tag{4.25}$$

where $a = e^{\frac{V_{th5}-V_{th3}}{\eta V_T}}$. Hence, linear tuning of R_{o5} is possible by varying I_3 $(= I_o)$.

4.1.1 Noise analysis

Log domain filters are internally nonlinear and externally linear. Hence, noise generated within the log domain filter cannot be transformed to the output by using small signal analysis. There exists an intermodulation between signal and noise due to internal non-linearities (Mulder *et al.* 1997, Enz *et al.* 1999). A method to calculate the noise of log domain filters by using transfer functions is described in (Ng and Sewell 2002) and the same is exploited in this proposed work.

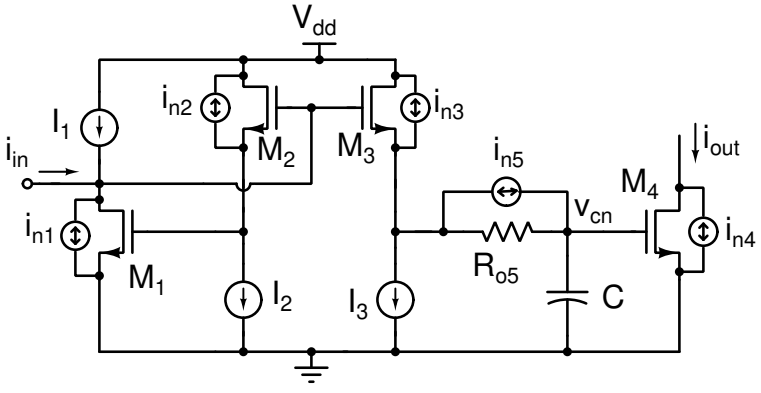


Figure 4.3: Noise equivalent of the proposed log domain filter.

Noise equivalent of the proposed log domain filter is shown in Figure 4.3. Transistor M_5 is represented by its equivalent resistance, R_{o5}. Noise current associated with each transistor is indicated in the circuit. To make the analysis simpler, noise currents of

the current mirror transistors are neglected. Output current noise can be calculated by calculating the transfer functions from each individual noise source to the output. The transfer functions from i_{n1}, i_{n2} and i_{n5} to the output are represented by $H_{n1}(s)$, $H_{n2}(s)$ and $H_{n5}(s)$ respectively. All the bias currents I_1, I_2, I_3 and I_4 (DC current in M_4) are equal to I_o. The thermal and flicker $(1/f)$ noise power spectral densities (PSDs) of a transistor are given by (4.26) (Sarpeshkar *et al.* 1993) and (4.27) (Razavi 2002) respectively.

$$i^2_{n,\ thermal} = 2qI_o \tag{4.26}$$

$$i^2_{n,1/f} = \frac{K_f}{C_{ox}WL}.\frac{1}{f}.\left(\frac{I_o}{\eta V_T}\right)^2 \tag{4.27}$$

where, K_f is the flicker noise parameter and all other terms have their usual meanings. Device sizes (W and L) are taken sufficiently large to reduce the flicker noise. Hence, in this design, the expressions for thermal noise are derived. By using (4.19), $H_{n1}(s)$ and $H_{n2}(s)$ can be written as

$$H_{n1}(s) = \frac{i_{no1}}{i_{n1}} = \frac{I_2}{I_3}.\frac{1}{1+s\tau_1} \tag{4.28}$$

$$H_{n2}(s) = \frac{i_{no2}}{i_{n2}} = \frac{I_1}{I_3}.\frac{1}{1+s\tau_1} \tag{4.29}$$

where, i_{noj} is the output noise current due to transistor M_j. As M_3 is a cascode device to M_5, the noise current of M_3 can be neglected. The expression for H_{n5} is derived as follows. Gate voltage of M_4 is given by

$$v_{cn} = \frac{R_{o5}}{1+s\tau_1}.i_{n5} \tag{4.30}$$

By using (4.7), total output current in M_4 is given by

$$I_4 + i_{no5} = K_4 e^{\frac{V_{GS4}+v_{cn}}{\eta V_T}} = I_{D0} e^{\frac{V_{GS4}}{\eta V_T}}.e^{\frac{v_{cn}}{\eta V_T}} \tag{4.31}$$

In (4.31), $K_4 e^{\frac{V_{GS4}}{\eta V_T}}$ can be replaced by I_4. If we assume $v_{cn} \ll \eta V_T$, (4.31) is simplified

to (4.32).

$$I_4 + i_{no5} = I_4(1 + \frac{v_{cn}}{\eta V_T}) \tag{4.32}$$

$$\Rightarrow i_{no5} = I_4\frac{v_{cn}}{\eta V_T} = \frac{I_4}{\eta V_T}.\frac{R_{o5}}{1+s\tau_1}.i_{n5} \tag{4.33}$$

$$\Rightarrow H_{n5} = \frac{i_{no5}}{i_{n5}} = \frac{I_4 R_{o5}}{\eta V_T}.\frac{1}{1+s\tau_1} \tag{4.34}$$

By using (4.28), the PSD of the noise at the output due to i_{n1} can be written as

$$i_{no1}^2 = i_{n1}^2.\frac{I_2^2}{I_3^2}.\frac{1}{\mid 1+s\tau_1 \mid^2} = 2qI_o.\frac{I_o^2}{I_o^2}.\frac{1}{\mid 1+s\tau_1 \mid^2} = \frac{2qI_o}{\mid 1+s\tau_1 \mid^2} \tag{4.35}$$

Hence, the integrated output noise power due to i_{n1} can be written as

$$P_{no1} = 2qI_o.\int_0^\infty \frac{df}{\mid 1+s\tau_1 \mid^2} = \frac{qI_o}{2\tau_1} \tag{4.36}$$

From (4.36), it can be seen that output noise power can be reduced by reducing the bias current, I_o. However, reducing I_o will reduce the input signal swing. By using (4.29), the PSD of the noise at the output due to i_{n2} can be written as

$$i_{no2}^2 = \frac{I_1^2}{I_3^2}.i_{n2}^2.\frac{1}{\mid 1+s\tau_1 \mid^2} \tag{4.37}$$

If an input sinusoidal signal, $I_o sin(\omega t)$ is applied to the filter, then its RMS value $(I_o/\sqrt{2})$ is a large signal and should be added to the DC current (I_o). Hence, (4.37) is modified to (4.38).

$$i_{no2}^2 = \frac{I_o^2 + i_{in,rms}^2}{I_o^2}.i_{n2}^2.\frac{1}{\mid 1+s\tau_1 \mid^2} = \frac{I_o^2 + \frac{I_o^2}{2}}{I_o^2}.2qI_o.\frac{1}{\mid 1+s\tau_1 \mid^2} = \frac{3qI_o}{\mid 1+s\tau_1 \mid^2} \tag{4.38}$$

Hence, the integrated output noise power due to i_{n2} can be written as

$$P_{no2} = \frac{3qI_o}{4\tau_1} \tag{4.39}$$

By using (4.34), the PSD of the noise at the output due to i_{n5} can be written as in

(4.40). Here, RMS value of the output signal current is added to the DC current.

$$i_{no5}^2 = i_{n5}^2 . \frac{I_o^2 + \frac{I_o^2}{2}}{\eta^2 V_T^2} . \frac{R_{o5}^2}{\mid 1 + s\tau_1 \mid^2} = \frac{3}{2} i_{n5}^2 . \frac{I_o^2 R_{o5}^2}{\eta^2 V_T^2} . \frac{1}{\mid 1 + s\tau_1 \mid^2} \tag{4.40}$$

The thermal noise PSD of a transistor operating in sub-threshold triode region is $4qI_o$ (Sarpeshkar *et al.* 1993). From Table 4.2, it can be seen that $R_{o5}I_o \approx 1$. Hence, (4.40) is simplified to (4.41).

$$i_{no5}^2 = \frac{3}{2} . 4qI_o . \frac{1}{\eta^2 V_T^2} . \frac{1}{\mid 1 + s\tau_1 \mid^2} = \frac{6qI_o}{\eta^2 V_T^2} . \frac{1}{\mid 1 + s\tau_1 \mid^2} \tag{4.41}$$

Hence, the integrated output noise power due to i_{n5} can be written as

$$P_{no5} = \frac{6qI_o}{\eta^2 V_T^2} . \frac{1}{4\tau_1} = \frac{3qI_o}{2\eta^2 V_T^2} . \frac{1}{\tau_1} \tag{4.42}$$

As $\eta V_T < 1$, $P_{no5} > P_{no2}$ and $P_{no5} > P_{no1}$. Hence, the noise contributed by M_5 is more than the noise contributed by all other transistors in the circuit. The noise current i_{n4} is directly contributed to the output. Hence, P_{no4} is given by

$$P_{no4} = \frac{2qI_o}{\tau_1} \tag{4.43}$$

Therefore, the total integrated output thermal noise power is given by

$$P_{no} = P_{no1} + P_{no2} + P_{no4} + P_{no5} \tag{4.44}$$

4.1.2 Second order LPF

By cascading two identical first order sections of the proposed log domain filter, a 2^{nd} order LPF is obtained as shown in Figure 4.4. For this 2^{nd} order LPF, -3 dB frequency (f_{-3dB}) is written as in (4.45) (Sawigun and Serdijn 2016).

$$f_{-3dB} = f_{c1}\sqrt{\sqrt{2} - 1} \tag{4.45}$$

For f_{-3dB} of 100 Hz, the required f_{c1} is 155.4 Hz. C_1 and C_2 are calculated to be 0.92 pF.

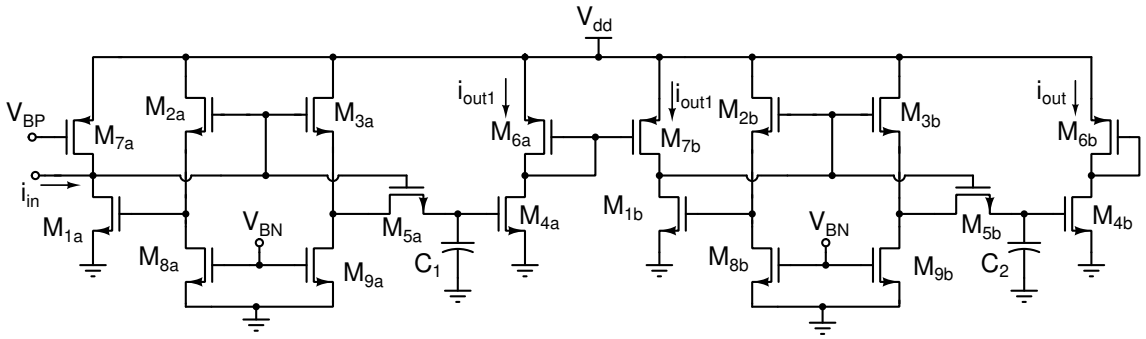


Figure 4.4: 2^{nd} order LPF.

4.1.3 Post-layout Simulation Results & Discussion

The proposed log domain filter (Figure 4.2a) and 2^{nd} order LPF (Figure 4.4) are designed and laid out using UMC 65 nm CMOS technology. The frequency response of the proposed log domain first order filter for $I_o = 1$ nA and $C = 0.92$ pF is shown in Figure 4.5. DC gain and cutoff frequency are -0.4 dB and 155.4 Hz respectively.

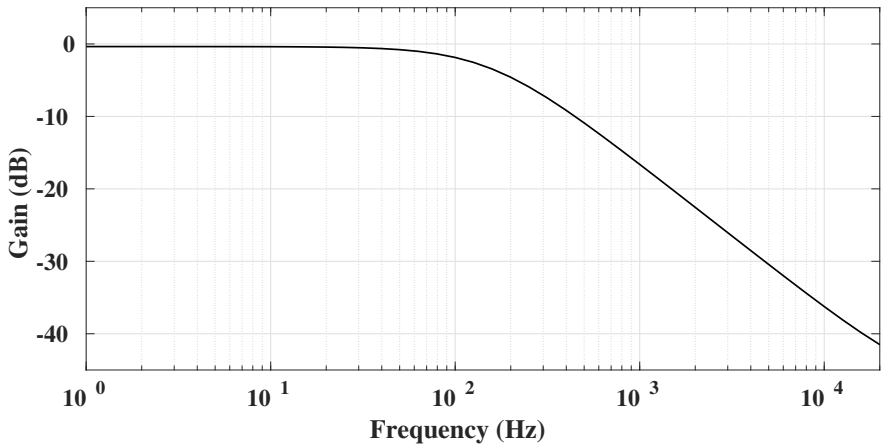


Figure 4.5: Frequency response of the proposed log domain first order filter.

From Table 4.2 it is evident that $R_{o5} \gg 1/(g_{m3} + g_{mb3})$. This confirms that the cutoff frequency of the proposed filter (Figure 4.2a) depends mainly on R_{o5} (Eq. (4.21)) whereas the cutoff frequency of the basic log domain filter (Figure 4.1) depends on $g_{m3} + g_{mb3}$ (Eq. (4.4)). For $I_o = 1$ nA, to get a cutoff frequency of 155.4 Hz, basic log domain filter requires a capacitance of 40 pF whereas the proposed filter requires only 0.92 pF. In other words, for a given bias current, area of the circuit is reduced by 43.5 times. Hence, by using the proposed technique, filters with low cutoff frequency

can be realized without using large capacitors.

Table 4.2: R_{o5} and $g_{m3} + g_{mb3}$ values for the proposed log domain filter.

I_o (nA)	R_{o5} (MΩ)	$g_{m3} + g_{mb3}$ (nS)	$1/(g_{m3} + g_{mb3})$ (MΩ)	$R_{o5} + 1/(g_{m3} + g_{mb3})$ (MΩ)
0.1	10870	3.98	250	11120
1	1085	39.3	25	1110
5	213.5	193.2	5.17	218.7

From Table 4.2, we can see that R_{o5} decreases almost linearly as I_o increases. Therefore, the cutoff frequency of the proposed log domain filter can be linearly tuned with I_o.

Figure 4.6 shows the layout of 2^{nd} order LPF. It takes an area of 0.005 mm^2 (78 μm×67 μm). MIM capacitors are used for C_1 and C_2. For I_o = 1 nA, DC gain and f_{-3dB} of the 2^{nd} order LPF are -0.8 dB and 100 Hz respectively as shown in Figure 4.7.

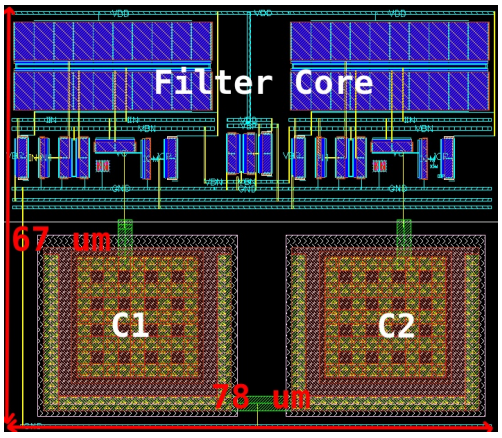


Figure 4.6: Layout of 2^{nd} order LPF.

To analyze the linearity of the filter, a sinusoidal current signal of frequency 20 Hz is fed into the filter. THD is found to be ≤ 2 % for an input current of 2 nA peak-peak. Figure 4.8a shows the harmonics in the output current for the same input. Second order harmonic component is more dominant and second order harmonic distortion (HD_2) of -35 dB is observed. The output noise current of the filter is shown in Figure 4.8b. The flicker noise is more dominant upto a frequency of about 5 Hz and thermal noise dominates after 5 Hz. IRN integrated over the frequency range, 1-100 Hz is

observed as 2.4 pArms. From these values, the DR of the filter is calculated as 49.4 dB.

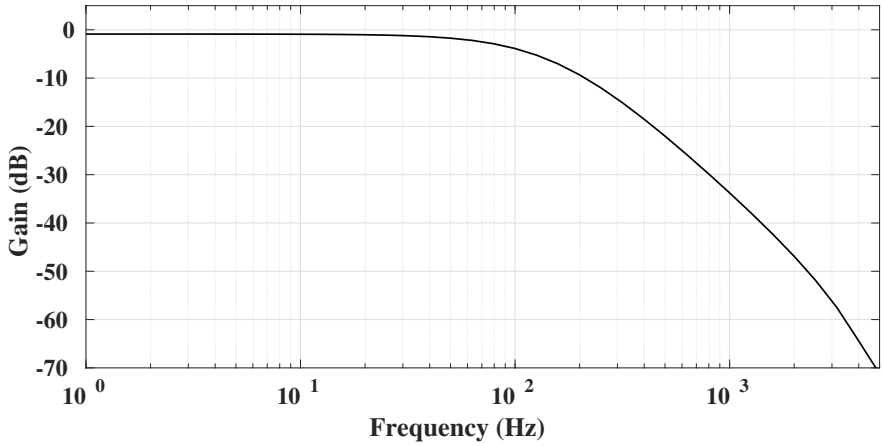


Figure 4.7: Frequency response of the 2^{nd} order LPF.

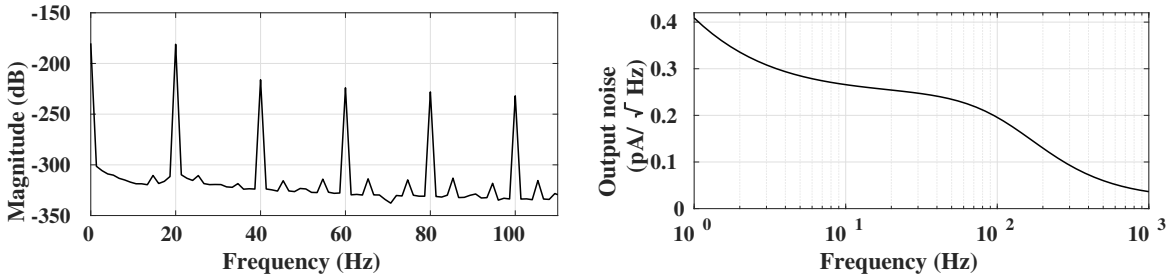


Figure 4.8: 2^{nd} order LPF (a) Harmonic components, (b) Output noise.

Transient response shown in Figure 4.9 portrays the input-output linearity. Output peak-to-peak current is slightly less than 2 nA as the filter gain is -0.8 dB.

FoM1 of the proposed filter is as less as 0.68×10^{-13} J. f_{-3dB} of the filter can be linearly tuned from 10 to 500 Hz by adjusting the bias current, I_o from 0.1 nA to 5 nA as shown in Figure 4.10.

Table 4.3 shows the comparison of results. A 2^{nd} order LPF by cascading two identical basic log domain filters (Figure 4.1) given in (Frey 2000) is designed in UMC 65 nm CMOS technology and its results are included in Table 4.3. When compared to the basic log domain filter (Frey 2000), linearity and noise performance of the proposed 2^{nd} order LPF are slightly degraded due to the addition of M_{5a} and M_{5b}.

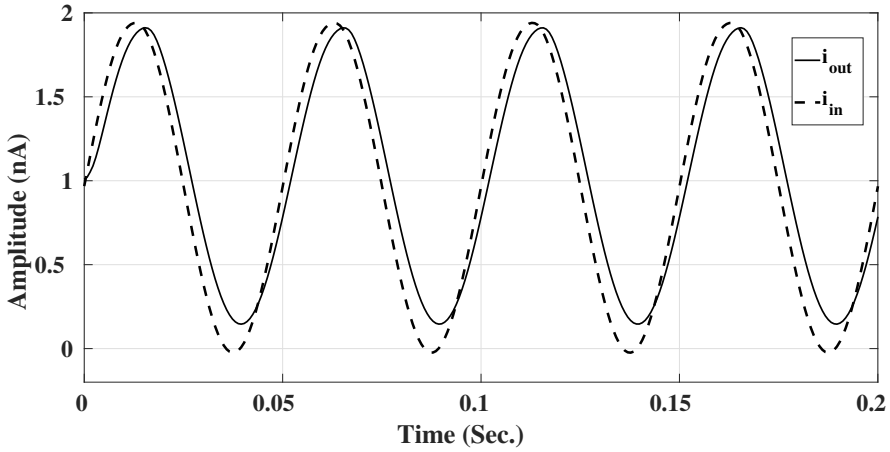


Figure 4.9: Transient response.

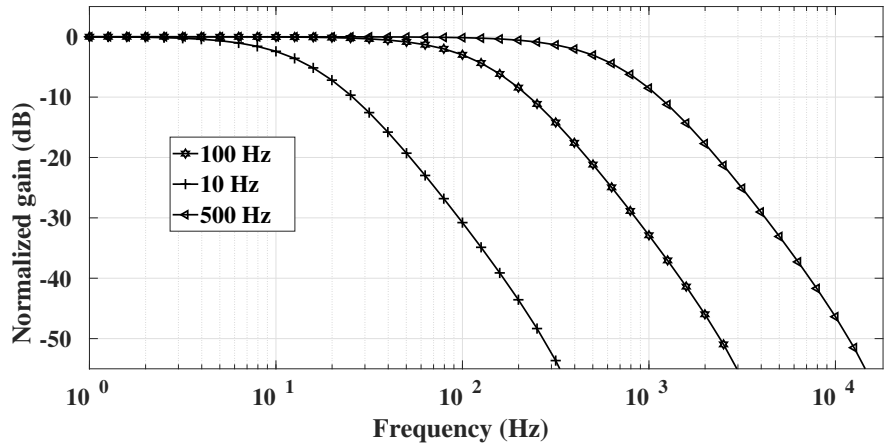


Figure 4.10: f_{-3dB} tuning of the 2^{nd} order LPF. The results are in the format [I_o, f_{-3dB}]. [0.1 nA, 10 Hz], [1 nA, 100 Hz] and [5 nA, 500 Hz].

However, capacitance is reduced by a factor of 43.5 times, hence, the proposed circuit is area efficient.

The proposed filter uses the lowest capacitance/pole among all the designs listed. Hence, the area of the proposed design reduces significantly without compromising much on linearity. FoM1 of the filter is better than the designs given in (Khanday and Shah 2013, Tsirimokou and Psychalinos 2014, Kafe and Psychalinos 2014, Kafe *et al.* 2014).

Table 4.3: 2^{nd} order log domain filter - results summary and performance comparison.

Parameter	La Croz-Blas *et al.* 2005	Khanday and Shah 2013	Tsirimokou and Psychalinos 2014	Kafe and Psychalinos 2014	Kafe *et al.* 2014	Frey 2000	**This Work**
Technology (nm)	800	350	180	180	180	65	**65**
V_{dd} (V)	1.2	0.75	0.5	0.5	0.5	0.5	**0.5**
Filter order	1	2	1	2	4	2	**2**
Cutoff frequency (Hz)	25 - 35 k	13	9.6	6.3	51.3	100	**100**
Power (nW)	4700	19.2	3.05	16.19	35	4	**4**
Input peak-to-peak current for 2 % THD (nA)	–	0.17†	5.82	–	1.59	2.2	**2**
IRN_{rms} (pA)	260	0.067	1.2	–	0.94	1.15	**2.4**
DR (dB)	75	59.2	64.7	55.24	55.5	56.6	**49.4**
Capacitance / pole (pF)	300	75.3	47.1	95	100	40	**0.92**
Active area (mm^2)	0.1	–	0.024	–	–	–	**0.005**
FoM (J) ($\times 10^{-13}$)	–	8.1	1.8	22.2	2.9	0.3	**0.68**

† Input peak-to-peak current is calculated for 1 % THD.

4.1.3.1 Deviation in f_{-3dB} due to PVT variations

The frequency response of the filter across process corners is shown in Figure 4.11. Gain is normalized to 0 dB to compare the results. f_{-3dB} is 98 Hz and 102.5 Hz in 'ss' and 'ff' corners respectively. Worst case deviations occur in these two corners. Hence, the deviation in f_{-3dB} is $\leq$ 2.5 % across all the process corners. As shown in Figure 4.12, f_{-3dB} deviation is only $\pm$1 % for a $\pm$10 % variation in V_{dd}.

The frequency response of the filter for different temperatures is shown in Figure 4.13. f_{-3dB} deviation is $\leq$ 4 % in the temperature range of 0-70°C. The small variation in f_{-3dB} is due to the small variation in R_{o5} with temperature. By adjusting the bias current, f_{-3dB} can be set back to 100 Hz. Figure 4.14 shows the Monte Carlo

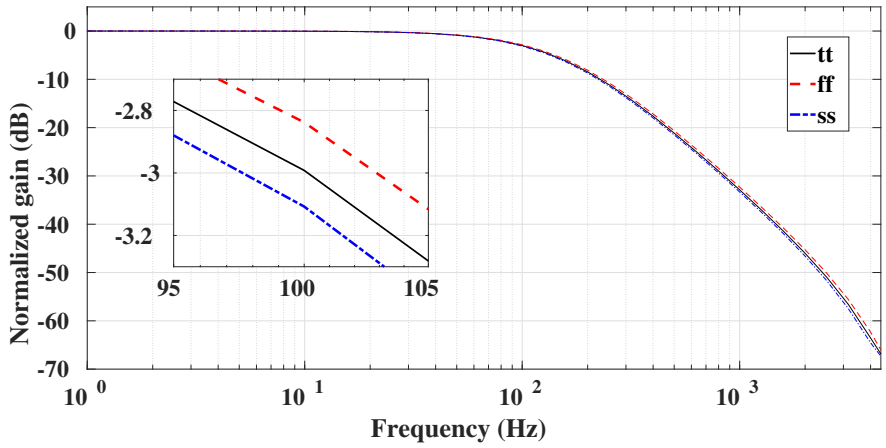


Figure 4.11: Frequency response of the 2^{nd} order LPF across process corners.

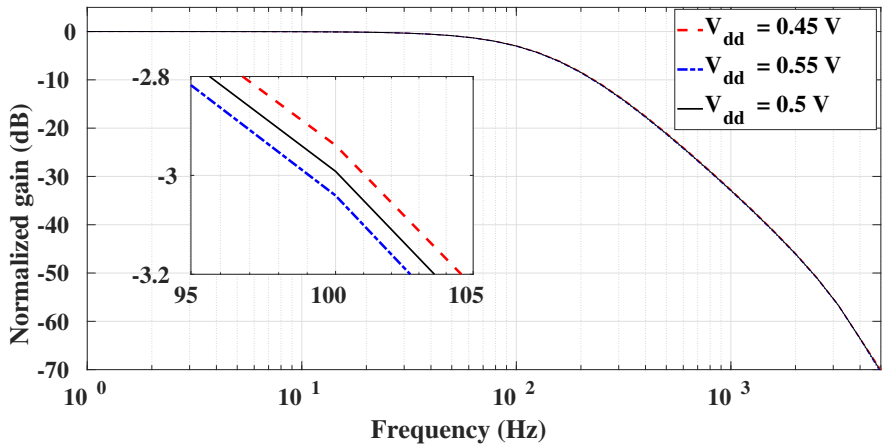


Figure 4.12: Frequency response of the 2^{nd} order LPF across V_{dd} variations.

simulations of f_{-3dB} for 100 runs. The observed mean and standard deviation are 100.2 Hz and 4.8 Hz respectively.

All these results show that the proposed design is an area efficient log domain filter circuit with the lowest area and capacitance/pole without compromising much on power and linearity.

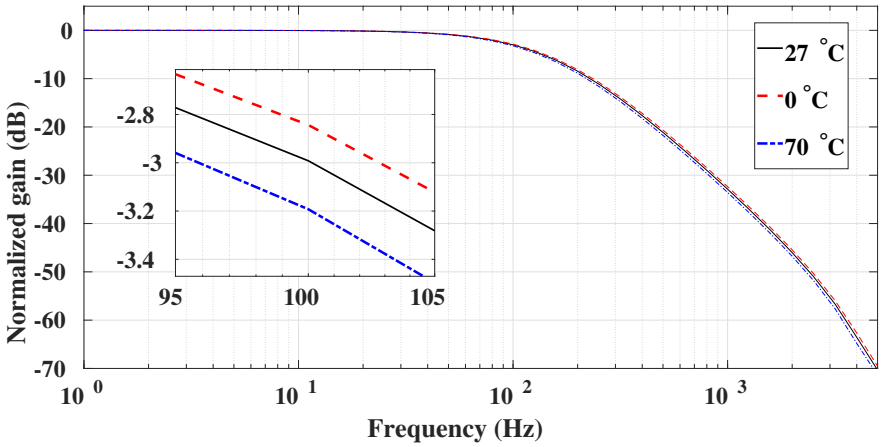


Figure 4.13: Frequency response of the 2^{nd} order LPF across temperature variations.

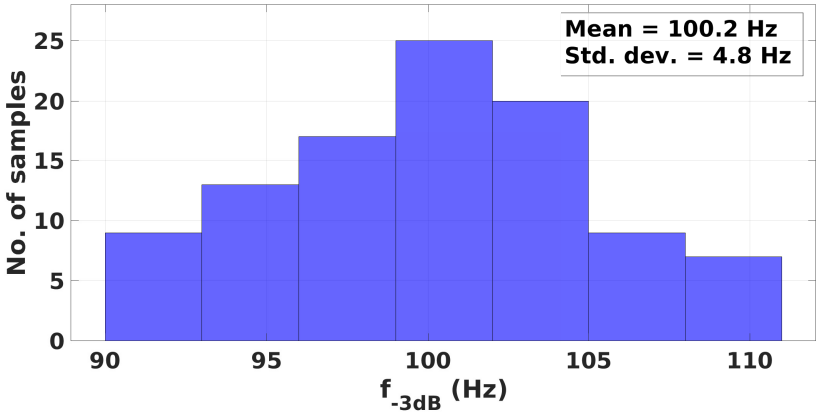


Figure 4.14: Monte Carlo simulations of f_{-3dB} for 100 runs.

Chapter 5

CURRENT REFERENCE CIRCUITS

Current reference circuits are necessary building blocks used to set the operating point of analog circuits. As the circuit performance varies depending upon the operating point, the current reference should be stable enough to be independent of variations in process and supply voltage. Circuits need either a constant (temperature independent) current or PTAT current depending upon their behavior. In this chapter, the basic beta-multiplier circuit is exploited to get nA-range PTAT current. To overcome the drawbacks in the basic beta-multiplier circuit, a 0.8 V PTAT current reference and a 0.5 V SC PTAT current reference are proposed. Both the PTAT circuits are designed in UMC 65 nm technology.

5.1 Beta-multiplier Circuit

The basic beta-multiplier circuit (Razavi 2002) is shown in Figure 5.1a. If all the transistors are operating in weak-inversion saturation, it gives a PTAT current as explained later in this section.

From Figure 5.1a, V_R (voltage across R) can be written as

$$V_R = V_{GS1} - V_{GS2} \tag{5.1}$$

Using (A.2), gate-source voltages of M_1 and M_2 can be written as in (5.2) and (5.3)

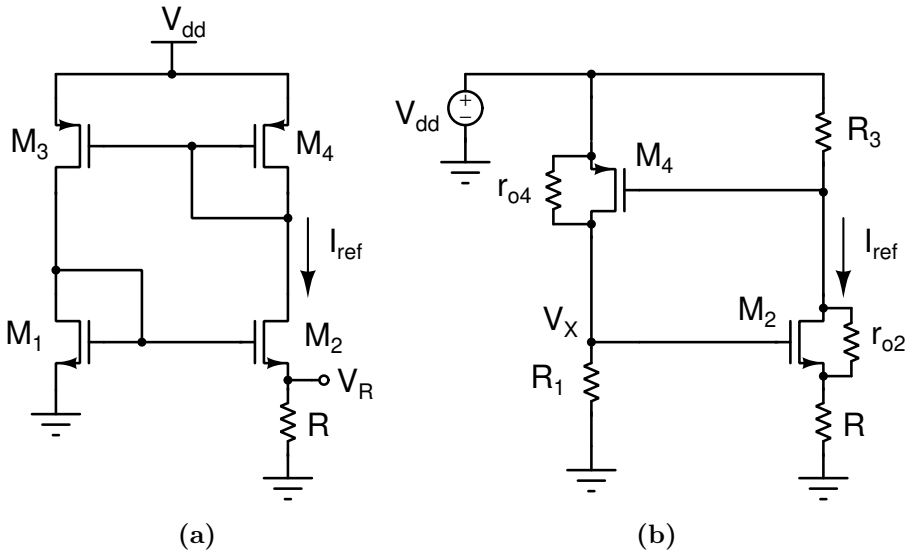


Figure 5.1: Beta-multiplier (a) Schematic, (b) Equivalent circuit.

respectively.

$$V_{GS1} = \eta V_T ln(\frac{I_{D1}}{I_{D0}(\frac{W}{L})_1}) + V_{th1} \tag{5.2}$$

$$V_{GS2} = \eta V_T ln(\frac{I_{D2}}{I_{D0}(\frac{W}{L})_2}) + V_{th2}^{'} \tag{5.3}$$

$V_{th2}^{'}$ can be written as in (5.5) (Ferreira *et al.* 2008) to include the body effect of M_2.

$$V_{th2}^{'} = V_{th2} + (\eta - 1)V_{SB} = V_{th2} + (\eta - 1)(V_R) \tag{5.4}$$

$$\Rightarrow V_{th2}^{'} = V_{th2} + (\eta - 1)(I_{ref}R) \tag{5.5}$$

By substituting (5.2) and (5.3) in (5.1) and by assuming $V_{th1} = V_{th2}$, I_{ref} can be derived as

$$I_{ref} = \frac{V_T ln(p)}{R} \tag{5.6}$$

where $p = \frac{(W/L)_2}{(W/L)_1}$. If the resistor, R is assumed to be thermally stable, then I_{ref} is directly proportional to temperature and hence it follows PTAT characteristics.

Main drawback of the basic beta-multiplier circuit is the variation of I_{ref} with V_{dd}. Figure 5.2 shows the variation of I_{ref} with V_{dd} of the beta-multiplier circuit designed using UMC 65 nm technology. Supply voltage sensitivity ($S_{V_{dd}}^{I_{ref}}$) defined in (5.7) (Razavi 2002) can be used to observe the effect of supply voltage variations on

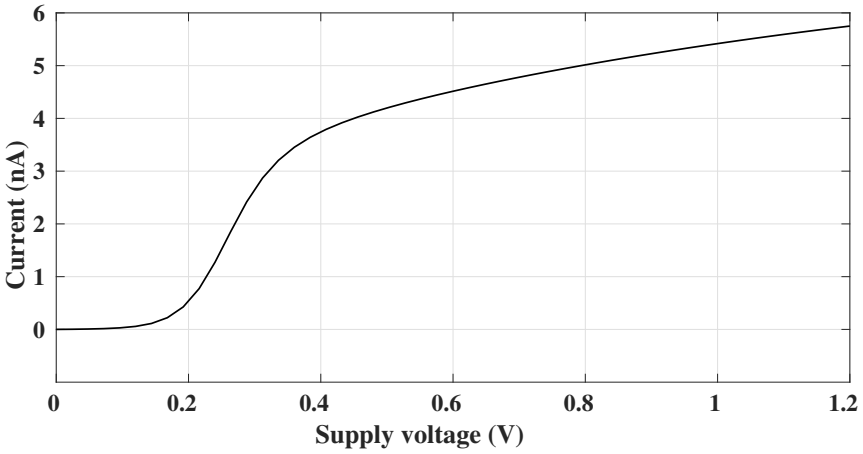


Figure 5.2: I_{ref} versus supply voltage of beta-multiplier circuit.

I_{ref}.

$$S_{V_{dd}}^{I_{ref}} = \frac{\partial I_{ref}}{\partial V_{dd}} \frac{1}{I_{ref}} \tag{5.7}$$

The change in I_{ref} due to change in V_{dd} ($\frac{\partial I_{ref}}{\partial V_{dd}}$) of the beta-multiplier circuit can be calculated from its equivalent circuit as shown in Figure 5.1b. Here, $R_1 = r_{o1} \parallel (1/g_{m1})$, $R_3 = r_{o3} \parallel (1/g_{m3})$ and the small signal gate-source voltage of M_4 is $-I_{ref}R_3$. By applying the KCL at node V_X,

$$\frac{V_{dd} - V_X}{r_{o4}} + I_{ref}R_3 g_{m4} = \frac{V_X}{R_1} \tag{5.8}$$

The equivalent transconductance of M_2 can be denoted by G_{m2}, which is given by (5.9)

$$G_{m2} = \frac{I_{ref}}{V_X} \tag{5.9}$$

From (5.8) and (5.9), $\frac{\partial I_{ref}}{\partial V_{dd}}$ can be written as

$$\frac{\partial I_{ref}}{\partial V_{dd}} = \frac{1}{r_{o4}}\left[\frac{1}{G_{m2}(r_{o4} \parallel R_1)} - g_{m4}R_3\right]^{-1} \tag{5.10}$$

G_{m2} can be written as

$$G_{m2} = \frac{g_{m2}r_{o2}}{R + r_{o2} + g_{m2}Rr_{o2}} \tag{5.11}$$

As $g_{m2}r_{o2} \gg 1$, (5.11) can be simplified to (5.12)

$$G_{m2} \approx \frac{g_{m2}}{1 + g_{m2}R} \tag{5.12}$$

By substituting (5.12) in (5.10), we get

$$\frac{\partial I_{ref}}{\partial V_{dd}} \approx \frac{1}{r_{o4}}[\frac{1 + g_{m2}R}{\frac{g_{m2}}{g_{m1}}} - \frac{g_{m4}}{g_{m3}}]^{-1} \tag{5.13}$$

All transistors in Figure 5.1a carry same current. By assuming that both NMOS and PMOS transistors have same η values, we can write $g_{m1} \approx g_{m2}$ and $g_{m3} \approx g_{m4}$. Hence, (5.13) can be simplified to (5.14).

$$\frac{\partial I_{ref}}{\partial V_{dd}} \approx \frac{1}{g_{m2}r_{o4}R} \tag{5.14}$$

As per (5.14), $\frac{\partial I_{ref}}{\partial V_{dd}}$ can be reduced by increasing r_{o4}. Cascode transistors can be used to improve the output resistance. However, cascode structure demand higher supply voltage. In such cases, composite transistors (Ferreira *et al.* 2008) can be used to increase the output resistance without requiring higher supply voltage .

5.2 0.8 V PTAT Current Reference

The proposed PTAT current reference circuit is shown in Figure 5.3. All the transistors ($M_1 - M_4$) in basic beta-multiplier are replaced by composite transistors ($M_{1a}, M_{1b} - M_{4a}, M_{4b}$) to improve supply voltage sensitivity without consuming extra power. The size of the composite transistor, M_{2a}, M_{2b} is 3 times the size of the composite transistor, M_{1a}, M_{1b} and R (off-chip resistor) is taken as 6 MΩ.

Output resistance of the composite transistor, $M_{4a} - M_{4b}$ can be written as

$$r_{o4} = g_{m4b}r_{o4b}r_{o4a} \tag{5.15}$$

By substituting (5.15) in (5.14), the gain from V_{dd} to I_{ref} for the proposed circuit can be written as in (5.16).

$$\frac{\partial I_{ref}}{\partial V_{dd}} \approx \frac{1}{g_{m2a}g_{m4b}r_{o4b}r_{o4a}R} \tag{5.16}$$

From (5.16), it can be seen that the supply voltage sensitivity of the proposed circuit

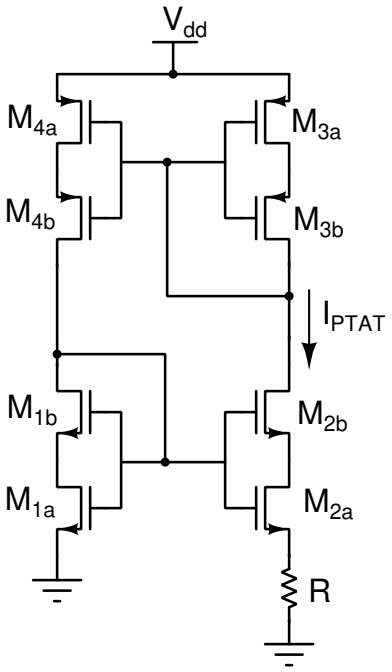


Figure 5.3: Proposed 0.8 V PTAT circuit

is reduced approximately by a factor of $g_m r_o$ (intrinsic gain of the transistor), when compared to the conventional beta-multiplier circuit.

5.2.1 Post-layout Simulation Results

Layout of the proposed circuit is shown in Figure 5.4. It takes an area of 432 μm^2 (24 μm$\times$18 μm). Figure 5.5 plots I_{ref} with respect to temperature. I_{ref} is linearly increas-

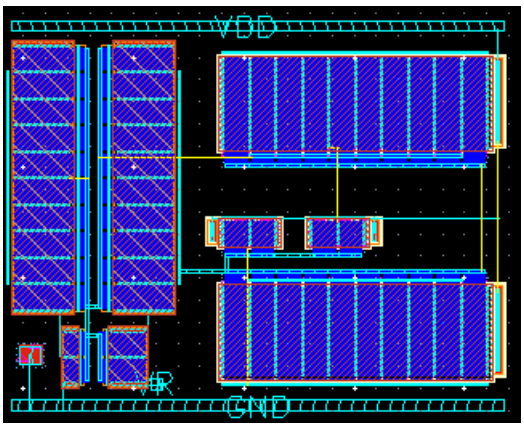


Figure 5.4: Layout of 0.8 V PTAT current reference

ing with temperature in the range of 0 - 80°C. Hence, it follows PTAT characteristics.

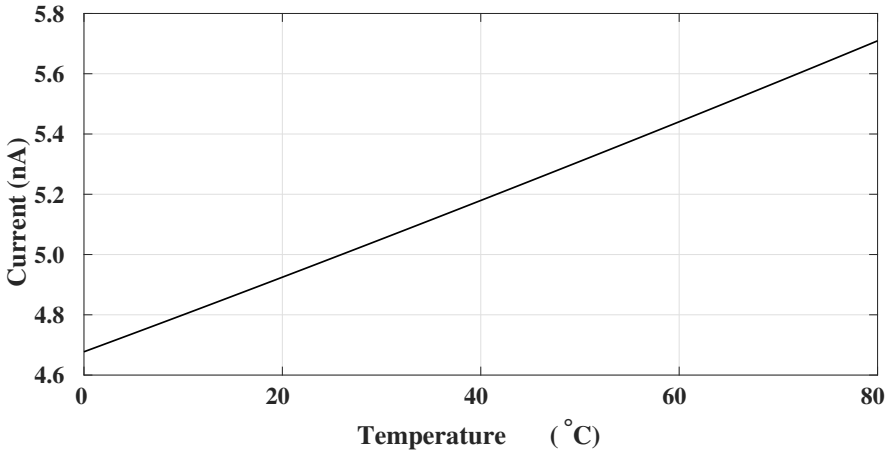


Figure 5.5: I_{ref} versus temperature

Figure 5.6 plots I_{ref} with respect to the supply voltage. It can be observed that I_{ref} of the proposed circuit is almost constant from 0.5 V on wards, whereas I_{ref} of the beta-multiplier circuit (Figure 5.1a) is increasing with the supply voltage (Figure 5.2). According to (5.7), the supply voltage sensitivity of the proposed and beta-multiplier circuits are found to be 2.6 %/V and 41 %/V respectively in the supply voltage range of 0.6 - 1.2 V. The proposed circuit can be operated down to a supply voltage of 0.5 V.

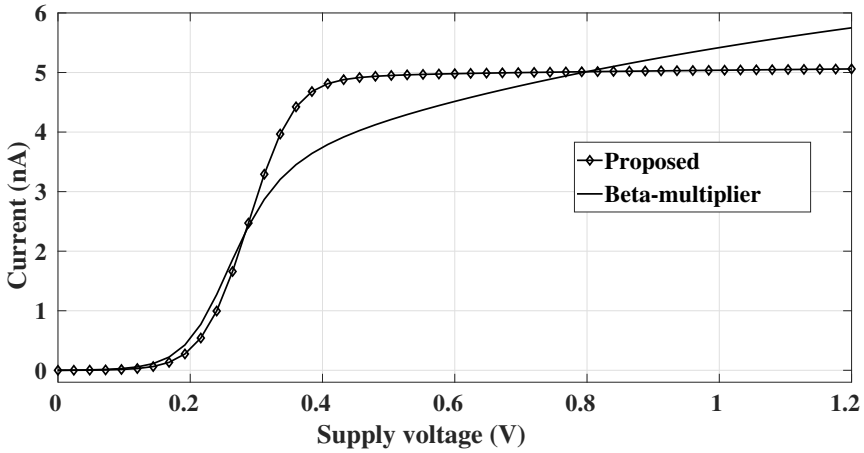


Figure 5.6: I_{ref} versus supply voltage

Table 5.1: Comparison of the proposed PTAT circuit with other similar designs

Parameter	Camacho-Galeano *et al.* 2005	Osaki *et al.* 2013	Jorge and Aita 2016	Re-design of beta-multiplier	**This work**
Technology (μm)	1.5	0.18	0.04	0.065	**0.065**
V_{dd} (V)	1.2	1.2	1	0.8	**0.8**
I_{Ref} (nA)	0.4	6	100	5	**5**
Power (nW)	2	–	350	8	**8**
$S_{V_{dd}}^{I_{ref}}$ (%/V)	6	6.47	2.9	41.2	**2.6**

The proposed circuit consumes a power of 8 nW at room temperature with V_{dd} of 0.8 V. A performance comparison of the proposed circuit with the state-of-the-art PTAT current reference circuits is given in Table 5.1. The proposed PTAT circuit operates with the lowest supply voltage and has the lowest supply voltage sensitivity among the papers listed. This circuit can be used as a biasing circuit in low voltage, low frequency log-domain and $G_m - C$ filter circuits to make the cutoff frequency of the filter independent of temperature.

5.3 0.5 V SC PTAT Current Reference

To design a PTAT current of 1 nA using beta-multiplier circuit shown in Figure 5.1a, a resistor of approximately 10 MΩ is required for p = 1.5. These large resistors occupy huge area on the chip and also are more process dependent. This limits the accuracy of I_{ref}. In systems where a precise clock frequency is available, the resistor, R in Figure 5.1a can be replaced by a SC equivalent to reduce silicon area. The clock can be obtained from digital circuits as they co-exist with analog circuits in a typical SoC.

The proposed switched-capacitor PTAT current reference circuit is shown in Figure 5.7a. The size of M_2 is chosen as 1.5 times the size of M_1 to get p = 1.5. Here, the resistor is replaced by a SC formed by C_1 and transmission gate switches (formed by M_n and M_p). The size of M_p is chosen as 4 times the size of M_n to make the ON resistance of the transmission gate independent of the voltage across it. Two complementary clocks ('clk' and 'clk_b') of same frequency (f_{clk}) are used for the switching operation. When 'clk' is high ('clk_b' is low), C_1 charges and it discharges when 'clk' is low ('clk_b' is high). The average resistance (R_{eq}) of the switched capacitor is given

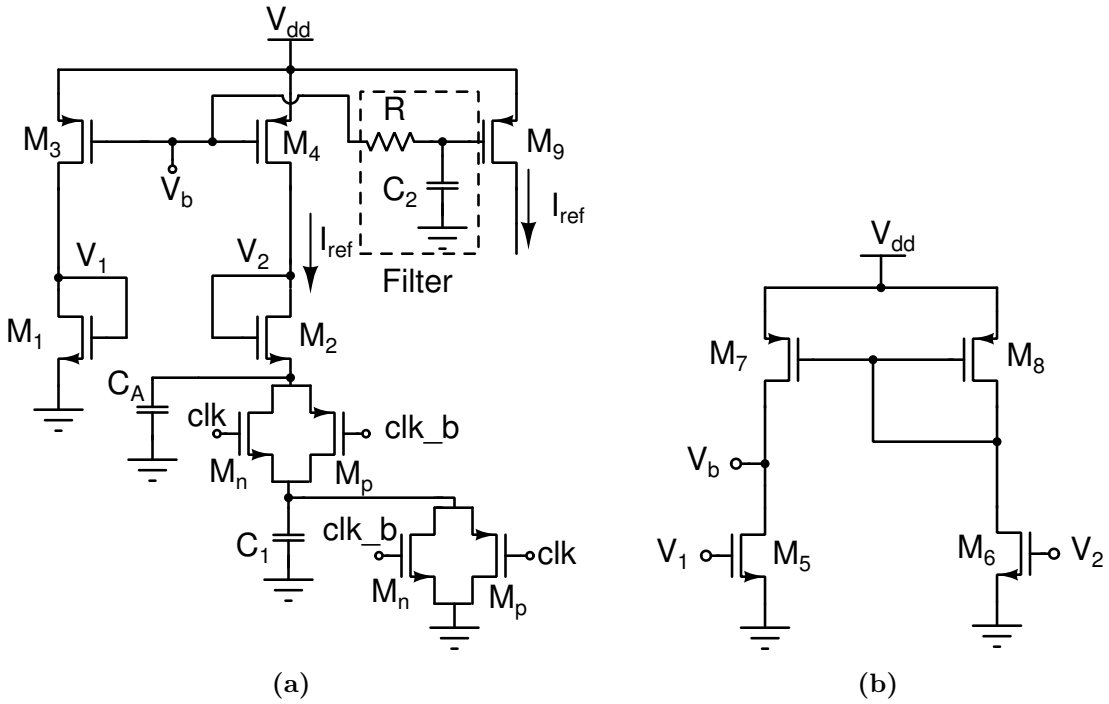


Figure 5.7: (a) Proposed 0.5 V SC PTAT circuit, (b) Error amplifier.

as in (5.17) (Razavi 2002).

$$R_{eq} = \frac{1}{f_{clk} C_1} \tag{5.17}$$

where f_{clk} denotes frequency of the clock used for switching operation. By substituting R_{eq} (5.17) in place of R in (5.6), we get

$$I_{ref} = V_T f_{clk} C_1 ln(p) \tag{5.18}$$

From (5.18) it can be seen that I_{ref} is directly proportional to C_1. For the currents in the range of nAs, the capacitor can be a small value by appropriately choosing f_{clk} and 'p'.

The error amplifier shown in Figure 5.7b makes the drain voltages of both M_1 and M_2 equal and hence currents through M_1 and M_2 are equal. This arrangement will also reduce the dependency of I_{ref} on V_{dd}. The capacitor C_A is used to shunt the high frequency switching noise (ripples) to ground. Additionally, a simple low pass filter formed by R and C_2 is added to remove ripples further in the reference current.

f_{clk} is chosen as 100 kHz. Capacitors, C_1, C_2 and C_A are taken as 0.8 pF, 0.1 pF

and 10 pF respectively. The resistor, R is taken as 1 kΩ.

5.3.1 Simulation Results

Periodic steady state (PSS) analysis is used to plot the reference current. A clock frequency of 100 kHz is used throughout the simulations. At V_{dd} = 0.5 V and room temperature (27°C), the circuit generates a reference current of 1 nA as shown in Figure 5.8a. In this figure, the average reference current is plotted for one clock period (10 μs) using PSS analysis.

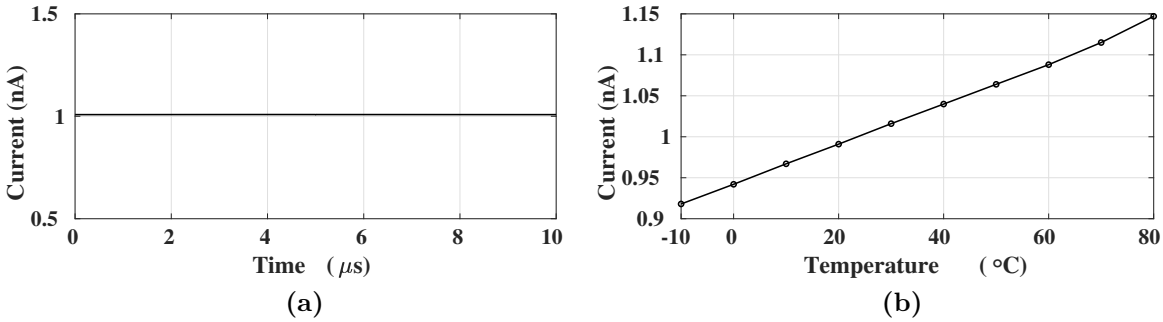


Figure 5.8: I_{ref} (a) with time, (b) with temperature.

Figure 5.8b plots I_{ref} with respect to temperature in the range of -10°C to 80°C for V_{dd} = 0.5 V and in the 'tt' corner. It can be seen that I_{ref} varies linearly with temperature. Hence, I_{ref} follows a PTAT characteristics.

In Figure 5.9, I_{ref} is plotted for V_{dd} values of 0.4 V, 0.5 V and 0.9 V at room temperature and in the 'tt' corner. I_{ref} is 0.998 nA and 1.012 nA for 0.4 V and 0.9 V respectively. From the above values, the supply voltage sensitivity of I_{ref} is calculated as 2.7 %/V. The circuit can be operated in a supply voltage range of 0.4 V - 0.9 V.

Figure 5.10 plots I_{ref} in different process corners (ss, ff, tt, fnsp and snfp) at room temperature with V_{dd} = 0.5 V. Maximum deviation of I_{ref} occurs in 'ss' and 'ff' corners. I_{ref} is 1.03 nA and 0.982 nA in 'ss' and 'ff' corners respectively. The maximum deviation is less than ±2.8 %.

Figure 5.11 shows the transient response of the current at the source of M_2. It contains ripples of magnitude about 0.15 nA. The transient response of the ripple free current flowing through M_9 is shown in Figure 5.12. The settling time is approximately 8 ms, which can be reduced by adding a start-up circuit to the proposed PTAT circuit.

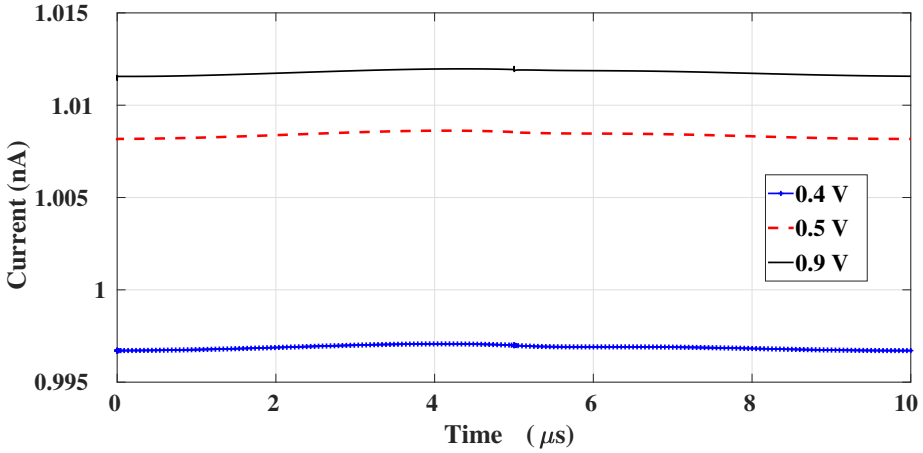


Figure 5.9: I_{ref} for different supply voltages.

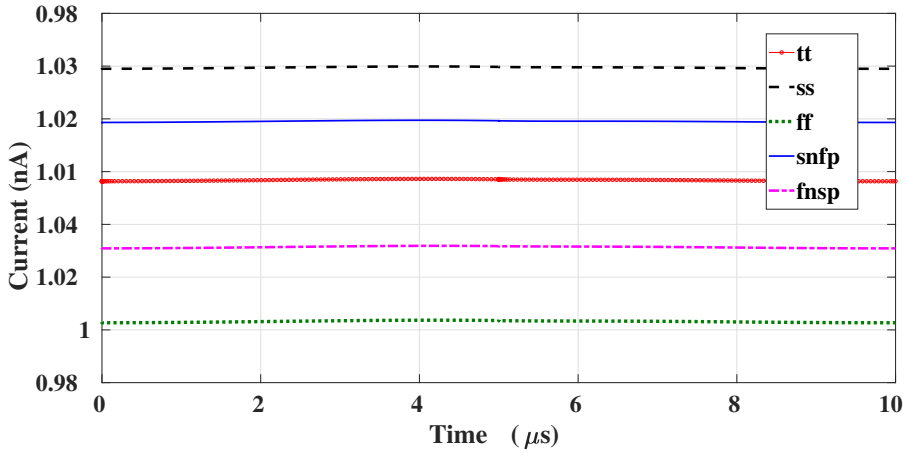


Figure 5.10: I_{ref} across the process corners.

The proposed circuit consumes a power of 1.5 nW at room temperature with V_{dd} = 0.5 V. A performance comparison of the proposed circuit with the state-of-the-art PTAT current reference circuits is given in Table 5.2. The proposed PTAT circuit operates with the lowest supply voltage and has the lowest supply voltage sensitivity among the papers listed. This circuit can be used as a biasing circuit in low voltage, low frequency log-domain and $G_m - C$ filter circuits to make the cutoff frequency of the filter independent of temperature.

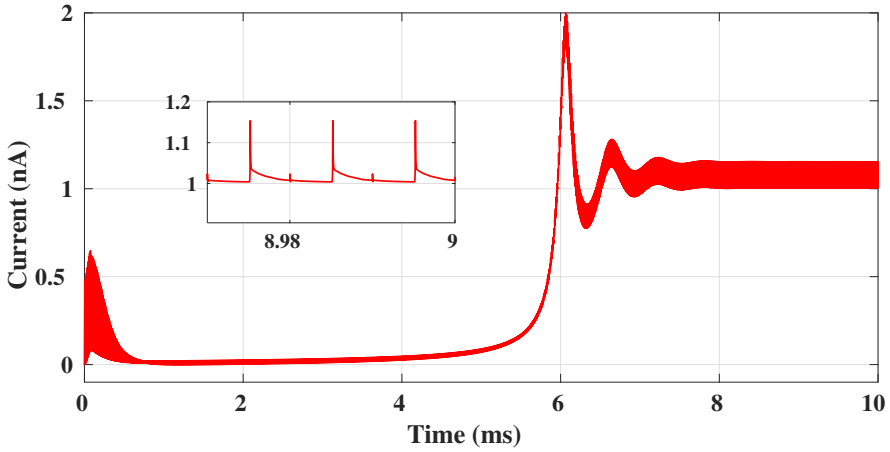


Figure 5.11: Transient response of the current (in Figure 5.7a) at the source of M_2.

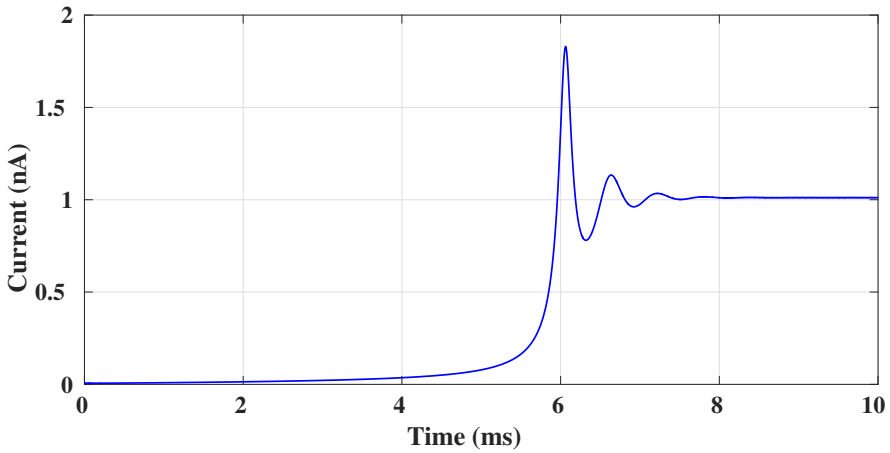


Figure 5.12: Transient response of the current flowing through M_9.

Table 5.2: Comparison of the proposed SC PTAT with other similar designs.

Parameter	Camacho-Galeano *et al.* 2005	Osaki *et al.* 2013	Jorge and Aita 2016	**This work**
Technology (μm)	1.5	0.18	0.04	**0.065**
V_{dd} (V)	1.2	1.2	1	**0.5**
I_{Ref} (nA)	0.4	6	100	**1**
Power (nW)	2	–	350	**1.5**
$S_{V_{dd}}^{I_{ref}}$ (%/V)	6	6.47	2.9	**2.7**

Chapter 6

CONCLUSIONS AND FUTURE DIRECTIONS

6.1 Conclusions

This thesis addresses the issues in designing low voltage, low power continuous time filters for low frequency applications. Three different designs of bulk-driven transconductors operating with supply voltages 0.3 V, 0.5 V and 0.8 V are proposed. To test the performance of these proposed designs, 2^{nd} order low frequency $G_m - C$ Butterworth LPFs are designed from 0.5 V and 0.8 V transconductors. A 4^{th} order $G_m - C$ Butterworth LPF with tunable cutoff frequency from 50 Hz to 250 Hz is designed using the 0.3 V transconductor. It is observed that DR and FoM1 of all these filters are comparable with many other similar designs reported in the literature.

In addition, a simple technique to increase the time constant of a filter without using large capacitors is proposed. Using this technique, low frequency 2^{nd} order SF and log domain LPFs are designed. It is observed that the capacitance/pole of these filters is the lowest among the similar designs given in the literature. Further, a 0.3 V bulk-driven VF is proposed and a 4^{th} order LPF with cutoff frequency tunable from 50 Hz to 250 Hz is designed by cascading the proposed bulk-driven VFs. This 4^{th} order VF LPF offers the lowest FoM2 compared to the state-of-the-art low frequency filters.

Current reference circuits are required to bias filter circuits. For this purpose, a couple of PTAT current reference circuits and a constant current reference circuit operating with supply voltages of 0.5 V and 0.8 V, are proposed. These current

reference circuits show better performance in terms of supply voltage sensitivity.

Monte Carlo simulations and simulations across PVT variations have been performed to check the robustness of these proposed designs. It is found that all the designs are robust across these variations.

6.2 Future Directions

One of the issues in designing CT filters is to maintain filter specifications (cutoff frequency and quality factor) constant across transistor mismatches and PVT variations. Automatic tuning circuits are used for fixing these filter specifications. The main focus of this research was to design low frequency filters with low voltage (≤ 0.8 V), low power (of the order of nW) and less area. Therefore, no significant effort has been made towards the design of automatic tuning circuits. It will be quite interesting to design on-chip automatic tuning circuits under these low voltage and low power conditions.

In recent years, SF and VF based filters have become popular for low power and low frequency applications. These filters are more linear and power efficient when compared to regular $G_m - C$ filters. They offer more DR even under low supply conditions. Design of SF and VF based filter architectures can be explored further.

In this thesis, the design of current reference circuits is not explored much. They require very large resistors which occupy more Si area to generate nA-range current. These large resistors can be replaced with transistors. One more challenge is to design these current reference circuits with ultra low supply voltage such as 0.3 V. It will be a challenging task to design nA-range current reference circuits without using large resistors and with supply voltage down to 0.3 V.

Since designing low voltage filter circuits for low frequency applications is quite challenging, the scope of research in designing such filter circuits is never-ending. Any analog circuit which can be thought of, is worthwhile to be tried for sub-1 V applications.

Appendix I
SUB-THRESHOLD REGION OF OPERATION

A-1 Introduction

In order to get lower transconductance and to reduce overall power consumption of the circuit, transistors are operated in sub-threshold (weak inversion) region. In this region, the drain current equation of a MOS transistor is given by (A.1) (Tsividis and McAndrew 2011, Taur and Ning 2013).

$$I_D = I_{D0}(\frac{W}{L})e^{\frac{V_{GS}-V_{th}}{\eta V_T}}(1-e^{\frac{-V_{DS}}{V_T}}) \tag{A.1}$$

where $I_{D0} = \mu_n C_{ox}(\eta-1)V_T^2$; μ_n, C_{ox}, η and V_T $(= kT/q)$ are mobility of the electron, capacitance per unit area presented by the gate oxide, sub-threshold slope factor and thermal voltage respectively. For saturation region $(V_{DS} \geq 4V_T)$, $1 - e^{\frac{-V_{DS}}{V_T}} \approx 1$. Hence, (A.1) is approximated to (A.2).

$$I_D = I_{D0}(\frac{W}{L})e^{\frac{V_{GS}-V_{th}}{\eta V_T}} \tag{A.2}$$

The transconductance of the transistor operating in sub-threshold saturation region is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{\eta V_T} \tag{A.3}$$

Hence, the current I_D can be reduced, to get low g_m.

Appendix II
PERFORMANCE METRICS OF A FILTER

A-2 Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is a measure to estimate the non-linearity of a system. It is defined as the ratio of sum of the powers of all harmonic components to the power of the fundamental component. It is expressed in percentage (%) or in decibels (dB). THD is also expressed in terms of RMS voltages as given in (A.4).

$$THD\,(dB) = 20\,log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ...}}{V_f}\right) \tag{A.4}$$

where V_i $(i = 2,\ 3,\ 4....)$ is the RMS voltage of i^{th} harmonic component. V_f is the RMS voltage of the fundamental component.

Lower THD indicates less distortion in the filter output. In general, a THD of 1 % (-40 dB) is considered as reference point.

A-3 Noise

As the biological signals are of low amplitude, the filter circuit must exhibit low input referred noise (IRN) to process these weak signals precisely. MOS devices exhibit thermal and flicker $(1/f)$ noises. The power spectral densities (PSDs) of thermal and

flicker noises of a transistor are given by (A.5) and (A.6) respectively (Razavi 2002).

$$\overline{i_{n,th}^2} = \frac{4}{3} kT\gamma g_m \tag{A.5}$$

$$\overline{i_{n,1/f}^2} = \frac{K_f}{C_{ox}WL}.\frac{1}{f}.g_m^2 \tag{A.6}$$

where the coefficient γ is 2/3 for long-channel devices, k is the Boltzmann constant and K_f is the flicker noise parameter.

From (A.6) it can be seen that the flicker noise can be reduced by increasing the gate area (WL) of the transistors.

A-4 Dynamic Range (DR)

Dynamic range is defined as the ratio of maximum input signal level to the minimum input signal level that a circuit can handle. Maximum input signal is limited by the distortion and minimum input is limited by the IRN. For continuous filters, dynamic range is defined as

$$\text{DR} = \frac{\text{RMS value of the input signal for a specified THD at the output}}{\text{Input referred noise}} \tag{A.7}$$

A-5 Figure of Merit

Figure of merit is used to evaluate the power efficiency of filter circuits. In this work, we have used two expressions for the figure of merit defined in (A.8) (Zhang *et al.* 2013) and (A.9) (Corbishley and Rodriguez-Villegas 2007).

$$FoM1 = \frac{P}{N \times f_o \times DR} \tag{A.8}$$

$$FoM2 = \frac{P \times V_{dd}}{N \times f_o \times DR} \tag{A.9}$$

where P is the total power consumption, N is the filter order and f_o is the cutoff frequency. Lower value of Figure of merit indicates better performance of the filter.

Bibliography

Adams, R. W., Filtering in the log domain. *In Audio Engineering Society Convention 63*. Audio Engineering Society, 1979.

Akbari, M. and **O. Hashemipour** (2017). A 63-dB gain OTA operating in subthreshold with 20-nW power consumption. *International Journal of Circuit Theory and Applications*, **45**(6), 843–850.

Alzaher, H. A. and **M. K. Algamdi** (2014). Employing R-0.5R networks in ultra-low bio-medical active-RC lowpass filters. *Analog Integrated Circuits and Signal Processing*, **81**(2), 407–416.

Amaljith, M., **G. H. Rao**, and **S. Rekha**, Low voltage current reference circuit with low temperature coefficient. *In 2018 IEEE Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER)*. IEEE, 2018.

Arya, R. and **J. P. Oliveira**, Gm-C biquad filter for low signal sensor applications. *In 23rd IEEE International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES-2016)*. 2016.

Baker, R. J. and **C. Boyce** (2005). Circuit design, layout, and simulation. *IEEE Press Series on Microelectronic Systems*.

Bruschi, P., **N. Nizza**, **F. Pieri**, **M. Schipani**, and **D. Cardisciani** (2007). A Fully Integrated Single-Ended 1.5–15-Hz Low-Pass Filter with Linear Tuning Law. *IEEE journal of Solid-State Circuits*, **42**(7), 1522–1528.

Camacho-Galeano, E. M., **C. Galup-Montoro**, and **M. C. Schneider** (2005). A 2-nW 1.1-V self-biased current reference in CMOS technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **52**(2), 61–65.

Chatterjee, S., **Y. Tsividis**, and **P. Kinget** (2005). 0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design. *IEEE journal of solid-state circuits*, **40**(12), 2373–2387.

Corbishley, P. and **E. Rodriguez-Villegas** (2007). A nanopower bandpass filter for detection of an acoustic signal in a wearable breathing detector. *IEEE Transactions on Biomedical Circuits and Systems*, **1**(3), 163–171.

Doménech-Asensi, G., **J. M. Carrillo-Calleja**, **J. Illade-Quinteiro**, **F. Martínez-Viviente**, **J. Á. Díaz-Madrid**, **F. Fernández-Luque**, **J. Zapata-Pérez**, **R. Ruiz-Merino**, and **M. A. Domínguez** (2014). Low-Frequency CMOS Bandpass Filter for PIR Sensors in Wireless Sensor Nodes. *IEEE Sensors Journal*, **14**(11), 4085–4094.

Enz, C., **M. Punzenberger**, and **D. Python** (1999). Low-voltage log-domain signal processing in CMOS and BiCMOS. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **46**(3), 279–289.

Enz, C. C., **F. Krummenacher**, and **E. A. Vittoz** (1995). An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. *Analog integrated circuits and signal processing*, **8**(1), 83–114.

Ferreira, L. H., **T. C. Pimenta**, and **R. L. Moreno** (2008). An ultra-low-voltage ultra-low-power weak inversion composite mos transistor: Concept and applications. *IEICE transactions on electronics*, **91**(4), 662–665.

Ferreira, L. H. and **S. R. Sonkusale** (2014). A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **61**(6), 1609–1617.

Frey, D. (1993). Log-domain filtering: an approach to current-mode filtering. *IEE Proceedings G (Circuits, Devices and Systems)*, **140**(6), 406–416.

Frey, D. (2000). Future implications of the log domain paradigm. *IEE Proceedings-Circuits, Devices and Systems*, **147**(1), 65–72.

Geiger, R. L. and **E. Sanchez-Sinencio** (1985). Active filter design using operational transconductance amplifiers: A tutorial. *IEEE Circuits and Devices Magazine*, **1**(2), 20–32.

Gerosa, A., **A. Maniero**, and **A. Neviani** (2004). A fully integrated dual-channel log-domain programmable preamplifier and filter for an implantable cardiac pacemaker. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **51**(10), 1916–1925.

Goldberger, A. L., **L. A. N. Amaral**, **L. Glass**, **J. M. Hausdorff**, **P. C. Ivanov**, **R. G. Mark**, **J. E. Mietus**, **G. B. Moody**, **C.-K. Peng**, and **H. E. Stanley** (2000). PhysioBank, PhysioToolkit, and PhysioNet: Components of a new research resource for complex physiologic signals. *Circulation*, **101**(23), e215–e220. Circulation Electronic Pages: http://circ.ahajournals.org/content/101/23/e215.full PMID:1085218; doi: 10.1161/01.CIR.101.23.e215.

Guzinski, A., **M. Bialko**, and **J. Matheau** (1987). Body driven differential amplifier for application in continuous-time active-C filter. *Proc. ECCD*, **87**, 315–319.

Hanumantha Rao, G. and **S. Rekha** (2019). A 0.8-V, 55.1-dB DR, 100 Hz Low-Pass Filter with Low-Power PTAT for Bio-Medical Applications. *IETE Journal of Research*, 1–11.

Jorge, V. and **A. L. Aita**, A 1-V PTAT current reference circuit with 0.05%/V current sensitivity to VDD. *In Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*. 2016.

Kafe, F., **F. A. Khanday**, and **C. Psychalinos** (2014). A 50 mHz Sinh-Domain High-pass Filter for Realizing an ECG Signal Acquisition System. *Circuits, Systems, and Signal Processing*, **33**(12), 3673–3696.

Kafe, F. and **C. Psychalinos** (2014). Realization of companding filters with large time-constants for biomedical applications. *Analog integrated circuits and signal processing*, **78**(1), 217–231.

Khanday, F. and **N. Shah** (2013). A low-voltage and low-power sinh-domain universal biquadratic filter for low-frequency applications. *Turkish Journal of Electrical Engineering & Computer Sciences*, **21**(Sup. 2), 2205–2217.

Khateb, F., **T. Kulej**, **M. Akbari**, and **P. Steffan** (2019). 0.3-V bulk-driven nanopower OTA-C integrator in 0.18 μm CMOS. *Circuits, Systems, and Signal Processing*, **38**(3), 1333–1341.

Krishna, J. R. M. and **T. Laxminidhi** (2018). Widely tunable low-pass gm-C filter for biomedical applications. *IET Circuits, Devices & Systems*.

La Croz-Blas, C., **A. Lopez-Martin**, and **A. Carlosena** (2005). 1.2 v 5 μW class-AB CMOS log-domain integrator with multidecade tuninig. *IEEE. Trans. Circuits Syst. II, Analog Digit. Signal process*, **52**(10), 665–668.

Lee, S.-Y. and **C.-J. Cheng** (2009). Systematic design and modeling of a OTA-C filter for portable ECG detection. *IEEE Transactions on Biomedical Circuits and Systems*, **3**(1), 53–64.

Li, H., **J. Zhang**, and **L. Wang** (2012). 5 mHz highpass filter with-80 dB total harmonic distortions. *Electronics letters*, **48**(12), 698–699.

Liu, Y.-T., **D. Y. Lie**, **W. Hu**, and **T. Nguyen**, An ultralow-power CMOS transconductor design with wide input linear range for biomedical applications. *In IEEE International Symposium on Circuits and Systems (ISCAS)*. 2012.

Mahmoud, S. A., **A. Bamakhramah**, and **S. A. Al-Tunaiji** (2013). Low-noise low-pass filter for ECG portable detection systems with digitally programmable range. *Circuits, Systems, and Signal Processing*, **32**(5), 2029–2045.

Martínez, J. and **A. Vazquez-Gonzalez**, Impedance Scalers for IC Active Filters. *In Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, 1998. ISCAS'98.*, volume 1. IEEE, 1998.

Mulder, J., **M. Kouwenhoven**, and **A. Van Roermund** (1997). Signal $\times$ noise intermodulation in translinear filters. *Electronics Letters*, **33**(14), 1205–1207.

Ng, A. E. and **J. I. Sewell** (2002). Direct noise analysis of log-domain filters. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **49**(2), 101–109.

Osaki, Y., **T. Hirose**, **N. Kuroki**, and **M. Numa** (2013). 1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V subbandgap reference circuits for nanowatt CMOS LSIs. *IEEE Journal of Solid-State Circuits*, **48**(6), 1530–1538.

Rao, G. H. and **S. Rekha** (2018). Low Voltage, Low Power Gm-C Filter for Low Frequency Applications. *Journal of Low Power Electronics*, **14**(2), 266–274.

Rao, G. H. and **S. Rekha** (2019). Time Constant Enhancement Technique for Low-Frequency Filters. *Circuits, Systems, and Signal Processing*, 1–14.

Razavi, B., *Design of analog CMOS integrated circuits*. Tata McGraw-Hill, 2002.

Rekha, S. and **T. Laxminidhi** (2016). Common Mode Feedback Circuits for Low Voltage Fully-Differential Amplifiers. *Journal of Circuits, Systems and Computers*, 1650124.

Rodriguez-Villegas, E., **A. J. Casson**, and **P. Corbishley** (2011). A subhertz nanopower low-pass filter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **58**(6), 351–355.

Rodriguez-Villegas, E., **A. Yúfera**, and **A. Rueda** (2004). A 1.25-V Micropower Gm-C Filter Based on FGMOS Transistors Operating in Weak Inversion. *IEEE Journal of Solid-State Circuits*, **39**(1), 100–111.

Sarpeshkar, R., **T. Delbruck**, and **C. A. Mead** (1993). White noise in MOS transistors and resistors. *IEEE Circuits and Devices Magazine*, **9**(6), 23–29.

Sarpeshkar, R., **R. F. Lyon**, and **C. Mead** (1997). A low-power wide-linear-range transconductance amplifier. *Analog Integrated Circuits and Signal Processing*, **13**(1-2), 123–151.

Sawigun, C., **S. Hiseni**, and **W. A. Serdijn**, A 0.45 nW, 0.5 V, 59-dB DR, Gm-C Low-pass Filter for Portable ECG Recording. *In BIODEVICES*. 2012.

Sawigun, C., **W. Ngamkham**, and **W. A. Serdijn** (2014). A 0.5-V, 2-nW, 55-dB DR, fourth-order bandpass filter using single branch biquads: An efficient design for FoM enhancement. *Microelectronics Journal*, **45**(4), 367–374.

Sawigun, C. and **W. A. Serdijn**, A modular transconductance reduction technique for very low-frequency G m-C filters. *In 2012 IEEE International Symposium on Circuits and Systems*. IEEE, 2012.

Sawigun, C. and **W. A. Serdijn**, *Analog IC Design Techniques for Nanopower Biomedical Signal Processing*, volume 1. River Publishers, 2016.

Sawigun, C. and **S. Thanapitak** (2018). A 0.9-nW, 101-Hz, and 46.3-μVrms IRN Low-Pass Filter for ECG Acquisition Using FVF Biquads. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **26**(11), 2290–2298.

Sawigun, C. and **S. Thanapitak** (2019). A Nanopower Biopotential Lowpass Filter Using Subthreshold Current-Reuse Biquads With Bulk Effect Self-Neutralization. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **66**(5), 1746–1757.

Schaumann, R., **H. Xiao**, and **V. V. Mac**, *Design of Analog Filters 2nd Edition*. Oxford University Press, Inc., 2009.

Seevinck, E. (1990). Companding current-mode integrator: A new circuit principle for continuous-time monolithic filters. *Electronics Letters*, **26**(24), 2046–2047.

Seevinck, E., **E. A. Vittoz**, **M. du Plessi**, **T.-H. Joubert**, and **W. Beetge** (2000). CMOS Translinear Circuits for Minimum Supply Voltage. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **47**(12), 1560–1564.

Shiue, M., **K. Yao**, **C. Gong**, *et al.* (2011). Tunable high resistance voltage-controlled pseudo-resistor with wide input voltage swing capability. *Electronics letters*, **47**(6), 377.

Silva-Martinez, J. and **J. Salcedo-Suñer** (1997). IC Voltage to Current Transducers with Very Small Transconductance. *Analog Integrated Circuits and Signal Processing*, **13**(3), 285–293.

Solís-Bustos, S., **J. Silva-Martínez**, **F. Maloberti**, and **E. Sánchez-Sinencio** (2000). A 60-dB Dynamic-Range CMOS Sixth-Order 2.4-Hz Low-Pass Filter for Medical Applications. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **47**(12), 1391–1398.

Sun, C.-Y. and **S.-Y. Lee** (2018). A fifth-order butterworth OTA-C LPF with multiple-Output differential-Input OTA for ECG applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **65**(4), 421–425.

Tajalli, A. and **Y. Leblebici** (2012). Power and area efficient MOSFET-C filter for very low frequency applications. *Analog Integrated Circuits and Signal Processing*, **70**(1), 123–132.

Taur, Y. and **T. H. Ning**, *Fundamentals of modern VLSI devices*. Cambridge university press, 2013.

Thanapitak, S. and **C. Sawigun** (2018). A subthreshold buffer-based biquadratic cell and its application to biopotential filter design. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **65**(9), 2774–2783.

Tsirimokou, G. and **C. Psychalinos** (2014). Realization of current-mirror filters with large time-constants. *AEU-International Journal of Electronics and Communications*, **68**(12), 1261–1264.

Tsividis, Y. and **C. McAndrew**, *Operation and Modeling of the MOS Transistor*. Oxford Univ. Press, 2011.

Veeravalli, A., **E. Sánchez-Sinencio**, and **J. Silva-Martínez** (2002). Transconductance Amplifier Structures with Very Small Transconductances: A Comparative Design Approach. *IEEE Journal of Solid-State Circuits*, **37**(6), 770–775.

Veldandi, H. and **R. A. Shaik** (2018). A 0.3-V Pseudo-Differential Bulk-Input OTA for Low-Frequency Applications. *Circuits, Systems, and Signal Processing*, **37**(12), 5199–5221.

Vlassis, S. (2012). 0.5 V CMOS inverter-based tunable transconductor. *Analog Integrated Circuits and Signal Processing*, **72**(1), 289–292.

Webster, J., *Medical Instrumentation: application and design*. John Wiley & Sons, 2009.

Wong, A., **K.-P. Pun**, **Y.-T. Zhang**, and **K. Hung** (2005). A Near-Infrared Heart Rate Measurement IC with Very Low Cutoff Frequency Using Current Steering Technique. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **52**(12), 2642–2647.

Yodprasit, U. and **J. Ngarmnil**, Micropower transconductor for very-low frequency filters. *In The 1998 IEEE Asia-Pacific Conference on Circuits and Systems, 1998. IEEE APCCAS 1998.*. IEEE, 1998.

Yodtean, A. and **A. Thanachayanont** (2013). Sub 1-V highly-linear low-power class-AB bulk-driven tunable CMOS transconductor. *Analog Integrated Circuits and Signal Processing*, **75**(3), 383–397.

Yu, C.-G. and **R. L. Geiger**, Very low voltage operational amplifiers using floating gate mos transistor. *In 1993 IEEE International Symposium on Circuits and Systems*. IEEE, 1993.

Zhang, J., **S.-C. Chan**, **H. Li**, and **L. Wang**, A 0.5 V 60 nW fully-differential log-domain band-pass filter with tunable cutoff frequency for biosensor applications. *In IEEE 12th International Conference on ASIC (ASICON)*. 2017.

Zhang, T.-T., **P.-I. Mak**, **M.-I. Vai**, **P.-U. Mak**, **M.-K. Law**, **S.-H. Pun**, **F. Wan**, and **R. P. Martins** (2013). 15-nW Biopotential LPFs in 0.35 μm CMOS Using Subthreshold-Source-Follower Biquads With and Without Gain Compensation. *IEEE transactions on biomedical circuits and systems*, **7**(5), 690–702.

Publications Based on the Thesis

Journals:

1. **Hanumantha Rao G.** and Rekha S. "Low Voltage, Low Power G_m-C Filter for Low Frequency applications," Journal of Low Power Electronics (American Scientific Publishers), vol. 14, no.2, pp. 266-274, June 2018.
2. **Hanumantha Rao G.** and Rekha S. "A 0.8-V, 55.1-dB DR, 100 Hz Low-pass Filter with Low-power PTAT for Bio-medical Applications," IETE Journal of Research (Taylor & Francis), 2019. https://doi.org/10.1080/03772063.2019.1682074
3. Sreenivasulu P., **Hanumantha Rao G.**, Rekha S. and M.S. Bhat "A 0.3 V, 56 dB DR, 100 Hz fourth order low-pass filter for ECG acquisition system," Microelectronics Journal (Elsevier), vol. 94, pp. 104652, 2019.
4. **Hanumantha Rao G.** and Rekha S. "Time Constant Enhancement Technique for Low-Frequency Filters," Circuits, Systems, and Signal Processing (Springer), vol. 39, no. 3, pp. 1213-1226, 2020.
5. **Hanumantha Rao G.** and Rekha S. "An area efficient, large time constant log domain filter for low frequency applications," International Journal of Circuit Theory and Applications (Wiley), vol. 48, no. 2, pp. 170-180, 2020.

Conferences:

1. **Hanumantha Rao G.** and Rekha S. "Low Voltage, Low Power Transconductor for Low Frequency Gm-C Filters," 21^{st} International Symposium, VLSI Design and Test (VDAT 2017), IIT Roorkee, India, vol. 711. pp. 83-92, Springer, 2017.

2. Amaljith MK, **Hanumantha Rao G.** and Rekha S. "Low voltage current reference circuit with low temperature coefficient," IEEE International Conference on

Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER), Mangalore, India, 2018, pp. 60-63.

3. **Hanumantha Rao G.** and Rekha S. ˜A 0.5 V, 1 nA Switched Capacitor PTAT Current Reference Circuit,˝ IEEE International Conference on Modeling of Systems Circuits and Devices (MOS-AK India), IIT Hyderabad, India, 2019, pp. 51-54.
4. **Hanumantha Rao G.**, Muhammed Mansoor C. B. and Rekha S. ˜A 0.8 V, 5 nA PTAT current reference circuit with improved supply voltage sensitivity,˝ IEEE sponsored Global Conference for advancement in Technology (GCAT), Bangalore, India, 2019, pp. 1-4.
5. **Hanumantha Rao G.**, Sreenivasulu P., Rekha S. and M.S. Bhat ˜Ultra Low-voltage, Low-power Fourth-order Butterworth LPF for ECG Signal Processing,˝ IEEE 2^{nd} International Conference on VLSI Device, Circuit and System (VLSI-DCS), Kolkata, India, 2020, pp. 105-108.

CURRICULUM VITAE

Hanumantha Rao Gottam
Jalalapalem Post, Vinukonda Mandal, Guntur District,
Andhra Pradesh - 522647.
☎ : +91 7406981798
✉ : hanu.vnk@gmail.com

Work Experience:

1. Assistant Lecturer in National Institute of Technology Calicut from Jan. 2015 - June 2015.
2. Assistant Lecturer in National Institute of Technology Puducherry from Aug. 2014 - Dec. 2014.
3. Intern in Processor Verification team, Applied Micro Circuits, Bangalore from Oct. 2013 to June 2014.

Education:

1. Ph.D. (Analog VLSI), National Institute of Technology Karnataka, Surathkal, 2020.
2. M.Tech. (VLSI Systems), National Institute of Technology Tiruchirappalli, 2013.
3. B.Tech. (ECE), Koneru Lakshmaiah College of Engineering, Andhra Pradesh, 2010.

Research Interests:

Design of Analog & Mixed Signal Circuits.

Publications:

Number of Journal publications: 7
Number of International Conference proceedings/publications: 7