INVESTIGATIONS ON PERFORMANCE IMPROVEMENT OF ELECTRICAL POWER DISTRIBUTION SYSTEM WITH INCORPORATION OF DSTATCOM AND DISTRIBUTED ENERGY SOURCES

Thesis

Submitted in partial fulfilment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

SANATH SARALAYA

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING,
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,
SURATHKAL, MANGALORE -575025

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DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled **"Investigations on Performance Improvement of Electrical Power Distribution System with Incorporation of DSTATCOM and Distributed Energy Sources"** which is being submitted to the **National Institute of Technology Karnataka, Surathkal** in partial fulfillment of the requirement for the award of the Degree of **Doctor of Philosophy** in **Department of Electrical and Electronics Engineering** is a *bonafide report of the research work carried out by me.* The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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Sanath Saralaya, 138010EE13F05

Department of Electrical and Electronics Engineering

Place: NITK-Surathkal

Date:02-08-2021

CERTIFICATE

This is to *certify* that the Research Thesis entitled **"Investigations on Performance Improvement of Electrical Power Distribution System with Incorporation of DSTATCOM and Distributed Energy Sources"** submitted by **Sanath Saralaya** (Register Number: 138010EE13F05) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

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(Research Guide)

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Abstract

In recent years, the usage of nonlinear loads in the distribution system has increased drastically. Because of these nonlinear loads, power quality problems result in the system. The power quality problems such as voltage sag-swell, harmonics, voltage flicker and unbalance in the system voltage will appear. The current situation in the distribution system has become complicated due to the injection of power from renewable energy sources into the distribution grid. The integration of distributed generation source to the distribution network has created more power quality issues such as voltage unbalance and harmonics problem. Due to these facts, in recent years, globally there is more concern for addressing power quality problems in modern distribution network. Custom power device is one of the solutions to solve power quality issues in distribution system. Distribution Static Compensator (DSTATCOM) is used in distribution system for performance improvement. This device supply the reactive power to the distribution system to ensure power factor improvement, voltage regulation along with harmonics mitigation, load balancing and neutral current compensation. Also, DSTATCOM is expected to enhance the performance of distribution system in presence of distributed generation sources.

Firstly, the efficient working of DSTATCOM depends on the control algorithm which is used to generate switching pulses for controlling devices. Most of controller, proposed in the literature, considers only positive sequence component. To overcome these problems, there is a need of developing a control strategy which has the ability to reduce negative sequence components and have advantages of both current and voltage control mode for the unbalanced load condition. In this work an improved control algorithm is proposed. This research work presents investigation of performance of DSTATCOM with proposed positive sequence controller and proposed positive and negative sequence controller in distribution system under different operation scenarios. The performance of proposed controllers are analysed for a test system and a 9 bus distribution system.

Secondly, in modern power system, the penetration of renewable energy sources has increased since there are no negative impact on environment.

According to grid codes, renewable energy sources are not required to contribute to restore the voltage stability. As a result, the reliability and voltage stability of the power grid is negatively affected due to disturbances. The DSTATCOM can be used to improve the low voltage ride through behavior of micro grids in both grid connected and islanded mode of operation. The compensation of positive and negative sequences components are required to support voltage restoration as well as the power grid stabilization and DSTATCOM should be able to give satisfactory performance in improving low voltage ride through capability. In this work, the performance of DSTATCOM in different fault scenario and low voltage ride through capacity of controller are studied.

Lastly, to get efficient operation, the DSTATCOM should be optimally placed and size should be determined. The primary goal of this work is to lessen the active power loss of the radial distribution system with voltage profile improvement. In this report, Ant Colony Optimization technique is utilized for the ideal position of DSTATCOM in the distribution framework for lessening of line losses and rise of voltage profile. Later, the performance is analysed by incorporating the DSTATCOM at an optimised location in a practical system. When DG is incorporated into the system, the characteristics of the system will change; it will lead to more power quality issues in the power distribution system. This operating scenario should also be considered during performance analysis of DSTATCOM and there is a need to study impact of DSTATCOM and DG on distribution system.

The MATLAB simulation is carried out and the performance of the proposed controllers are analysed with different cases by considering unbalanced load conditions and step change in the load. Also, the voltage ride through capability of DSTATCOM with proposed controller is studied. The observed results demonstrate that the overall system performance improves with the proposed positive and negative sequence controller.

The ant colony optimisation algorithm is applied on IEEE 33 and a real time practical 207 radial distribution system by using MATLAB program. Results demonstrate the reduction in line losses and rise in voltage profile for all test frameworks. From the impact analysis of distributed generators

and DSTATCOM on distribution system it is observed that the proper selection of DSTATCOM and distributed generator are need to be done for improving distribution systems performance.

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Nomenclature

P	Active Power
Q	Reactive Power
v_q, v_d,v_0	dq0 Component of Voltage at PCC
i_q,i_d,i_0	dq0 Component of Current
P_e	Active Power supplied from DSTATCOM
P_0	Active Power at PCC
P_f	Active Power Loss at Filter Components
Q_e	Reactive Power supplied from DSTATCOM
Q_0	Reactive Power at PCC
Q_f	Reactive Power Loss at Filter Components
v	Voltage magnitude at PCC
e_q, e_d,e_0	dq0 component of voltage at DSTATCOM terminal
L_f	Filter Inductance
R_f	Filter Resistance
ω	Angular Frequency
S_f	Apparent Power supplied from DSTATCOM
S_0	Apparent Power at PCC
S_f	Apparent Power Loss at Filter Components
v_a, v_b,v_c	3 phase Voltage at PCC
k_{pdc}, k_{idc}	Coefficients of PI controller with respect to the PI controller of DC link side
V_{dc}	DC Link Voltage
k_{pac}, k_{iac}	Coefficients of PI controller with respect to the PI controller of AC loop
v_{pcc}	Actual value of magnitude of voltage at PCC
V_{dc}^*	Reference value of DC link voltage
v_{pcc}^*	Reference value of magnitude of voltage at PCC
v_0^*	Reference value 0^{th} Component of voltage
v_a^*,v_b^*,v_c^*	Generated reference signal of voltages of all three phases
v_q^{+*}	Reference value for quadrature voltage positive sequence component
v_d^+,v_q^+	Positive sequence component of voltage in dq0 frame
v_n	Negative sequence component of PCC voltage
v_d^-,v_q^-	Negative sequence component of PCC voltage in dq0 frame.
v_{dref}^-,v_{qref}^-	Reference value of negative sequence voltage in dq0 frame.

i_{dn},i_{qn}	Negative sequence component of current in dq0 frame.
i_{dnref},i_{qnref}	Reference value of negative sequence current in dq0 frame.
i_{dref},i_{qref}	Generated Reference value of current in dq0 frame.
P_k, Q_k	Effective Active and Reactive power flowing from k node to k+1 node
P'_{k+1},Q'_{k+1}	Total Active and Reactive power at $(k+1)^{th}$ node.
R_k, X_k	Resistance and Reactance of branch k to (k+1)
$P_{L(k+1)}$, $Q_{L(k+1)}$	Loads that are connected at node k+1.
$V_k \angle \delta_k$	Voltage at node k
$V_{k+1} \angle \delta_{k+1}$	Voltage at node k+1
I_k	Current at branch between k and k+1
$V'_n \angle \theta'_n$	New voltage at bus n
$V_m \angle \theta_m$	Voltage at bus m
R_m	Resistance of branch between m and n
X_m	Reactance of branch between m and n
Z_m	Impedance of branch between m and n
$I_m \angle \delta$	Current at branch between m and n
I_{DS}	Current injected from DSTATCOM
Q_{DS}	Reactive power of DSTATCOM
P_k	Real power flowing out of bus
Q_k	Reactive power flowing out of bus
P_{Lk+1}	Real load power at bus k+1
Q_{Lk+1}	Reactive load power at bus k+1
$P_{LOSS}(k, k+1)$	Real power Loss in the line section connecting buses k and k+1
$Q_{LOSS}(k, k+1)$	Reactive power Loss in the line section connecting buses k and k+1
$P_{T,LOSS}$	Total Real power Loss
$Q_{T,LOSS}$	Total Reactive power Loss
$P^k_{i,j}(t)$	Probability function
τ_{ij}	Pheromone intensity on the (i,j) path
η_{ij}	Heuristic value for the (i,j) path
P_{lij}	Observed losses between the (i,j) path
α	Pheromone decay parameter
β	Relative importance of pheromone versus distance
ρ	The pheromone dissipation rate
$L^k(t)$	The total loss of the k^{th} ant's tour

P_{DGi}	The real power injection from DG placed at node i
P_{Di}	The load demand at node i
Q_i	The reactive power injection at node i
P_i	The real power injection at node i
z_{ij}	ij^{th} element of Zbus matrix
$v_i \angle \delta_i$	Voltage at node i
$v_j \angle \delta_j$	Voltage at node j
v_{LL}	AC line output voltage of VSC
C_{dc}	DC link capacitor
V_{ph}	The supply phase voltage
f_s	The switching frequency
i_{cr}	The acceptable percentage range of current ripple in VSC output current
a	The overloading factor
m	Modulation index
t	The time for which dc bus voltage is to be recovered

Abbreviations

FACTS	Flexible AC Transmission System
VSC	Voltage Source Converter
DSTATCOM	Distribution Static Compensator
STATCOM	Static Compensator
SRF	Synchronous Reference Frame
LLMF	Leaky Least Mean Forth
VFFRLS	Variable Forgetting Factor Recursive Least Square
LMS	Least Mean Square
VSLMS	Variable Step Size LMS
WTIDSTATCOM	Winding Tap Injection Distribution Static Synchronous Compensator
PBC	Passivity-Based Control
NBP	Naive Back Propagation
3P3W	Three Phase Three-Wire
DG	Distributed Generation
PCC	Point of Common Coupling
THD	Total Harmonic Distortion
GMIT	G Madegowda Institute of Technology
RMS	Root Mean Square
PI	Proportional Integral
SLG	Single Line to Ground
DLG	Double Line to Ground
DL	Double Line
TSP	Traveling Salesman Problem
QAP	Quadratic Assignment Problem
ACO	Ant Colony Optimization
AS	Ant System

Chapter 1

Introduction

1.1 Overview

There is a huge demand for electric power in industrial and domestic applications. The current global scenario indicates that load demand is more than generation. The generated electrical energy is transmitted through high voltage transmission line and distributed through the low voltage distribution lines. The distribution system interconnects the consumers and utility. As the demand increases, the complexity in the operation of system also increases. The distribution system supplies electric power to different types of customers like industrial, commercial and domestic customers with requirements differing from each other. The loads connected to the system comprise of linear or nonlinear loads. Because of all these factors, the system security and reliability decreases.

The modern distribution network configuration consists of distributed generation sources integrated to the network. Most of the distributed generation sources are renewable energy sources. Based on the availability of renewable energy sources, many installations are likely to be situated in remote locations where grid is weak in terms of poor voltage and power transporting capabilities. The renewable energy sources cannot produce AC supply as per voltage and frequency regulation limit without appropriate controller. In order to regulate the voltage and frequency, the power electronics converters are employed. These converters which interface distributed generation sources to the distribution grid will increase the complexity of the system.

Increase in the nonlinear loads and integration of renewable energy sources to the distribution system; create power quality issues such as harmonics, voltage fluctua-

tions, flicker, voltage sag and swell. The main solution for these problems is achieved predominantly by reactive power compensation. Essentially, power quality is determined by spectrum of supply received at load point. As the concern for power quality growing in recent days, utilities have started usage of custom power devices in their system. Custom power devices are specific devices based on semiconductor technology capable of supplying high quality reliable power and dynamic voltage control. These custom power devices primarily are FACTS devices. These devices are dedicated to improve the power quality and reliability of distribution system and protect the user from the disturbance produced by other users on the distribution network. Custom power devices are very much helpful in protection of loads which are sensitive to harmonics. These devices are either connected in series, shunt or combination of both with the distribution network.

At present a wide range of flexible controllers, which can control modern power electronic devices, are emerging for custom power devices. They are designed to overcome specific power quality problems.

DSTATCOM is a voltage source converter (VSC) based custom power device which is connected in shunt to the distribution network. The function of DSTATCOM is similar to STATCOM used at transmission level and both use voltage source converter of the suitable rating. However DSTATCOM, the VSC used is of type 1 converter with PWM control over the magnitude of the injected voltage and constant voltage across DC link (Padiyar, 2007). Faster semiconductor devices are used to enable the use of more efficient control schemes to functions to achieve load balancing, active filtering and flicker mitigation. Figure 1.1 shows the connection of DSTATCOM to distribution grid and figure 1.2 shows the three leg DSTATCOM.

The three phase distribution system is experiencing severe power quality problems such as harmonics, poor voltage regulation, load balancing and high reactive power burden. To mitigate these problems, DSTATCOM is proposed as one of the compensating device by many researchers. In literature, there are many topologies and different control algorithms are available to mitigate these problems. When distributed generations are integrated to the distribution system, the power quality problems become more severe. Few power quality issues with integration of distributed generation to network are voltage sag-swell, unbalance and harmonics. The topologies proposed in the literature are divided in to two parts, they are 3 phase 3 wire topology and 3 phase 4 wire topologies (Singh et al., 2014). Figure 1.3 shows the different topologies

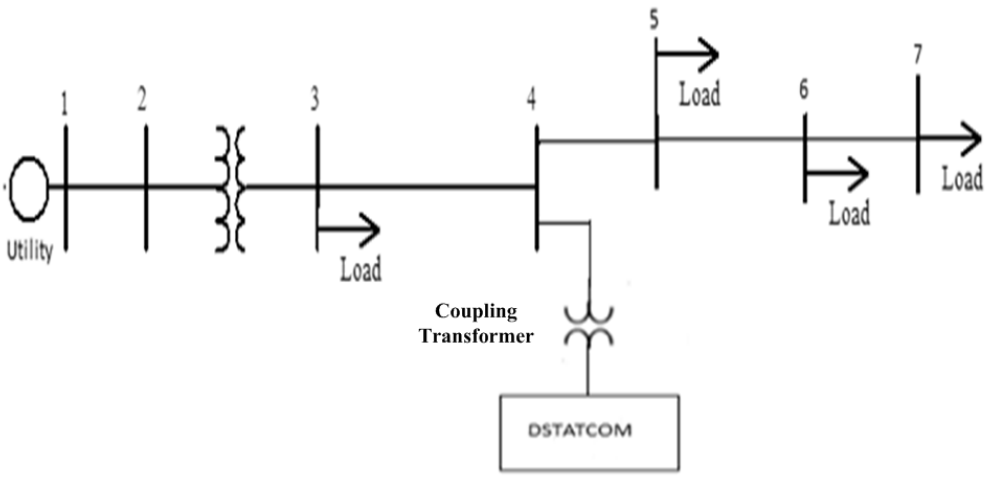


Figure 1.1: DSTATCOM connected to point of common coupling

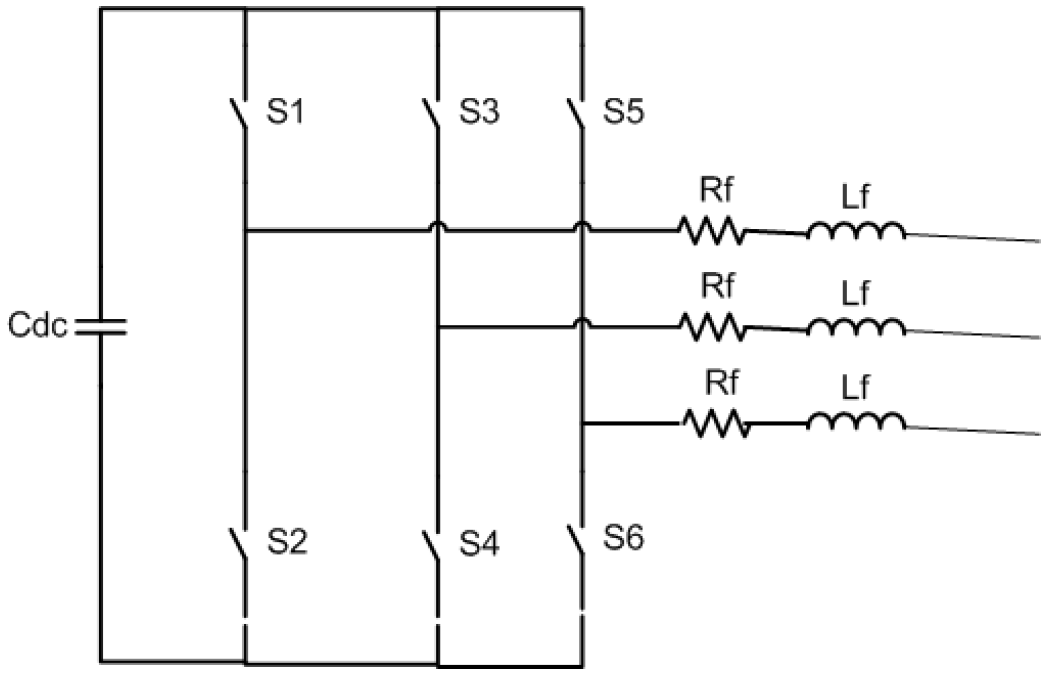


Figure 1.2: Three leg DSTATCOM

for 3 phase 3 wire DSTATCOM. Different topologies for 3 phase 4 wire is shown in figure 1.4.

DSTATCOM perform a noteworthy part in voltage balancing, improving voltage profile and lowering power losses in the system, under dynamic and steady state con-

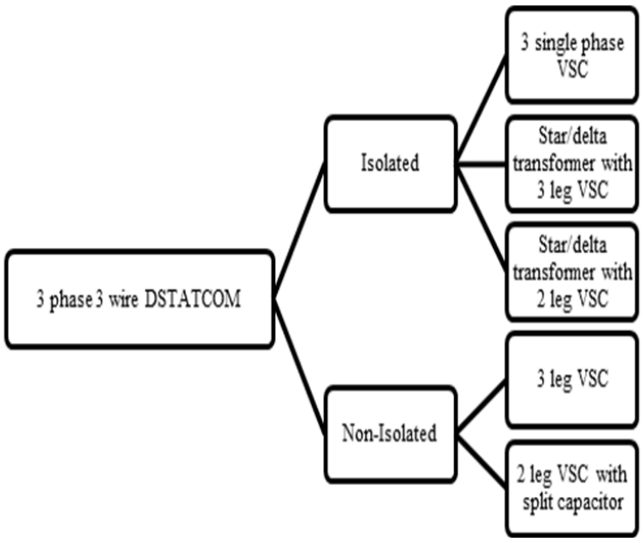


Figure 1.3: Different topologies for 3phase 3 wire DSTATCOM

ditions. The optimal performance of DSTATCOM depends on the control algorithm used. In literature, many topologies and control algorithms are proposed (Mishra et al., 2003, Kumar and Mishra, 2013, Comparatore et al., 2018). An improved current control algorithm is proposed using the self-tuned filter in DSTATCOM based on instantaneous reactive power theory for the extraction of fundamental component of load currents and reduce the switching ripples (Singh et al., 2015). In literature, the proportional integral controller is used as controller. But the tuning problem must be resolved satisfactorily. To overcome this issue, a fuzzy PI controller based algorithm is used in DSTATCOM to maintain the voltage stability in distribution network (Amoozegar, 2016).

The control algorithms are also proposed based on intelligent computation methods such as learning vector quantization, leaky least mean square, back propagation algorithms, etc. to enhance the power quality (Arya and Singh, 2013a,c,b, Singh et al., 2011). The different topologies are presented for four wire and three wire networks and aim to reduce the dc link rating. Supply of both reactive and real power from DSTATCOM is achieved by connecting active source to the VSC (Kannan and Rengarajan, 2012, Sundarabalan and Selvi, 2014).

A hybrid particle swarm optimisation – firefly algorithm based controller is proposed

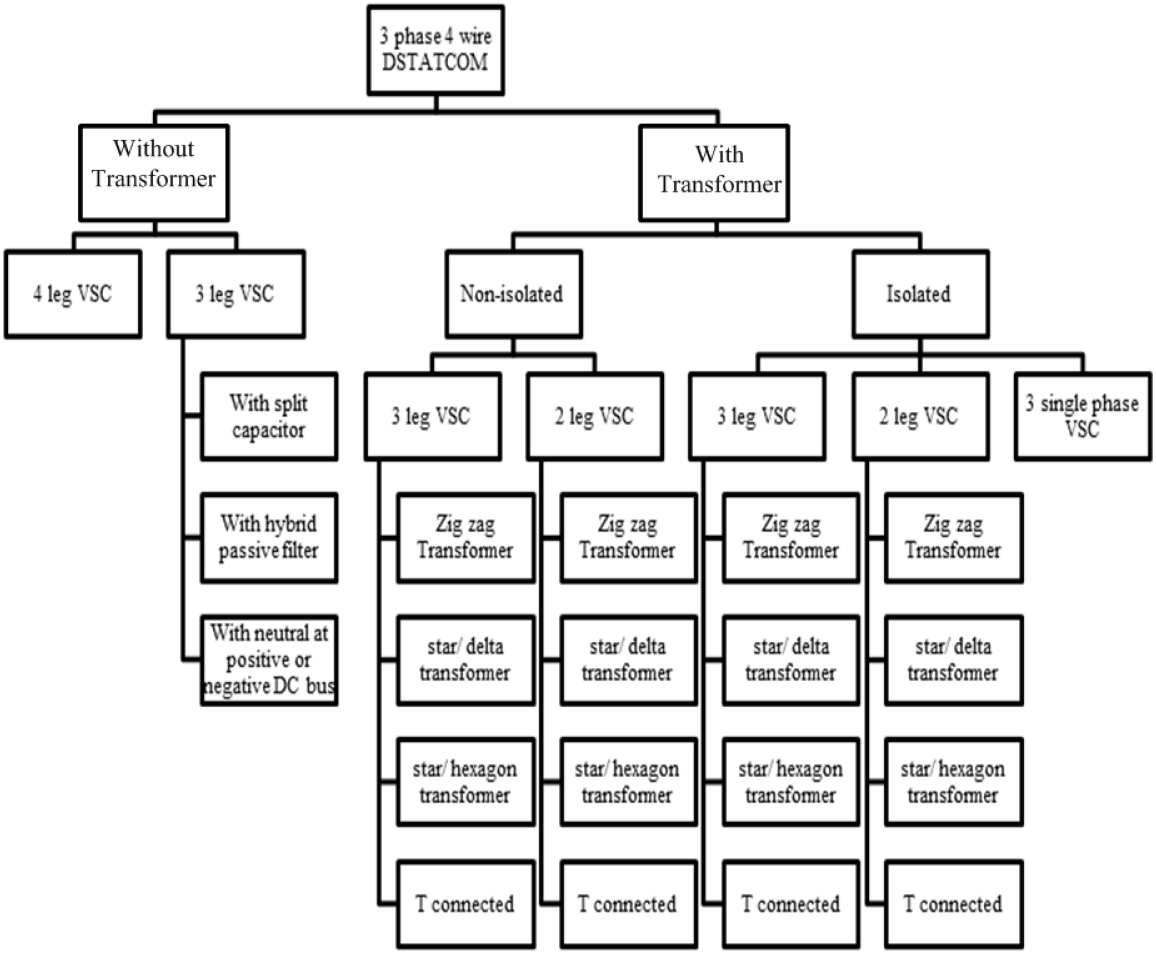


Figure 1.4: Different topologies for 3 phase 4 wire DSTATCOM

to enhance the power quality in wind power distribution system (Thirupathaiah, 2018). A study on the performance of DSTATCOM on power quality issues with the presence of wind energy is analysed. In this case, a DSTATCOM with battery is used with synchronous reference frame (SRF) based control algorithm (Mahela and Shaik, 2016). (Badoni et al., 2015) developed a SPV-DSTATCOM incorporating leaky least mean forth (LLMF) algorithm for the generation of reference currents and the same is implemented practically in a prototype of 6.8 kW. The performance of the DSTATCOM is analyzed under nonlinear loads, unbalanced nonlinear loads, in constant solar irradiation. It was found that the voltage fluctuations and harmonics are within the permissible limits in both the grid currents that are specified by IEEE -519

and IEEE-1547. (Kumar et al., 2010) employed a variable forgetting factor recursive least square (VFFRLS) control algorithm in three-phase DSTATCOM for calculating the reference current by extracting the active and reactive power components from the distorted non-sinusoidal load currents. The estimated reference current is used as switching pulses for the voltage source converter. The proposed algorithm is compared with the conventional recursive least square (RLS)-variable step size LMS (VSLMS) and it is found that VFFRLS algorithm performs better in mitigating the power quality.

(Lei et al., 2017) proposed a transformer winding tap injection distribution static synchronous compensator (WTIDSTATCOM) for medium-voltage reactive power compensation. Instead of utilizing auxiliary coupling transformer, the cascaded multilevel converter based DSTATCOM is connected to the tapping of the primary winding of the transformer. This connection enhances the usefulness of the transformer. Passivity-based control (PBC) strategy is used to control the DSTATCOM. The developed system increases the reactive power compensation and dynamic response of the system. (Mangaraj and Panda, 2018) a performance comparison of DSTATCOM is done by incorporating conventional icosϕ and proposed naive back propagation (NBP)-based icosϕ control algorithms for threephase three-wire (3P3W) distribution system under changing load condition. It is found that the developed control algorithm shows the superior performance in terms of voltage regulation, power factor enhancement and source current harmonic reduction. It also lessens the DSTATCOM rating. The performance evaluated for time variant and invariant load conditions. The selection of topology and reference algorithms are mainly dependant on the system requirement.

In many works, current control algorithms are presented. But very less work is done on voltage control mode algorithms (Kumar and Mishra, 2014b,a). The current sensorless voltage controllers based on power balancing theory are proposed in (Woei-Luen Chen and Yuan-Yih Hsu, 2003). In this, the authors considered only balanced voltage condition and have not tested for unbalanced and nonlinear load conditions. From the literature survey, it has been found that voltage control method is suitable for maintaining voltage at a desired value. However, it also found that current control method performs better than voltage control method for mitigating other current related power quality issues. Most of controller proposed in the literature considers only positive sequence component, but these controllers will fail in mitigating neg-

ative sequence component present in unbalanced system. In unbalanced condition, both positive and negative sequence components will be present in the system. So while developing a controller, both negative and positive sequence controller need to be considered. Therefore in this research work, an improved positive and negative sequence controller is presented for unbalanced load conditions. The improved controller is developed using power balancing theory using the synchronous reference frame.

1.2 Research Gaps and Research Objectives

1.2.1 Research Gaps

Based on the literature review carried out as mentioned in the previous section, the following research gaps were observed.

- Many control algorithms are found in literature which propose to mitigate different current related power quality issues using DSTATCOM. These algorithms are unable to efficiently overcome power quality issues. At the same time, in some literature it is found that voltage at the point of common coupling is kept at desired level, maintaining the voltage stability. In these cases, the DSTATCOM is only used for the purpose of voltage regulation. They do not discuss about power quality issues related to current. From the literature survey, it has been found that voltage control method is suitable for maintaining voltage at a desired value. However, it is also found that current control method performs better than voltage control method for mitigating other current related power quality issues. Most of controller proposed in the literature considers only positive sequence component. To overcome these problems there is a need of developing a control strategy which has the ability to reduce negative sequence components and have advantages of both current and voltage control mode for the unbalanced load condition.

- As observed from literature, the performance of DSTATCOM is not analysed when a fault occurs affecting the voltage at the point of common coupling. To maintain the voltage at load terminal the DSTATCOM can be used. So there is

a need to investigate the performance of DSTATCOM during the fault interval. DSTATCOM should able to give satisfactory performance in maintaining the desired voltage at the point of coupling.

- In literature, the developed control algorithm is investigated for different load and utility operating scenarios. To get efficient operation of DSTATCOM, it is required to analyse in larger distribution system. In larger system, the DSTATCOM should be optimally placed and size should be determined. Later, the performance is analysed by incorporating the DSTATCOM at an optimised location in a practical system.

- A fundamental part of the modern distribution system is a distributed generation source. When DG is incorporated into the system, the characteristics of the system will change; it will lead to more power quality issues in the power distribution system. This operating scenario should also be considered during performance analysis of DSTATCOM and there is a need to study the impact of DSTATCOM and DG on distribution system.

1.2.2 Research Objectives

Based on the research gaps discussed in the previous section, the objectives of the research is set as below:

- Development and performance analysis of control strategy for DSTATCOM with positive and negative sequence compensation.

- Performance analysis of DSTATCOM with proposed controller under fault scenario

- Performance analysis of optimal placed DSTATCOM with proposed control strategy

- Impact analysis of addition of distribution energy sources on system performance

1.2.3 Contributions

In DSTATCOM operation, controller plays a critical role in enhancing the quality of the power supplied to the customer. These can be done by developing an efficient controller for DSTATCOM. In this work an improved positive and negative sequence controller is proposed and the performance of this controller is analysed for different operating conditions and compared with existing positive sequence controller. The performance analysis is carried out using MATLAB/SIMULINK tool. The results are summarised below

- Performance improved positive sequence controller is found better in RMS voltage perception compared with existing positive sequence controller and improved positive and negative sequence controller.

- The PCC voltage and current THD are reduced using improved positive and negative sequence controller compared with existing positive sequence controller and improved positive sequence controller.

- In negative sequence voltage perception, it is found that the improved positive and negative sequence controller has better performance compared to existing positive sequence controller and improved positive sequence controller.

The performance of controller is also studied for different unsymmetrical fault conditions.The study results are summarised below

- The performance of DSTATCOM with improved positive and negative sequence controller found better in perception of voltage in each phase.

- From the analysis it is observed that during fault condition, DSTATCOM will contribute to the short circuit current. The contribution to short circuit current in the case of improved positive and negative sequence controller is less compared to the existing positive sequence controller.

- In negative sequence voltage perception, it is found that the improved positive and negative sequence controller has better performance compared to existing positive sequence controller.

To get efficient operation of DSTATCOM, it is required to analyse in larger distribution system. There is a need of optimal placement of DSTATCOM for efficient operation. An Ant Colony Optimaisation algorithm is developed to find the optimal location of DSTATCOM. IEEE 33 bus system and GMIT 207 bus systems are used to study the performance of developed algorithm and controller. The obtained results are summarized as below

- Using presented algorithm, optimal location and size of DSTATCOM is obtained for both IEEE 33 bus system and GMIT 207 bus system using MATLAB simulation

- Using presented algorithm, optimal location and size of DSTATCOM is obtained for both IEEE 33 bus system and GMIT 207 bus system using MATLAB simulation

- The load flow analysis with two DSTATCOM in IEEE 33 bus system and GMIT 207 bus system is performed. The voltage profile is increased compared to without DSTATCOM case and there is a significant reduction in power loss.

- The performance analysis of proposed positive and negative controller is performed in IEEE 33 bus system and GMIT 207 bus system by placing DSTATCOM at optimal location. From the results it is observed that using proposed controller the DSTATCOM is able to maintain the voltage 1 pu in both the systems.

In literature, DSTATCOM is used to increase the DG penetration and control the voltage within the standard voltage limit PCC on a distribution feeder. So it is required to study the performance of DSTATCOM with the presence of DG. IEEE 33 bus is used as test system. From the analysis, the observations are summarized as follows:

- On the perceptive of the voltage, performance with two DG and one DSTATCOM is found better compared to other combinations.

- On the perceptive of the power loss, performance with one DG and two DSTATCOM is found better compared to other combinations. The power loss is found maximum in the system without DG and DSTATCOM.

- On the perceptive of both voltage and power loss, performance with two DG and two DSTATCOM is found better compared to other combinations. In this case the voltage at 18^{th} bus is maintained at 0.979 pu and power loss is 0.081 MW.

1.3 Thesis Organization

The thesis has been organized into six chapters. The outline of the thesis is briefly discussed below:

Chapter 1: The context and motivation of the thesis, along with the literature review is presented. The research gaps, research objectives and dissertation outlines are discussed.

Chapter 2: In this chapter, initially an improved positive sequence controller is proposed considering unbalanced condition. The performance of this controller is analysed for different operating conditions and compared with existing positive sequence controller. These controllers are validated using MATLAB/SIMULINK for different scenarios. It has been observed from the results that the performance of proposed positive sequence controller found better in perspective of voltage at point of common coupling (PCC) and total harmonic distortions in case of unbalanced nonlinear load. When system voltage is unbalanced, there will be both positive and negative sequence components. To compensate both the components, it is required for DSTATCOM to produce both positive and negative sequence component in its output. To compensate both positive and negative sequence a modified controller is proposed. The performance of proposed positive and negative sequence controller is analysed for different operating conditions and results are compared with proposed positive sequence controller and existing positive sequence controller. It has been observed that, proposed positive and negative sequence controller is able to maintain voltage at PCC and also reduce voltage and current harmonics. This controller is also able to reduce negative sequence component in the system. The simulation was carried out by considering two different systems: a) Two bus system and b) IEEE 9 bus system without DSTATCOM, with existing positive sequence controller, improved positive sequence controller and improved positive and negative sequence controller.

Chapter 3: In this chapter, the existing positive sequence controller and improved positive and negative sequence controllers are analysed under fault scenario. Three

unsymmetrical disturbances are introduced such as single line to ground fault, double line fault and double line to ground fault. These faults are applied with and without DSTATCOM for different control strategy such as existing positive sequence controller and improved positive and negative sequence controller. The system voltage drop is analysed with fault current contribution. The simulation was carried out by considering three unsymmetrical faults: a) Single line to ground fault, b) Double line to ground fault and c) Double line fault without DSTATCOM, with existing positive sequence controller and improved positive and negative sequence controller.

Chapter 4: In this section optimal placement algorithm is discussed. In this work, for load flow analysis of distribution system the backward forward sweep method is used. For getting optimal location and size of DSTATCOM, ant colony method is used.

To assess the viability and effectiveness of the algorithm, the algorithm has been implemented on two different test systems for the following configurations.

- The system without DSTATCOM,
- The system with one DSTATCOM,
- The system with two DSTATCOM.

Location and size obtained by above algorithm is used to place the DSTATCOM with improved positive and negative sequence controller and performance of controller for different cases have been analysed. IEEE 33 bus system and GMIT 207 bus systems are simulated in PSCAD software for performance analysis.

Chapter 5: In modern power system, the interface of distribution generation sources to the distribution system is increasing day by day. The impact of distributed energy sources on the system performance with and without DSTATCOM, are presented in this chapter.

Chapter 6: This chapter summarizes the conclusions drawn from the research work carried out. Further, scope for future work is suggested.

Chapter 2

Design and Performance Analysis of Improvised Positive Sequence Controller for DSTATCOM

This chapter will cover the modeling of DSTATCOM control in detail. The design of existing positive sequence controller and improved positive sequence controller are discussed in the first section of this chapter. In the later section of the chapter, the simulation results of existing positive sequence controller and improved positive sequence controller are presented. The performance of these controllers are studied on IEEE 9 bus system connected with DSTATCOM.

The system configuration of distribution system with DSTATCOM is shown in Figure 2.1. The DSTATCOM is connected in shunt with the load consisting of voltage source converter (VSC) and filter. Ls and Rs representing the line inductance and resistance respectively. The main function of DSTATCOM is to maintain voltage at the PCC.

2.1 Existing Positive Sequence Controller

A positive sequence voltage controller is proposed by W. Chen and others (Woei-Luen Chen and Yuan-Yih Hsu, 2003) based on power balancing theory to control the output voltage. Block diagram of the existing positive sequence controller is shown in figure 2.2. This method is developed by considering balanced load condition. Although,

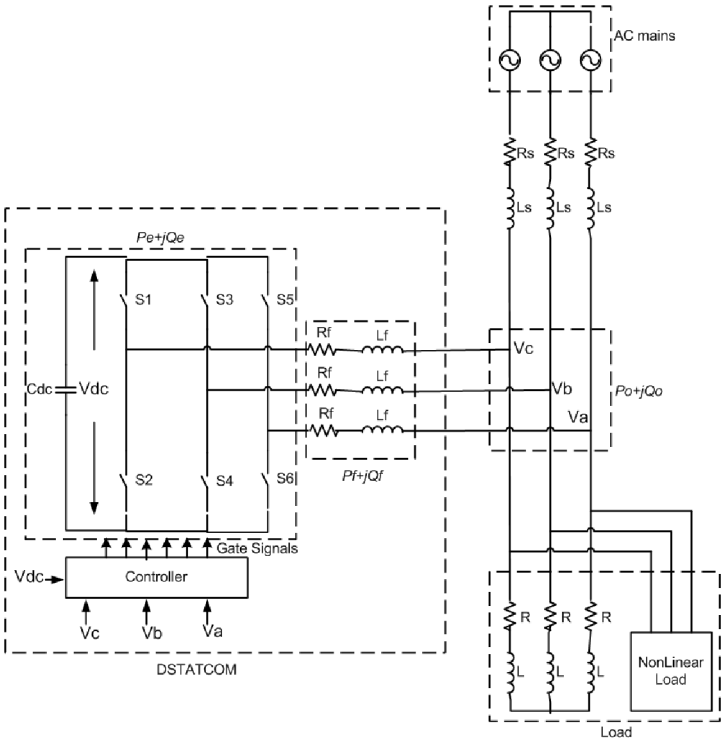


Figure 2.1: DSTATCOM System configuration

this control method has fast response for fluctuating load and good voltage regulation, it is suitable only for balanced load condition. v_d and v_q are the synchronous reference frame quantities of voltage and i_d and i_q are the dq0 components of the current. P and Q are real and reactive power respectively. From power balancing theory in balanced load condition,

$$P = \frac{3}{2}(v_q i_q + v_d i_d) \tag{2.1}$$

$$Q = \frac{3}{2}(v_d i_q - v_q i_d) \tag{2.2}$$

The voltage source converter power should be equal to the sum of power consumed by filter components and the power delivered to the power distribution system. The DSTATCOM power is given as $P_e + jQ_e$. $P_o + jQ_o$ and $P_f + jQ_f$ are the power supplied to the distribution network and power consumed by the filter respectively.

$$P_e = P_o + P_f \tag{2.3}$$

$$Q_e = Q_o + Q_f \tag{2.4}$$

For simplicity, in this method it is considered as, d axis is always in coincidence with instantaneous voltage and in quadrature with q axis. Hence

$$v_d = |v| \tag{2.5}$$

$$v_q = 0 \tag{2.6}$$

Using equation (2.1) and (2.2), the converter output is written as,

$$P_e = \frac{3}{2}(e_q i_q + e_d i_d) \tag{2.7}$$

$$Q_e = \frac{3}{2}(e_d i_q - e_q i_d) \tag{2.8}$$

The power delivered to the distribution system is given by,

$$P_o = \frac{3}{2}(v_q i_q + v_d i_d) = \frac{3}{2}|v| i_d \tag{2.9}$$

$$Q_o = \frac{3}{2}(v_d i_q - v_q i_d) = \frac{3}{2}|v| \tag{2.10}$$

The power consumed by filter is given by,

$$P_f = (i_d^2 + i_q^2) R_f \tag{2.11}$$

$$Q_f = (i_d^2 + i_q^2) \omega L_f \tag{2.12}$$

Substituting (2.7), (2.9) and (2.11) in (2.3),(Woei-Luen Chen and Yuan-Yih Hsu, 2003)

$$e_d = R_f i_d - \omega L_f i_q + |v| \tag{2.13}$$

Substituting (2.8), (2.10) and (2.12) in (2.4),(Woei-Luen Chen and Yuan-Yih Hsu, 2003)

$$e_q = R_f i_q + \omega L_f i_d \tag{2.14}$$

Obtained reference signals are converted to abc frame from dq frame and fed to PWM block as shown in the figure 2.2.

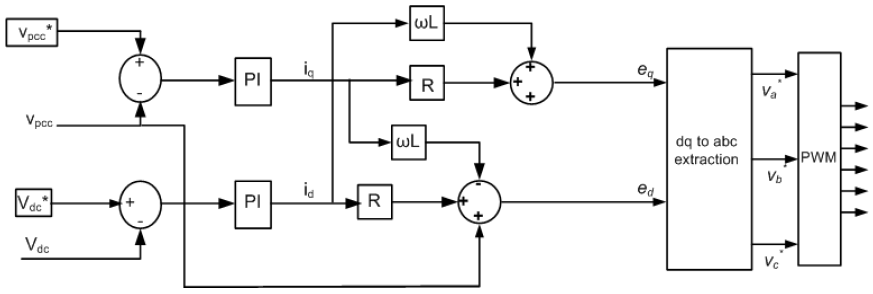


Figure 2.2: Existing Positive Sequence Controller Strategy for DSTATCOM

2.2 Improved Positive Sequence Controller

The existing positive sequence controller is suitable only for linear and balanced load condition. To overcome these limitations, an improved positive sequence control strategy has been presented to address unbalanced load condition. The real and reactive power under steady state condition of three phase system with unbalanced load conditions in terms of synchronous frame quantities are given in equation 2.15 and equation 2.16. v_d, v_q and v_0 are the synchronous reference frame quantities of voltage and i_d, i_q and i_0 are the dq0 components of current. P and Q are real and reactive power respectively.

$$P = \frac{3}{2}(v_q i_q + v_d i_d + 2v_0 i_0) \tag{2.15}$$

$$Q = \frac{3}{2}(v_d i_q - v_q i_d) \tag{2.16}$$

The power delivered from the voltage source converter should be equal to the total power delivered to the distribution network and the power loss in the filter. The DSTATCOM power is given as S_e. S_o and S_f are the power supplied to the distribution network and power consumed by the filter respectively. The flow of power from DSTATCOM to the distribution network is shown in figure 2.3. The power balancing equations are shown below:

$$S_e = S_o + S_f \tag{2.17}$$

$$P_e + jQ_e = (P_o + jQ_o) + (P_f + jQ_f) \tag{2.18}$$

$$P_e = P_o + P_f \tag{2.19}$$

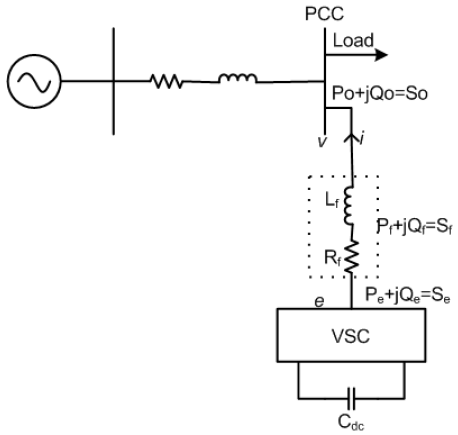


Figure 2.3: Single line diagram of 2 bus system with DSTATCOM

$$Q_e = Q_o + Q_f \tag{2.20}$$

From equation 2.15 and equation 2.16, the power delivered to the system synchronous reference frame are given by

$$P_o = \frac{3}{2}(v_q i_q + v_d i_d + 2v_0 i_0) \tag{2.21}$$

$$Q_o = \frac{3}{2}(v_d i_q - v_q i_d) \tag{2.22}$$

Similarly, the output power of DSTATCOM are given by

$$P_e = \frac{3}{2}(e_q i_q + e_d i_d + 2e_0 i_0) \tag{2.23}$$

$$Q_e = \frac{3}{2}(e_d i_q - e_q i_d) \tag{2.24}$$

The power absorbed by the filter components R_f and L_f are given by,

$$P_f = (i_d^2 + i_q^2)R_f \tag{2.25}$$

$$Q_f = (i_d^2 + i_q^2)\omega L_f \tag{2.26}$$

Substituting equation 2.21, equation 2.23, equation 2.25 in equation 2.19 yields,

$$\frac{3}{2}(e_q i_q + e_d i_d + 2e_0 i_0) = (i_d^2 + i_q^2)R_f + \frac{3}{2}(2v_o i_O + v_d i_d + v_q i_q) \tag{2.27}$$

Similarly, substituting equation 2.22, equation 2.24 and equation 2.26 in equation 2.20 gives,

$$\frac{3}{2}(e_d i_q - e_q i_d) = \frac{3}{2}(i_d^2 + i_q^2)\omega L_f + \frac{3}{2}(v_q i_d - v_d i_q) \tag{2.28}$$

Here an assumption is made that 0^{th} component will be supplied from inverter, that is $e_0 = v_0$. Therefore, equation 2.27 and equation 2.28 yield,

$$e_d = R_f i_d - \omega L_f i_q + v_d \tag{2.29}$$

$$e_q = R_f i_q + \omega L_f i_d + v_q \tag{2.30}$$

e_d and e_q are obtained from i_d, i_q and filter parameters R_f and L_f which is shown in equation 2.29 and equation 2.30.

Figure 2.3 shows the modified control strategy for DSTATCOM. From figure 2.3 it can be observed that, i_d and i_q are converted into e_d and e_q using filter parameters. As shown in figure 2.4, three phase voltages are transformed in to dq0 components.

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.31}$$

It can be observed from the figure 2.3 that the PI controller regulates DC link voltage and the output of PI controller is the real power current i_d, which is given in equation 2.32. The reactive power current i_q is obtained by the output of PI controller, which maintains the PCC voltage, given in equation 2.33.

$$i_d = (k_{pdc} + \frac{k_{idc}}{S})(V_{dc} - V_{dc}) \tag{2.32}$$

$$i_q = (k_{pac} + \frac{k_{iac}}{S})(V_{pcc} - V_{pcc}) \tag{2.33}$$

Where k_{pdc}, k_{idc}, k_{pac} and k_{iac} are the coefficients of PI controller with respect to the PI controller of DC link side and AC voltage loop, respectively. Substituting equation 2.32 and equation 2.33 in equation 2.29 and equation 2.30,

$$e_d = (k_{pdc} + \frac{k_{idc}}{S})(V_{dc}^* - V_{dc})R_f - \omega L_f(k_{pac} + k_{iac}S)(V_{pcc}^* - V_{pcc}) + V_d \tag{2.34}$$

$$e_q = (k_{pac} + \frac{k_{iac}}{S})(V^*_{pcc} - V_{pcc})R_f + \omega L_f(k_{pdc} + k_{idc}S)(V^*_{dc} - V_{dc} + V_q) \tag{2.35}$$

$$e_0 = v^*_0 - v_0 \tag{2.36}$$

From equation 2.24, equation 2.35 and equation 2.36, the output voltage of VSC is obtained by equation 2.37.

$$\begin{bmatrix} v^*_a \\ v^*_b \\ v^*_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \cos\theta & -\sin\theta \\ \frac{1}{\sqrt{2}} & \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} e_0 \\ e_d \\ e_q \end{bmatrix} \tag{2.37}$$

The obtained reference signals are fed to sinusoidal pulse width modulation block to generate the switching pulses at the desired switching frequency.

This control strategy is derived by considering the unbalance in the load. In un-

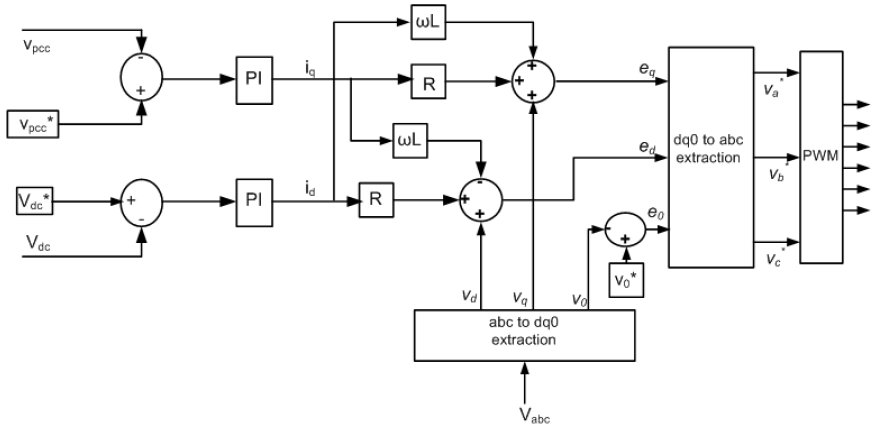


Figure 2.4: Improved Positive sequence Control Strategy for DSTATCOM

balanced condition, in dq0 frame the 0^{th} component will exist. This 0^{th} component is compared with reference value ($v^*_0 = 0$), the output of this block is taken as e_0 as shown in equation 2.36. e_d, e_q and e_0 are obtained by equation 2.34, equation 2.35 and equation 2.36 respectively. The reference voltage for PWM generation is obtained by equation 2.37. In the balanced load condition, in synchronous reference frame the 0^{th} component will be zero. Hence this improved method works similar to the existing method in literature. The pulses are generated using sinusoidal pulse width modulation technique. The reference voltage generated by equation 2.37 is given to PWM block as modulation signal.

2.3 Performance Analysis of Improved Positive Sequence Controller

The performance analysis of proposed controller is done using MATLAB/SIMULINK tool. The analysis of controller is done based on voltage at PCC, negative sequence components and THD perception.The design of DSTATCOM components are given in Appendix A. The PI controller parameters were obtained by trial and error method. The performance of this control strategy is validated for two different cases they are
i) Test system
ii) IEEE 9 bus system.

2.3.1 Test System

Figure 2.5 shows the test system used for analysis and table 2.1 gives the parameters of test system used for the simulation. The analysis of test system without DSTATCOM, with existing positive sequence controller and proposed improved positive sequence controller is presented. For the analysis, 220V is taken as base value for line voltage. Figure 2.6 shows the Simulink model of test system with DSTATCOM and controller. Figure 2.7 show the DSTATCOM model used for the simulation.

Table 2.1: Parameters of test system used for simulation

Parameters	**Values**	
System Frequency	50Hz	
MS Line Voltage	220V	
Supply line resistance	0.85Ω	
Supply line inductance	2.25mH	
Load	Za	60+j62.73Ω
	Zb	40+j78.5Ω
	Zc	50+j50.24Ω
	Nonlinear load	25Ω , 0.01H
C_{dc}	700μF	
R_f	0.2Ω	
L_f	15mH	

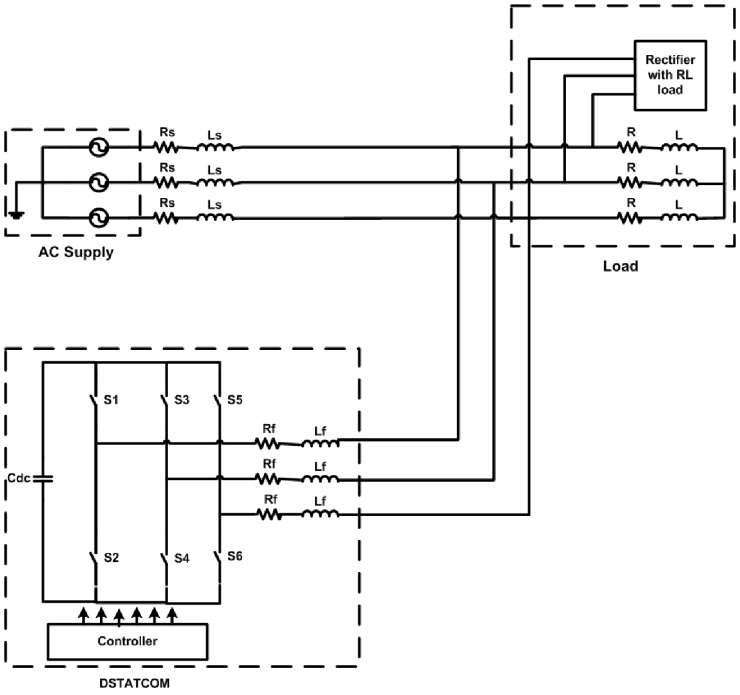


Figure 2.5: Test system

2.3.1.1 Enhancement of Voltage at PCC with Improved Positive Sequence Controller

Figure 2.8 shows the RMS voltage at PCC for all the three cases i.e. without DSTATCOM, with existing positive sequence controller and with proposed improved positive sequence controller. As shown in figure 2.8, the RMS voltage without DSTATCOM is 0.84 pu. The RMS voltage is maintained at 0.95 pu with existing positive sequence controller and with improvised positive sequence controller, it is 1 pu. From the table 2.2 it is observed that, based on the RMS voltage perspective the improvised positive sequence controller is found better than the existing positive sequence controller. Figure 2.9 shows the RMS voltage at PCC, when resistive load of 10 ohm is applied for each phase at 2s and removed at 3s. With proposed positive sequence controller, the voltage is maintained at 1 pu with response time of 5 cycles. Figure 2.10 shows the RMS voltage at PCC due to sudden decrease in the load. With proposed positive sequence controller the voltage is maintained near to 1 pu.

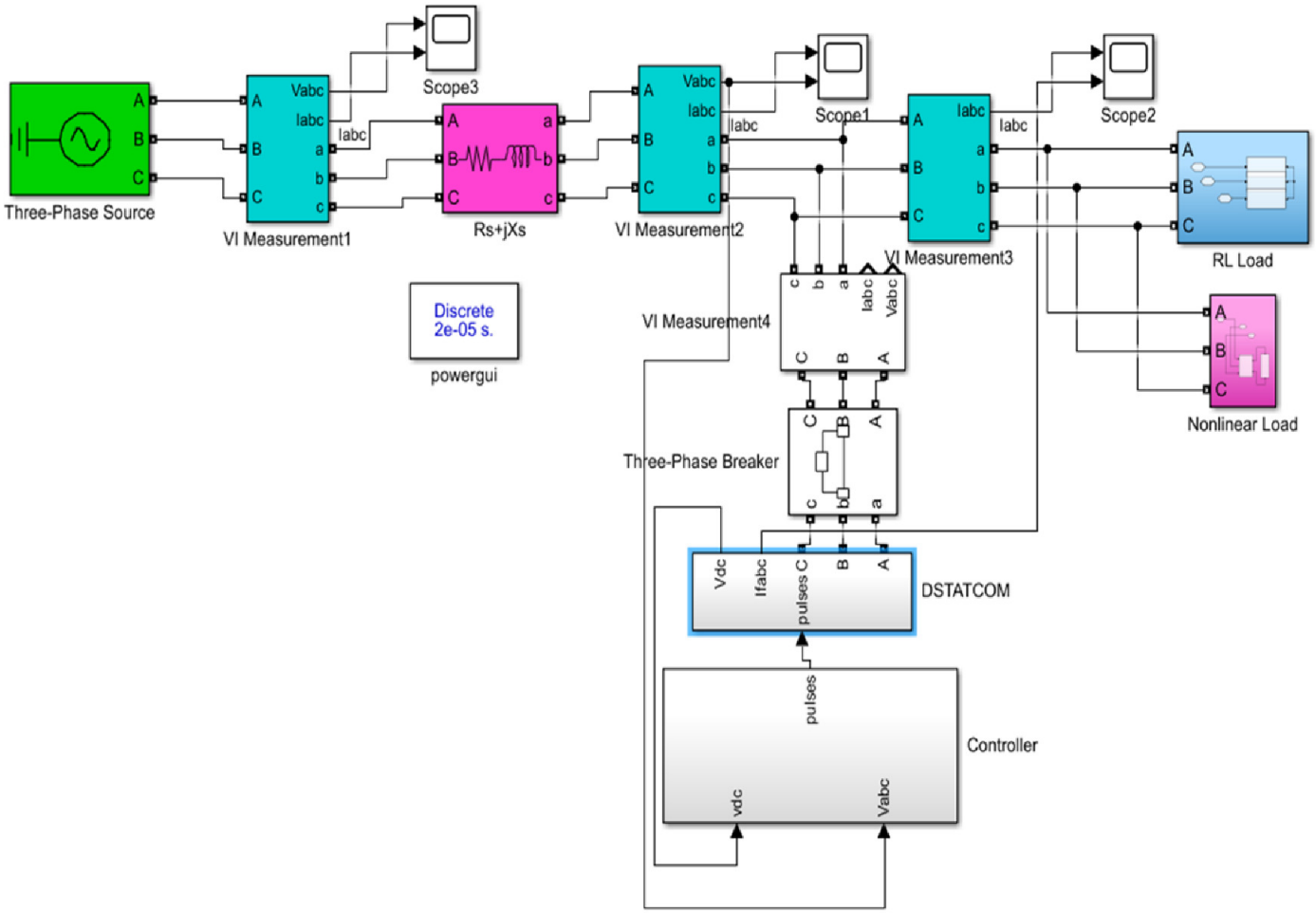


Figure 2.6: Simulink model of Test system

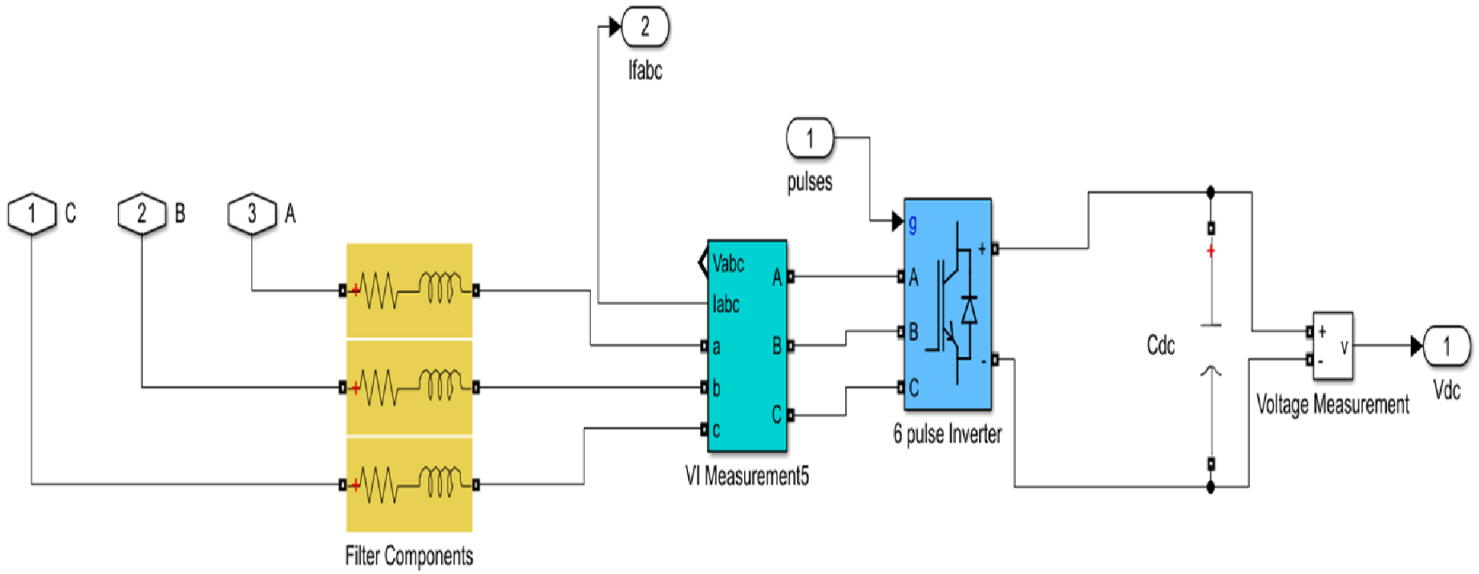


Figure 2.7: Simulink model of DSTATCOM

Table 2.2: RMS voltage at PCC without DSTATCOM and with positive sequence controlled DSTATCOM

	RMS Voltage in pu
Without DSTATCOM	0.84
With existing positive sequence controller	0.95
With improved positive sequence controller	1

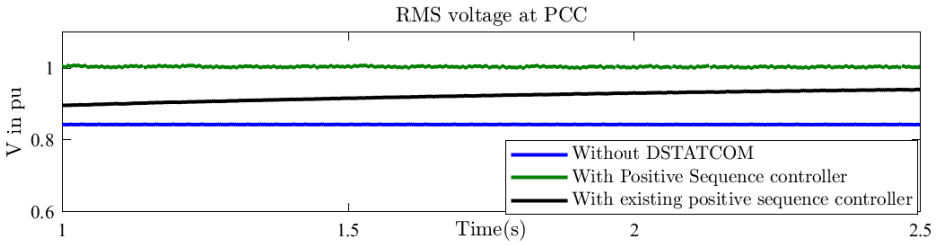


Figure 2.8: RMS voltage at PCC

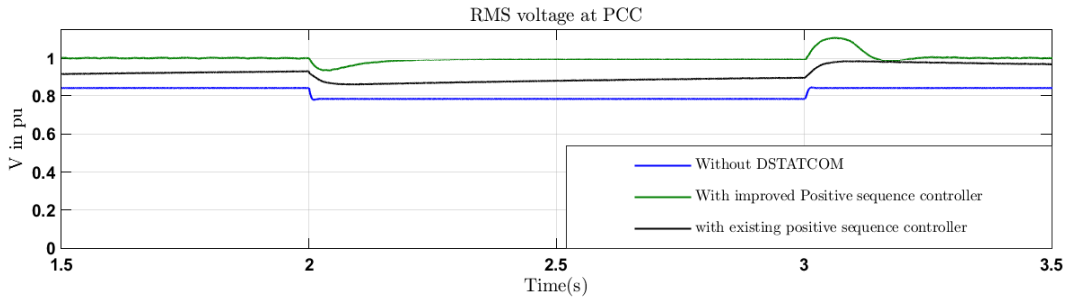


Figure 2.9: RMS voltage at PCC during increase in load

2.3.1.2 Reduction of Total Harmonic Distortion with Improved Positive Sequence Controller

Figure 2.11 shows the waveforms of instantaneous voltage at PCC without DSTATCOM, with existing positive sequence controller and improved positive sequence controller. Because of unbalance present in the load, the load current unbalance is observed as 13A, 12A and 12A and voltage of 168.5V, 168.7V and 168.6V with the presence of nonlinear load. But in the case of only linear load, the currents are ob-

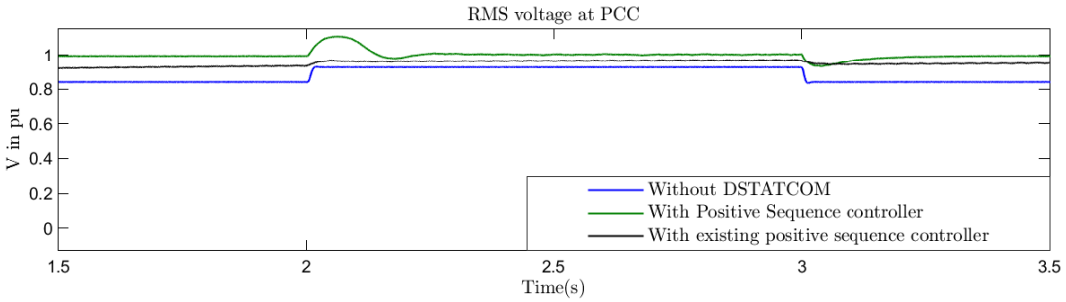
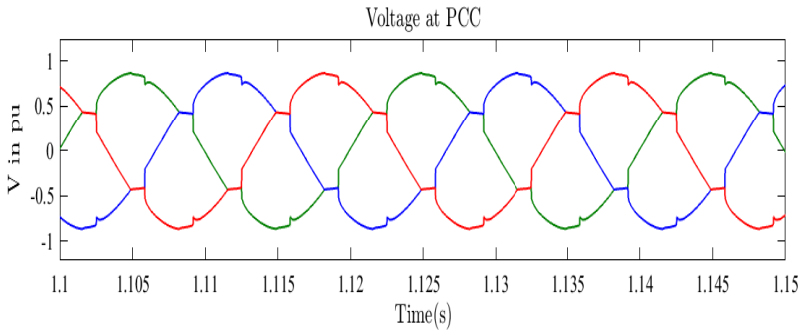


Figure 2.10: RMS voltage at PCC during decrease in load

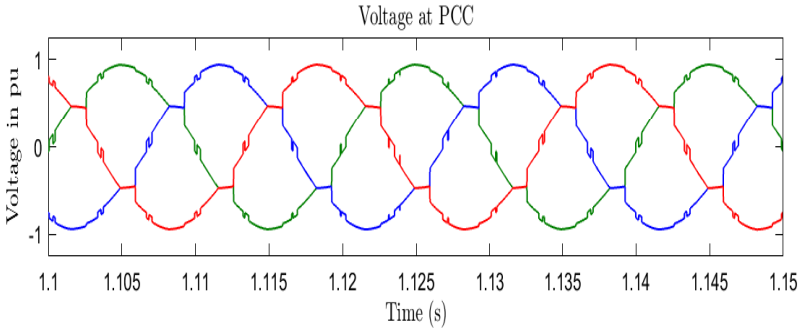
served as 2.29A, 2.1A and 2.12A and voltage of 171.1V, 177.4V and 177.1V. When it is converted to pu values the unbalnce is not visible in the waveform. Table 2.3 shows the percentage THD of PCC voltage and source current. The THD spectrum of PCC voltage and source currents are shown in the figure 2.12 and figure 2.13 respectively. From the table 2.3 it is observed that, the percentage THD of PCC voltage and source current are minimum in the case of improved positive sequence controller compared to the cases of without DSTATCOM and with existing positive sequence controller. From the figure 2.12, it is observed that the voltage THD in case of without DSTATCOM and existing controller is almost similar. So, the voltage at PCC at both these cases follows almost same prospective sinusoidal waveform. But in the case of proposed controller, the voltage THD is reduced to 2.2%. Hence, the disturbance is less compared to other two cases.

Table 2.3: Percentage THD PCC without DSTATCOM and with positive sequence controlled DSTATCOM in test system

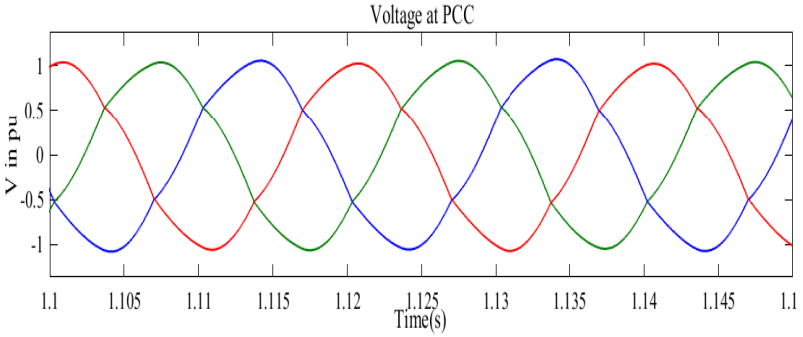
Parameter	**Without DSTATCOM**	**With existing positive sequence controller**	**With improved positive sequence controller**
% THD of PCC Voltage	8.69	7.98	2.224
% THD of Source Current	21.26	17.53	3.819



(a) Voltage at PCC without DSTATCOM



(b) Voltage at PCC with DSTATCOM with existing positive sequence controller

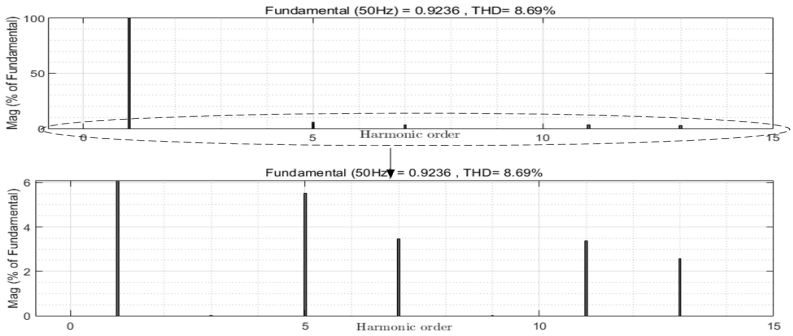


(c) Voltage at PCC with DSTATCOM with improved positive sequence controller

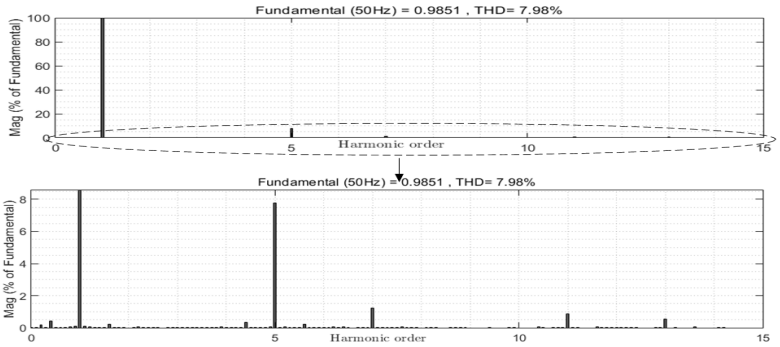
Figure 2.11: Voltage at PCC for different cases

2.3.1.3 Comparison of Negative Sequence Voltage with Improved Positive Sequence Controller

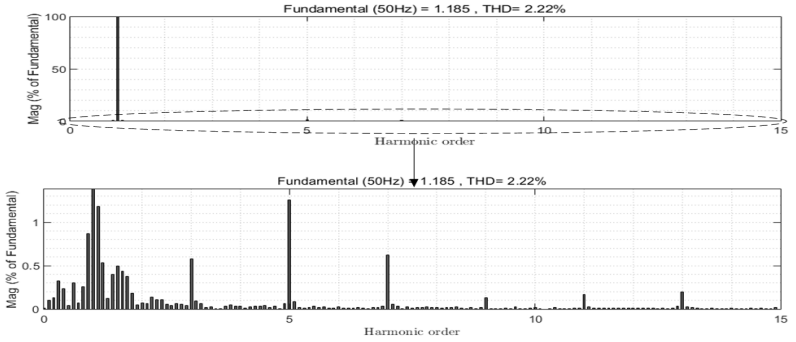
In unbalanced load condition, there will be both positive and negative sequence component. The table 2.4 shows the negative sequence component without DSTATCOM,



(a) THD spectrum of Voltage at PCC without DSTATCOM



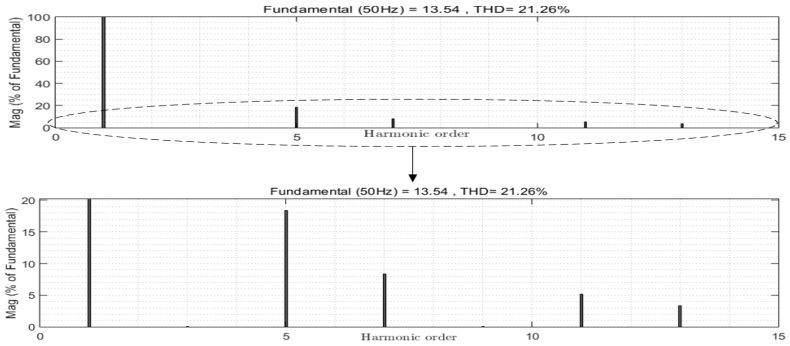
(b) THD spectrum of Voltage at PCC with DSTATCOM with existing positive sequence controller



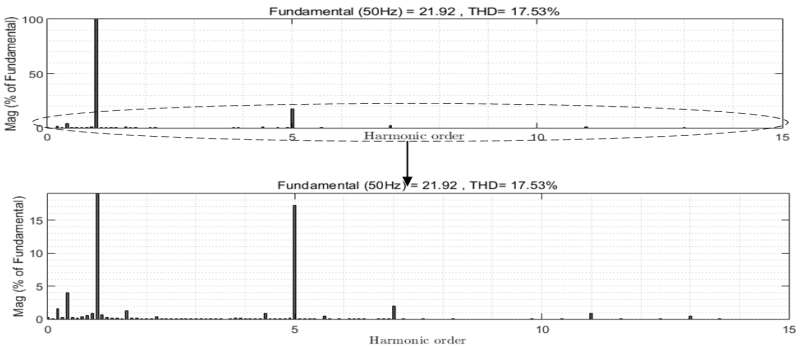
(c) THD spectrum of Voltage at PCC with DSTATCOM with improved positive sequence controller

Figure 2.12: THD spectrum of Voltage at PCC for different cases

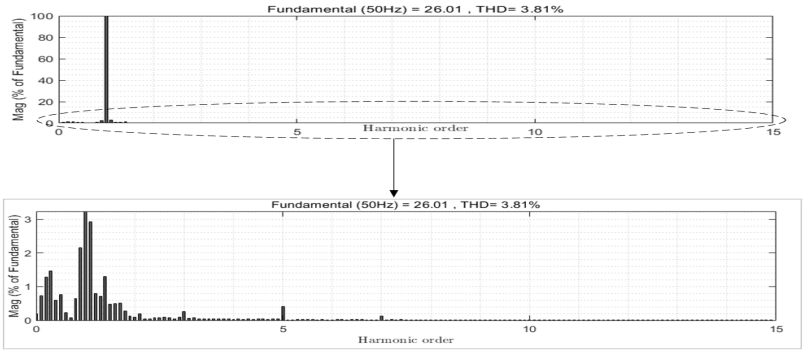
with existing positive sequence controller and improved positive sequence controller. From table 2.4 it is observed that, the magnitude of positive sequence components is 1 pu in the case of improved positive sequence controller. But the magnitude of negative sequence component is same in all the three cases.



(a) THD spectrum of source current without DSTATCOM



(b) THD spectrum of source current with DSTATCOM with existing positive sequence controller



(c) THD spectrum of source current with DSTATCOM with improved positive sequence controller

Figure 2.13: THD spectrum of source current for different cases

Table 2.5 shows the RMS voltage and THD for all the three cases. From the table, it is observed that the performance of improved positive sequence controller is better compared to the existing positive sequence controller. The THD of the source current is reduced from 21.26% to 3.819% and THD of PCC voltage is reduced from

Table 2.4: Magnitude of positive and negative sequence component without DSTATCOM and with positive sequence controlled DSTATCOM in test system

Parameter	**Without DSTATCOM**	**With existing positive sequence controller**	**With improved positive sequence controller**
Positive sequence voltage (pu)	0.84	0.93	1
Negative sequence voltage (pu)	0.13	0.13	0.13

Table 2.5: Summary of Results of test system without DSTATCOM and with positive sequence controlled DSTATCOM in test system

Parameter	**Without DSTATCOM**	**With existing positive sequence controller**	**With improved positive sequence controller**
RMS Voltage in pu	0.84	0.95	1
% THD of PCC Voltage	8.69	7.98	2.224
% THD of Source Current	21.26	17.53	3.819

8.69% to 2.224% which is within the IEEE standard value. The RMS voltage is also maintained at 1 pu. In the case of test system it is observed that, the performance of improved positive sequence is better than the existing positive sequence controller. The performance analysis of the DSTATCOM in IEEE 9 bus system with different controller is presented in the following section.

2.3.2 IEEE 9 Bus System

The performance analysis of DSTATCOM in IEEE 9 bus system is presented in this section. IEEE 9 bus system with DSTATCOM is shown in figure 2.14. For the purpose of analysis, a nonlinear load is connected at bus 6 and the DSTATCOM placed at bus 5. Data of IEEE 9 bus system is given in Appendix B (Rao and Narasimham, 2008). The base values of 10 MVA and 23 kV are considered for the analysis. Figure 2.15 shows the Simulink model of IEEE 9 bus system.

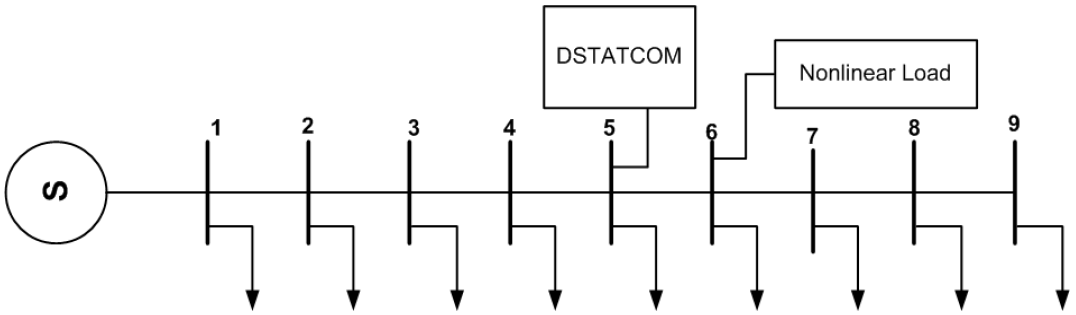


Figure 2.14: IEEE 9 bus system

2.3.2.1 Enhancement of Voltage at PCC with Improved Positive Sequence Controller

Figure 2.16 shows the RMS voltage in pu at bus number 5 for different cases. The RMS voltage at bus 5, without connecting DSTATCOM is 0.834 pu. When DSTATCOM is connected with existing positive sequence controller, the voltage at PCC is 0.95 pu. In the case of proposed improved positive sequence controller, the RMS voltage is increased to 0.987 pu. From the table 2.6 it is observed that the performance of improved positive sequence controller is better compared to existing positive sequence controller. Figure 2.17 shows the RMS voltage at PCC, when a load of 4.5 MW is applied at 2s and removed at 2.5s. With proposed positive sequence controller, the voltage is maintained at 0.98 pu with response time of 5 cycles. Figure 2.18 shows the RMS voltage at PCC due to sudden decrease in load. Step change in load is applied between 2s and 2.5s. With proposed positive sequence controller the voltage is maintained near to 1 pu.

Table 2.6: RMS voltage at PCC without DSTATCOM and with positive sequence controlled DSTATCOM at 5^{th} bus

	RMS Voltage in pu
Without DSTATCOM	0.834
With existing positive sequence controller	0.953
With improved positive sequence controller	0.987

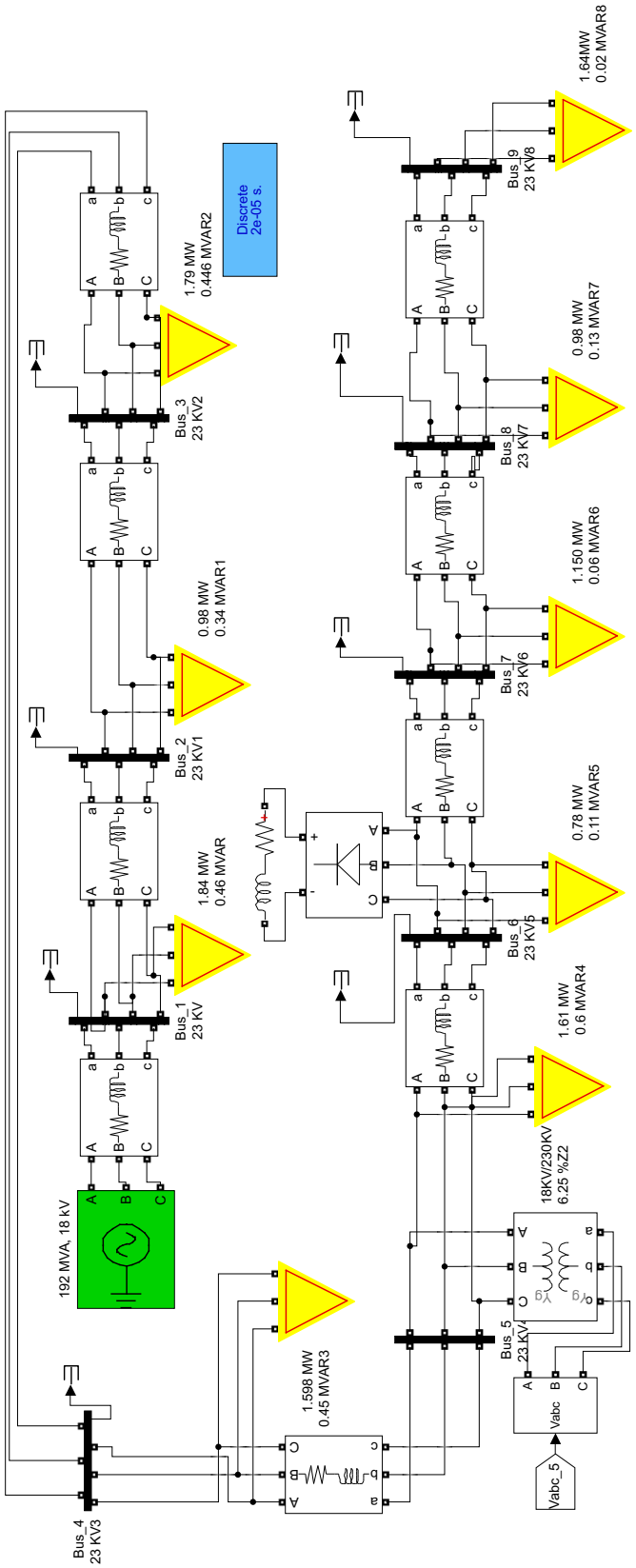


Figure 2.15: Simulink model of IEEE 9 bus system

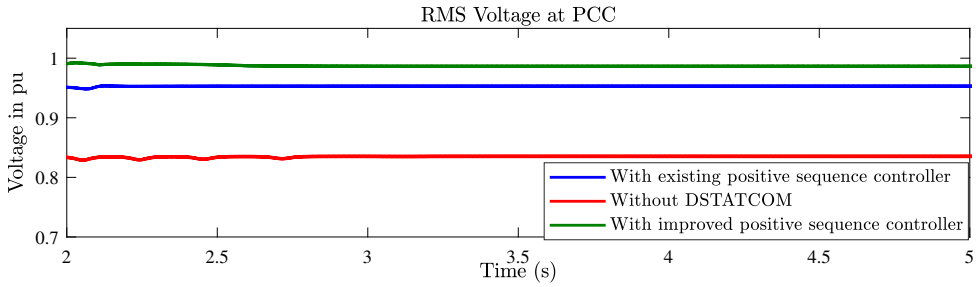


Figure 2.16: RMS voltage at bus 5

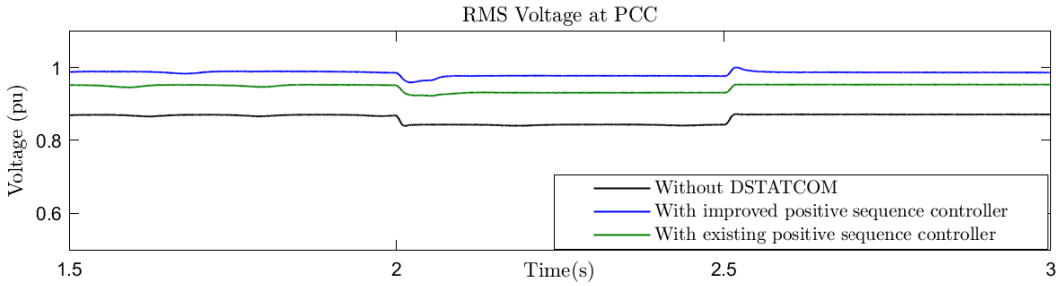


Figure 2.17: RMS voltage at PCC during increase in load

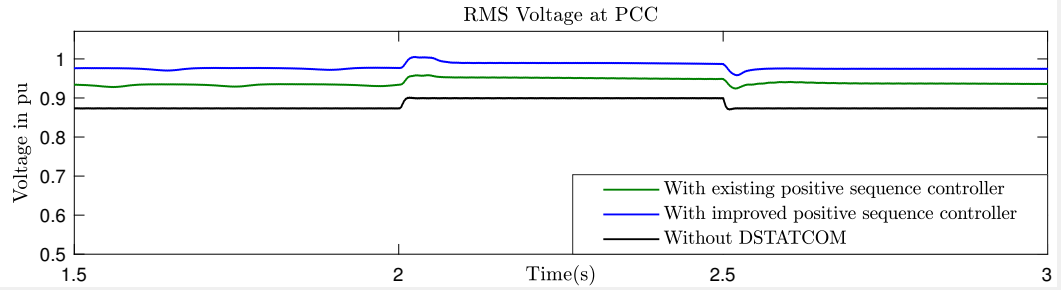


Figure 2.18: RMS voltage at PCC during decrease in load

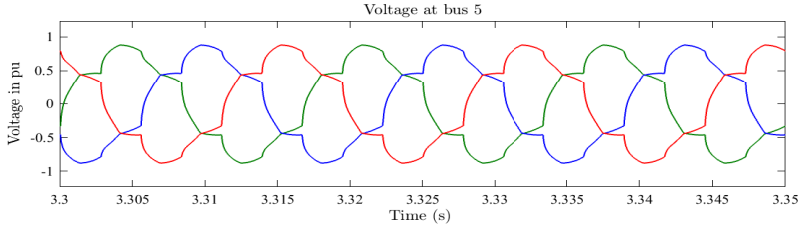
2.3.2.2 Reduction of Total Harmonic Distortion with Improved Positive Sequence Controller

Figure 2.19 shows the waveforms of instantaneous voltage at PCC without DSTATCOM, with existing positive sequence controller and improved positive sequence controller. Table 2.7 shows that the percentage THD of PCC voltage and source current. The THD spectrum of PCC voltage and source currents are shown in figure 2.20

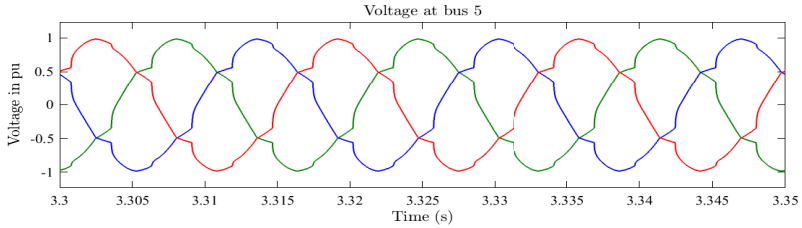
and figure 2.21 respectively. From the table it is observed that, the percentage THD of PCC voltage is minimum in the case of improved positive sequence controller compared to the cases of without DSTATCOM and with existing positive sequence controller.

Table 2.7: Percentage THD without DSTATCOM and with positive sequence controlled DSTATCOM in 9 bus system

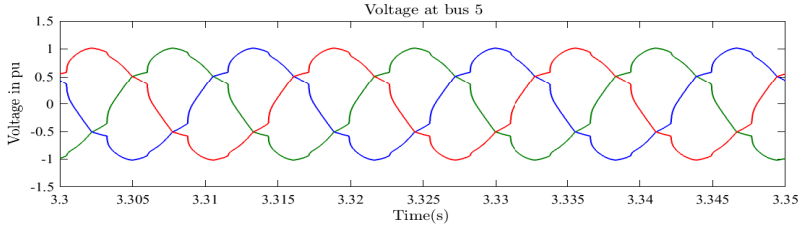
Parameter	**Without DSTATCOM**	**With existing positive sequence controller**	**With improved positive sequence controller**
% THD of PCC Voltage	9.2	8.4	7.8
% THD of Source Current	12.14	1.3	1.3



(a) Voltage at PCC without DSTATCOM

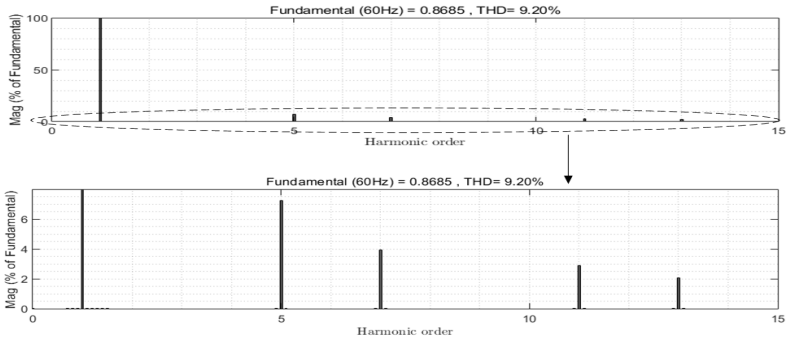


(b) Voltage at bus 5 with existing positive sequence controller

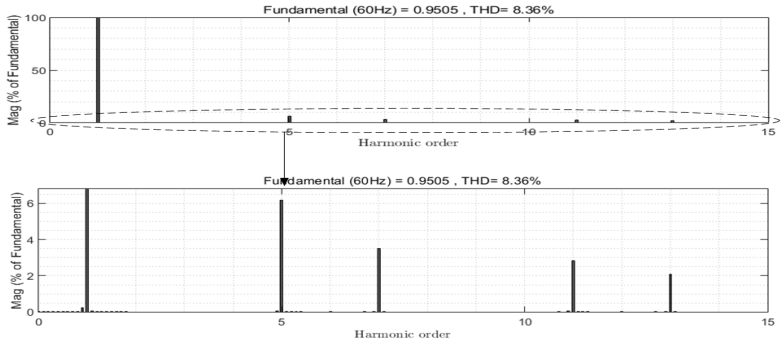


(c) Voltage at bus 5 with improved positive sequence controller

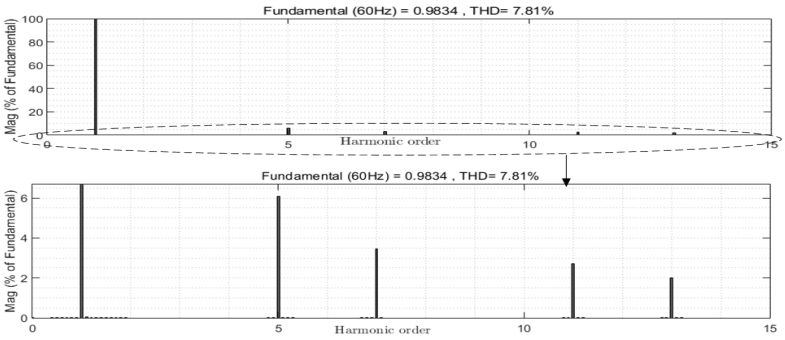
Figure 2.19: Voltage at bus 5 with different scenario



(a) THD spectrum of Voltage at PCC without DSTATCOM



(b) THD spectrum of Voltage at bus 5 with existing positive sequence controller

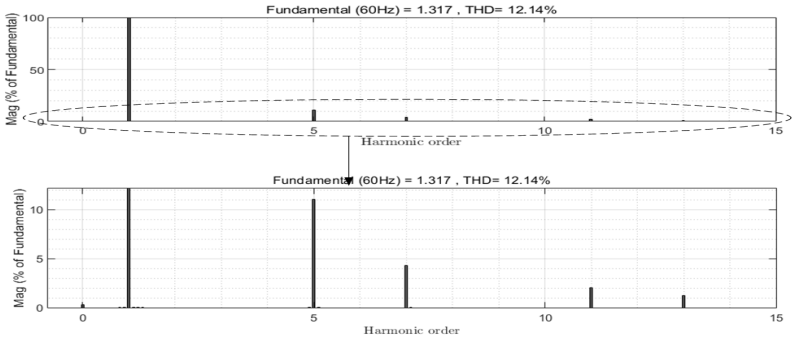


(c) THD spectrum of Voltage at bus 5 with improved positive sequence controller

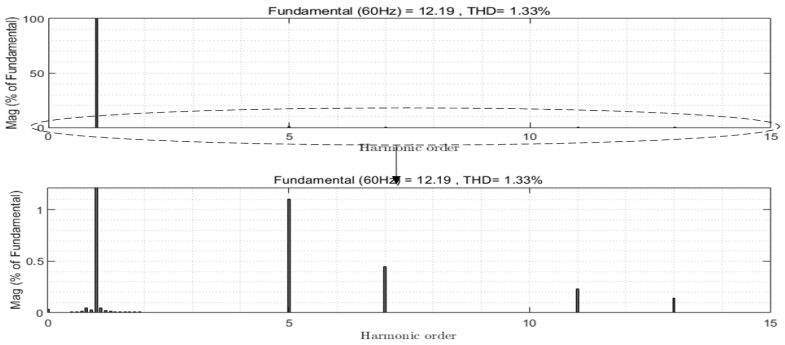
Figure 2.20: THD spectrum of Voltage at bus 5 with different scenario

2.3.2.3 Comparison of Negative Sequence Voltage with Improved Positive Sequence Controller

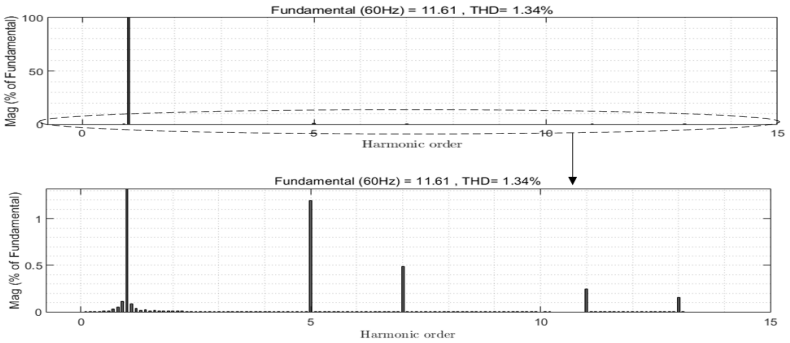
In unbalanced load condition, there will be both positive and negative sequence component. The table 2.8 shows the negative sequence component without DSTATCOM,



(a) THD spectrum of current without DSTATCOM



(b) THD spectrum of current with existing positive sequence controller



(c) THD spectrum of current with improved positive sequence controller

Figure 2.21: THD spectrum of current with different scenario

with existing positive sequence controller and improved positive sequence controller. From table 2.8 it is observed that, the magnitude of negative sequence component is increased by 0.03 pu in the case of existing positive sequence controller.The existing controller has designed considering balanced load conditions but the proposed positive sequence controller is designed by considering unbalanced load condition. But

the proposed positive sequence controller doesn't have effect on negative sequence component in terms of reduction.

Table 2.8: Magnitude of positive and negative sequence component without DSTATCOM and with positive sequence controlled DSTATCOM in IEEE 9 bus system

Parameter	**Without DSTATCOM**	**With existing positive sequence controller**	**With improved positive sequence controller**
Negative sequence voltage (pu)	0.21	0.24	0.21

Table 2.9: Summary of Results of 9 bus system

Parameter	**Without DSTATCOM**	**With existing positive sequence controller**	**With improved positive sequence controller**
RMS Voltage in pu	0.834	0.953	0.987
% THD of PCC Voltage	9.2	8.4	7.8
% THD of Source Current	12.14	1.3	1.3
Negative sequence Voltage(pu)	0.21	0.24	0.21

Table 2.9 shows the RMS voltage and THD for all the three cases. From the table, it is observed that the performance of improved positive sequence controller is better compared to existing positive sequence controller. THD of PCC voltage is reduced from 9.8% to 7.8%. The RMS voltage is also maintained at 0.987 pu. In the case of IEEE 9 bus system it is observed that, the performance of improved positive sequence controller is better than the existing positive sequence controller in terms of maintaining RMS voltage and PCC voltage THD reduction.

From the performance analysis of existing positive sequence controller and improved positive sequence controller it is observed that, the performance of improved positive sequence controller found better compared to existing positive sequence controller in terms of RMS voltage and reduction of THD. But the controller fails to compensate negative sequence component in both the cases. Because modeling of improved positive sequence controller considers only positive sequence part of the voltage. When

system is unbalanced there will be negative sequence components, which is also need to be compensated. For the compensation of both positive and negative sequence components, this controller is modified again as improved positive and negative sequence controller and presented in the next section.

2.4 Improved Positive and Negative Sequence Controller

In previous section, the modeling of proposed improved positive sequence controller is presented. When system voltage is unbalanced, there will be both positive and negative sequence components. To compensate both the components, the DSTATCOM has to produce both positive and negative sequence component in its output. To compensate both positive and negative sequence a modified controller is proposed in this section. To compensate the positive and negative sequence signal, both the positive and negative sequence signals are needed to be separated from the measured signal. The measured signal v_a, v_b and v_c are converted to v_α, v_β and v_0 using equation 2.38. In a balanced system, the v_α, v_β are separated by 90^o which will not be same in unbalanced condition. So the positive and negative sequence components have to be extracted. The positive sequence d-q components are obtained by the equation 2.39 and the negative sequence component of the voltage is obtained by the transformation shown in equation 2.40.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.38}$$

$$\begin{bmatrix} v_d^+ \\ v_q^+ \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{2.39}$$

$$\begin{bmatrix} v_d^- \\ v_q^- \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{2.40}$$

The proposed controller is mainly divided in to two parts, one is positive sequence control and other one is negative sequence control. The positive sequence control does

two functions. The First function is to maintain the DC voltage at the capacitor as constant and second function of this controller is to maintain the positive sequence voltage at point of common coupling to 1 pu. The other part is negative sequence controller, which balances the three phase voltage by reducing the negative sequence components. The reference signal is generated by the sum of all the signals.

2.4.1 Positive Sequence Controller:

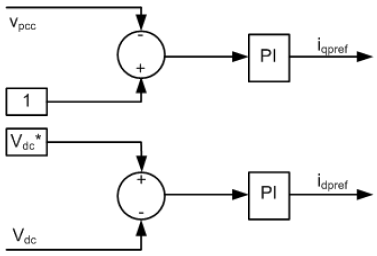


Figure 2.22: Positive sequence Controller

The capacitor is the DC voltage source for the DSTATCOM. The energy stored in the capacitor will drain because of the losses in the DSTATCOM. In order to have proper operation of DSTATCOM, it is required to maintain the DC voltage at the capacitor constant. Figure 2.22 shows the DC voltage regulator. The measured value of DC voltage is subtracted from the reference value of DC link voltage (V_{dc}^{*}). Then it is fed to PI controller to obtain the required amount of active current to maintain DC link voltage, which is given in equation 2.41.

$$i_{dperf} = (k_{pdc} + \frac{k_{idc}}{S})(V_{dc}^{*} - V_{dc}) \tag{2.41}$$

To maintain the PCC voltage constant, DSTATCOM will absorb the reactive power when voltage is more than the reference value and when voltage is less, the DSTATCOM will supply the reactive power. v_q^{+*} represents the reference value of positive sequence PCC voltage and usually set to 1 pu. The actual value is compared with reference value and output is given to PI controller to obtain amount of reactive current requirement as shown in equation 2.42.

$$i_{qdref} = (k_{pac} + \frac{k_{iac}}{S})(v_q^{+*} - v_q^{+}) \tag{2.42}$$

2.4.2 Negative Sequence Controller:

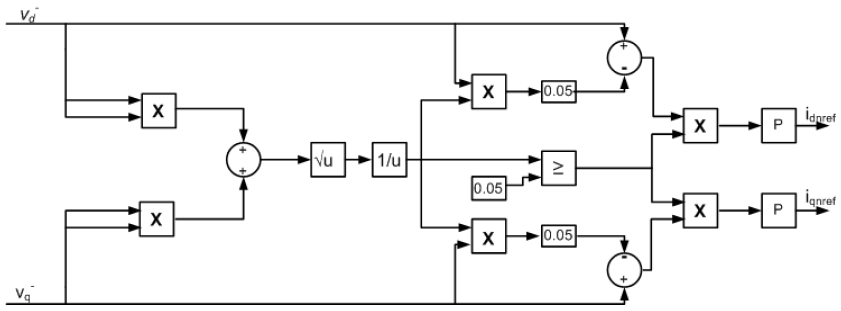


Figure 2.23: Negative sequence Controller

The block diagram of negative sequence reference generator is shown in figure 2.23. To reduce negative sequence voltage, usually the extracted negative sequence components are compared with zero. To generate negative sequence current references, block diagram shown in figure 2.23 is used. According to Osama. A (Almutairi, 2017), the negative sequence controller should activate when negative sequence components exceeds 5% of the nominal voltage. The following equations are formed based on the limit of 5%. In equation 2.43, v_n is the measured value of nominal negative sequence voltage and v_d^- and v_q^- are dq components of negative sequence voltage.

$$v_n = v_d^- + jv_q^- \tag{2.43}$$

$$v_{dref}^- = v_d^- - 0.05\frac{v_d^-}{\mid v_n \mid} \tag{2.44}$$

$$v_{qref}^- = v_q^- - 0.05\frac{v_q^-}{\mid v_n \mid} \tag{2.45}$$

Using equation 2.44 and equation 2.45, the dq components of negative sequence voltage reference is generated. These references are given to proportional controller to obtain current reference i_{dnref} and i_{qnref}. The direction of rotation of positive sequence and negative sequence are opposite. So to make both the components in same direction, the reference currents are multiplied by $e^{-j2\omega t}$ which is shown in the equation 2.46(Almutairi, 2017).

$$i_{dn} + ji_{qn} = (i_{dnref} + ji_{qnref}) * e^{-j2\omega t} \tag{2.46}$$

After multiplication, imaginary and real parts of the equations are written as,

$$i_{dn} = i_{dnref}\cos(2\omega t) + i_{qnref}\sin(2\omega t) \tag{2.47}$$

$$i_{qn} = i_{qnref}\cos(2\omega t) - i_{dnref}\sin(2\omega t) \tag{2.48}$$

The output signals from both positive sequence voltage controller and negative se-

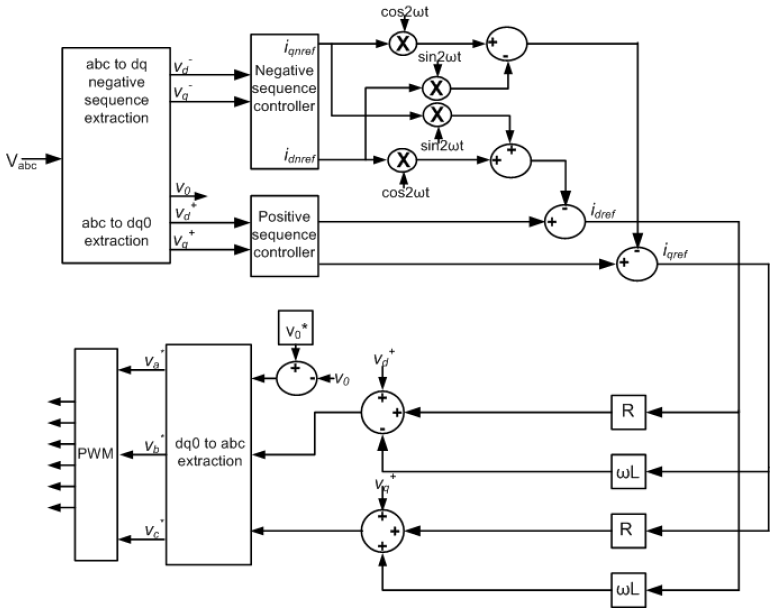


Figure 2.24: .Positive and Negative sequence Controller

quence voltage controller are summed up together and used as i_{dref} and i_{qref} to obtain e_d, e_q and e_0, which is similar to the improved positive sequence controller illustrated in section 2.3. From equation 2.29 and equation 2.30,

$$e_d = R_f i_{dref} - \omega L_f i_{qref} + v_d^+ \tag{2.49}$$

$$e_q = R_f i_{qref} + \omega L_f i_{dref} + v_q^+ \tag{2.50}$$

e_d and e_q are obtained from i_d, i_q, R_f and L_f which is shown in equation 2.49 and equation 2.50. Figure 2.24 shows the improved positive and negative sequence control strategy for DSTATCOM. From figure 2.24 it can be observed that, i_d and i_q are converted into e_d and e_q using filter parameters R_f and L_f. The 0^{th} component is compared with reference value (i.e. v_0^*=0) and this output is taken as e_0 as shown

in the block diagram. The obtained reference values i.e. e_d, e_q and e_0 are converted from dq0 to abc frame using equation 2.37. The obtained reference signals are fed to sinusoidal pulse width modulation block to generate the switching pulses at the desired switching frequency. It can be seen that this control strategy uses only voltage sensors. The control algorithm is simulated for different cases, which is presented in next section.

2.5 Performance Analysis of Improved Positive and Negative Sequence Controller

The analysis of controller is done based on voltage at PCC, negative sequence components and THD perception. The performance of improved positive and negative sequence control strategy is validated for two different cases, they are:
i) Test system
ii) IEEE 9 bus system.

2.5.1 Test System

The analysis of test system with improved positive sequence controller and proposed positive and negative sequence controller is presented in this section. For the analysis, 220V is taken as base value for voltage. The simulation parameters used for the simulation is given in table 2.10.

2.5.1.1 Reduction of Total Harmonic Distortion with Improved Positive and Negative Sequence Controller

Figure 2.25 shows the waveforms of instantaneous voltage at PCC without DSTATCOM, with improved positive sequence controller and improved positive and negative sequence controller. Table 2.11 shows the percentage THD of PCC voltage and source current. The THD spectrum of PCC voltage and source currents are shown in figure 2.26 and figure 2.27 respectively. From the table 2.11 it is observed that, the percentage THD of PCC voltage and source current are minimum in the case of improved positive and negative sequence controller compared to the case of improved

Table 2.10: Parameters of test system used for simulation

Parameters	**Values**	
System Frequency	50Hz	
MS Line Voltage	220V	
Supply line resistance	0.85Ω	
Supply line inductance	2.25mH	
Load	Za	60+j62.73Ω
	Zb	40+j78.5Ω
	Zc	50+j50.24Ω
	Nonlinear load	25Ω , 0.01H
C_{dc}	700μF	
R_f	0.2Ω	
L_f	15mH	

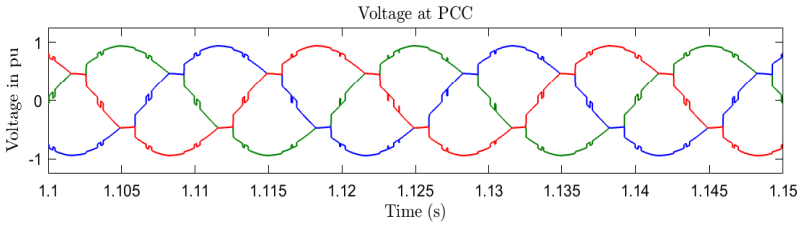
positive sequence controller.

Table 2.11: Percentage THD with positive and negative sequence controlled DSTATCOM in test system

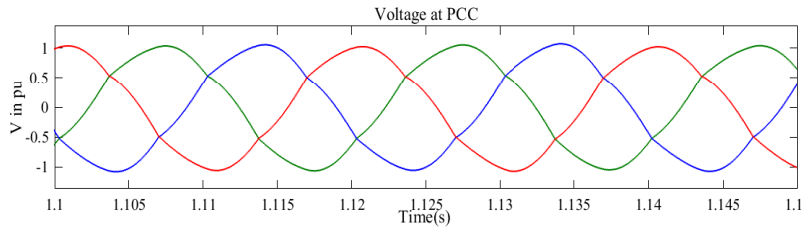
Parameter	**With existing positive sequence controller**	**With improved positive sequence controller**	**With improved positive and negative sequence controller**
% THD of PCC Voltage	7.98	2.224	2.2
% THD of Source Current	17.53	3.819	3.23

2.5.1.2 Comparison of Voltage at PCC with Improved Positive and Negative Sequence Controller

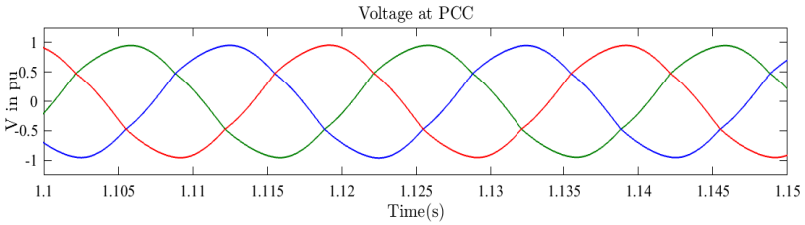
Figure 2.28 shows the RMS voltage at PCC for the two cases i.e. with improved positive sequence controller and with improvised positive and negative sequence controller. As shown in figure, RMS voltage is maintained at 0.96pu with improved positive and negative sequence controller and with improvised positive sequence controller, it is 1 pu. From the table 2.12 it is observed that, based on the RMS voltage perspective the improvised positive sequence controller is found better than the improvised positive and negative sequence controller. However the voltage tolerance is within acceptable limits. Figure 2.29 shows the RMS voltage at PCC, when resistive



(a) Voltage at PCC with DSTATCOM with existing positive sequence controller



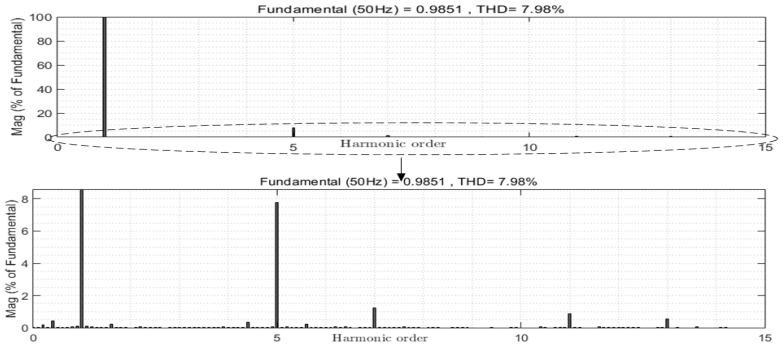
(b) Voltage at PCC with DSTATCOM with improved positive sequence controller



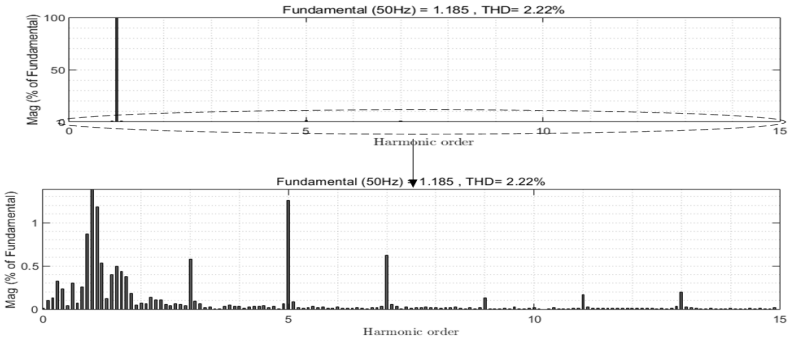
(c) Voltage at PCC with DSTATCOM with improved positive and negativesequence controller

Figure 2.25: Voltage at PCC for different cases

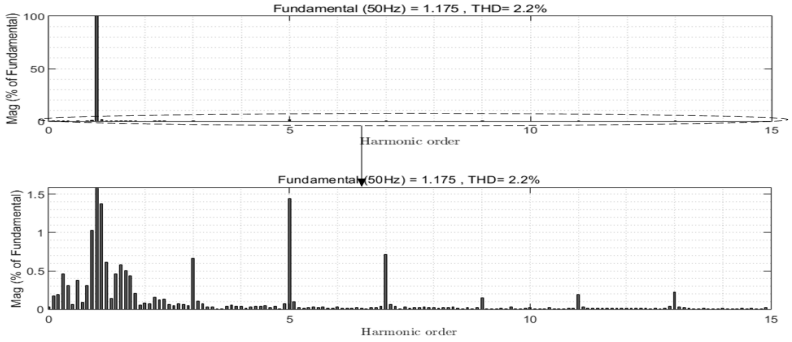
load of 10 ohm is applied for each phase at 2s and removed at 3s. With proposed positive and negative sequence controller the voltage is maintained at 0.96 pu with response time of 2 cycles which is less than response time of proposed positive sequence controller. Figure 2.30 shows the RMS voltage at PCC due to sudden decrease in load. The step change in load is applied from 2s to 3s. With proposed positive and negative sequence controller, the voltage is maintained at constant value of 0.96 pu.



(a) THD spectrum of Voltage at PCC with DSTATCOM with existing positive sequence controller

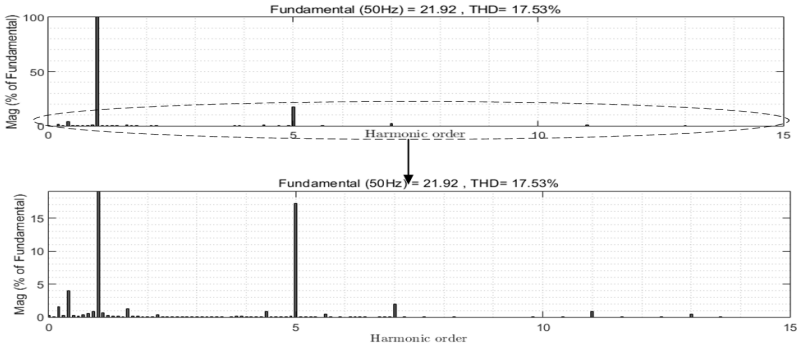


(b) THD spectrum of Voltage at PCC with DSTATCOM with improved positive sequence controller

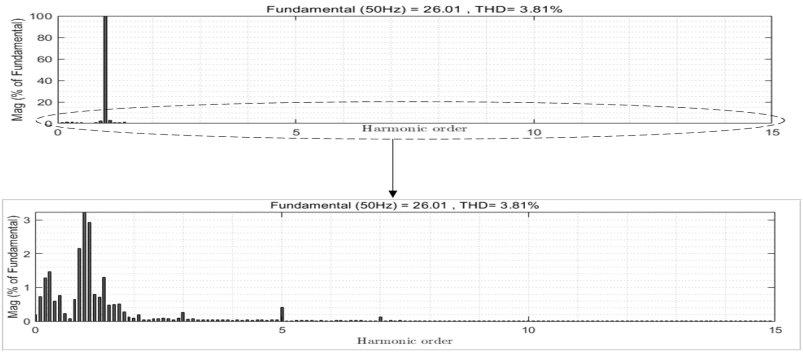


(c) THD spectrum of voltage at PCC with DSTATCOM with improved positive and negative sequence controller

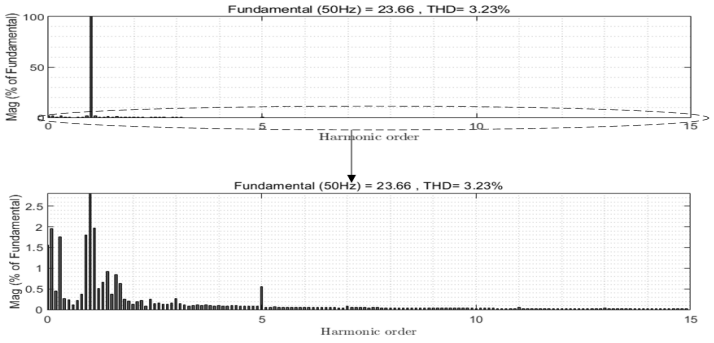
Figure 2.26: THD spectrum of Voltage at PCC for different cases



(a) THD spectrum of current with DSTATCOM with existing positive sequence controller



(b) THD spectrum of current with DSTATCOM with improved positive sequence controller



(c) THD spectrum of current with DSTATCOM with improved positive and negative sequence controller

Figure 2.27: THD spectrum of current for different cases

2.5.1.3 Comparison of Negative Sequence Component with Improved Positive and Negative Sequence Controller

The table 2.13 shows the negative sequence component with improved positive sequence controller and improved positive and negative sequence controller. From ta-

Table 2.12: RMS voltage at PCC with positive and negative sequence controlled DSTATCOM

	RMS Voltage in pu
With existing positive sequence controller	0.95
With improved positive sequence controller	1
With improved positive and negative sequence controller	0.96

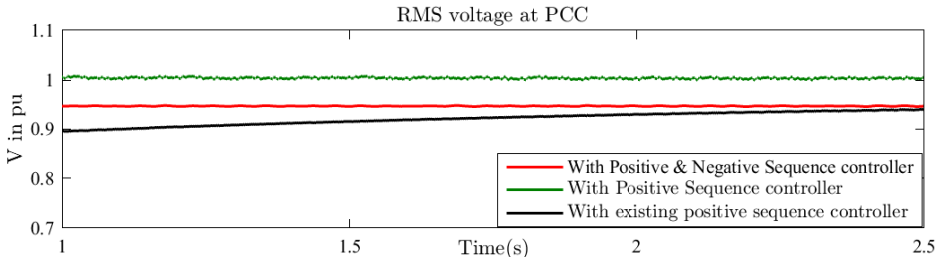


Figure 2.28: RMS voltage at PCC with positive and negative sequence controlled DSTATCOM

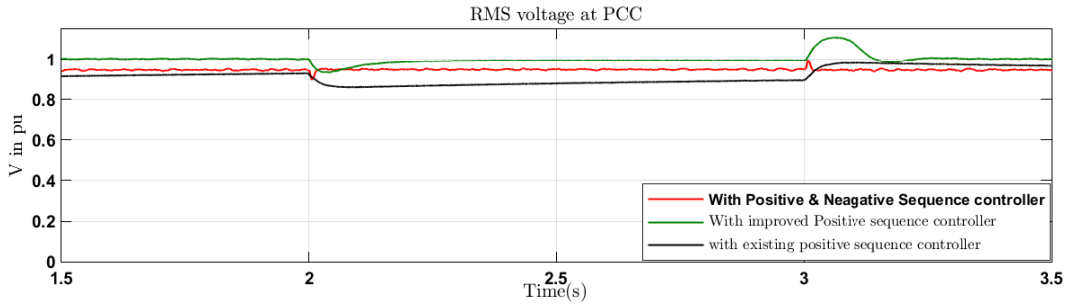


Figure 2.29: RMS voltage at PCC during increase in load

ble it is observed that, the magnitude of positive sequence components is 1 pu in the case of improved positive sequence controller. But the magnitude of negative sequence component is minimum in the case of improved positive and negative sequence controller.

From table 2.14 it is observed that, the performance of improved positive and negative sequence controller is found better than the improved positive sequence controller because THD is reduced and also the voltage at PCC is maintained at

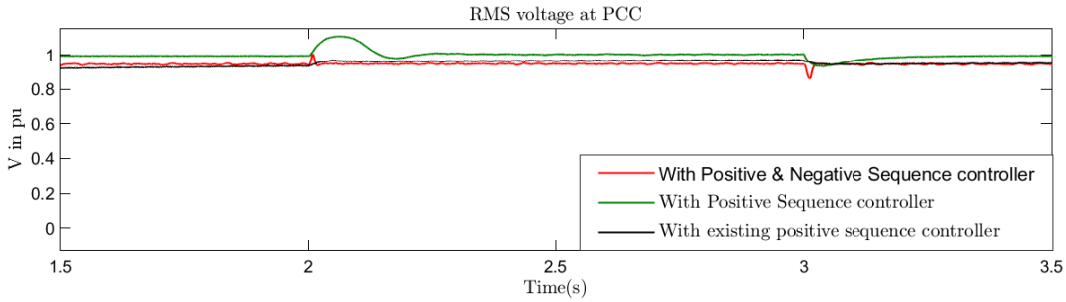


Figure 2.30: RMS voltage at PCC during decrease in load

Table 2.13: Magnitude of positive and negative sequence component with positive and negative sequence controlled DSTATCOM in test system

Parameter	**With existing positive sequence controller**	**With improved positive sequence controller**	**With improved positive and negative sequence controller**
Negative sequence voltage (pu)	0.13	0.13	0.02

Table 2.14: Summary of Results of test system

Parameter	**With existing positive sequence controller**	**With improved positive sequence controller**	**With improved positive and negative sequence controller**
RMS Voltage in pu	0.95	1	0.96
% THD of PCC Voltage	7.98	2.224	2.2
% THD of Source Current	17.53	3.819	3.23
Negative sequence voltage (pu)	0.13	0.13	0.02

acceptable limits. The percentage THD of voltage and current is maintained within the IEEE standard. Also the performance of improved positive and negative sequence controller is better in perception on negative sequence components. The performance analysis of controllers is also investigated with IEEE 9 bus system, which is presented in next section.

2.5.2 IEEE 9 Bus System

2.5.2.1 Reduction of Total Harmonic Distortion with Improved Positive and Negative Sequence Controller

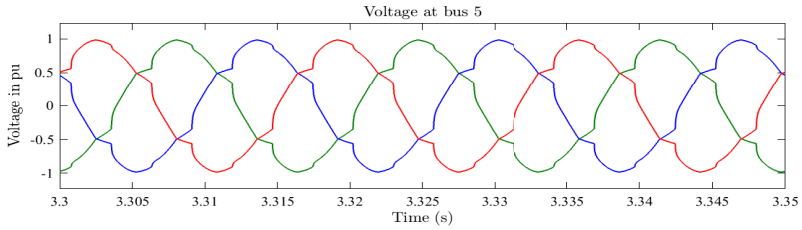
Figure 2.31 shows the waveforms of instantaneous voltage at PCC with improved positive sequence controller and improved positive and negative sequence controller. The THD spectrum of PCC voltage and source currents are shown in the figure 2.32 and figure 2.33 respectively. From the table 2.15 it is observed that, the percentage THD of PCC voltage and current is minimum in the case of improved positive and negative sequence controller compared to the case with improved positive sequence controller.

Table 2.15: Percentage THD with positive and negative sequence controlled DSTATCOM in 9 bus system.

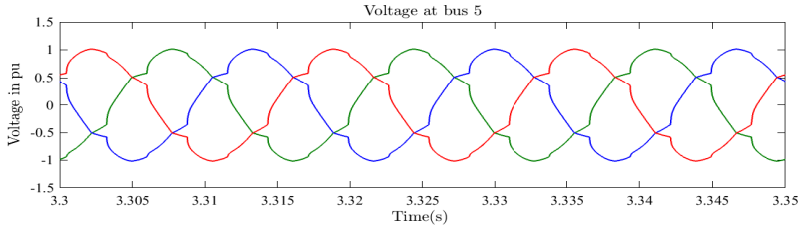
Parameter	**With existing positive sequence controller**	**With improved positive sequence controller**	**With improved positive and negative sequence controller**
% THD of PCC Voltage	8.36	7.8	4.7
% THD of Source Current	1.3	1.3	0.7

2.5.2.2 Comparison of Voltage at PCC with Improved Positive and Negative Sequence Controller

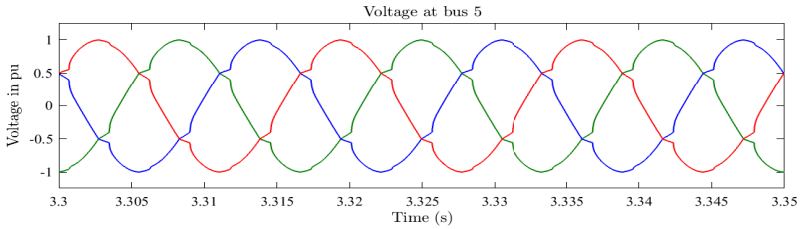
Figure 2.34 shows the RMS voltage in pu at bus number 5 for both the cases. When DSTATCOM is connected with improved positive sequence controller, the voltage at PCC is 0.987 pu. In the case of improved positive and negative sequence controller, the RMS voltage is 0.98 pu. From the table 2.16 it is observed that the performance of improved positive sequence controller and improved positive and negative sequence controller is almost equal in maintaining the RMS voltage at bus 5. Figure 2.35 shows the RMS voltage at PCC, when a load of 4.5 MW is applied at 2s and removed at 2.5s. With proposed positive and negative sequence controller the voltage is maintained at 0.98 pu with response time of 2 cycles which is less compared to positive sequence controller. Figure 2.36 shows the RMS voltage at PCC due to sudden decrease in



(a) Voltage at bus 5 with existing positive sequence controller



(b) Voltage at bus 5 with improved positive sequence controller



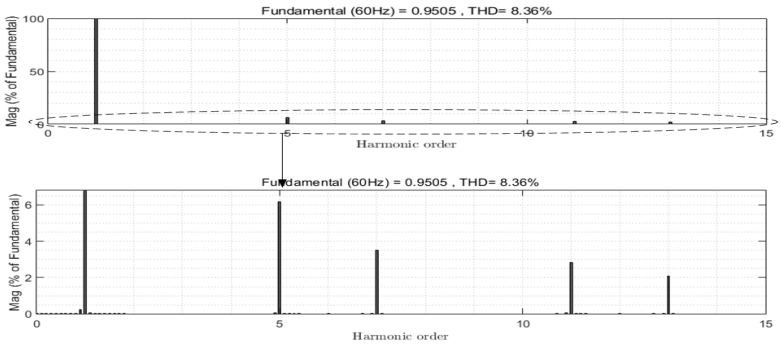
(c) Voltage at bus 5 with improved positive sequence controller

Figure 2.31: Voltage at bus 5 with different scenario

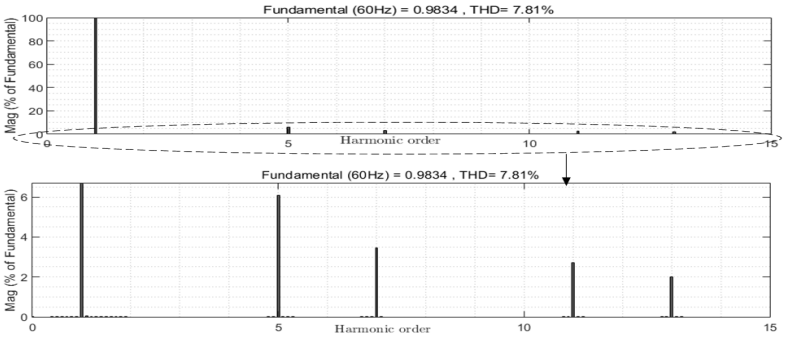
the load. With proposed positive and negative sequence controller the voltage is maintained near to 0.98 pu with lesser response time.

Table 2.16: RMS Voltage at bus 5

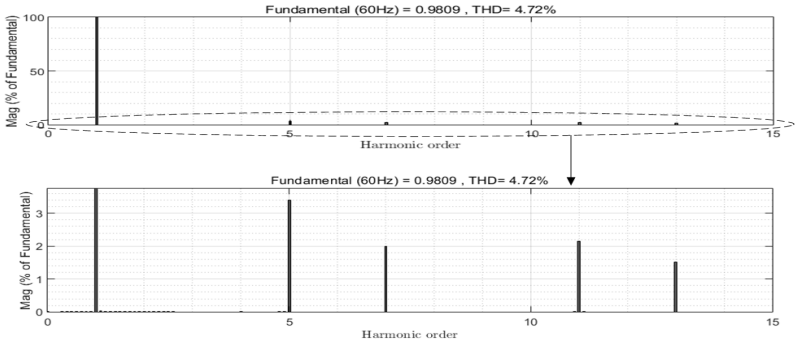
	RMS Voltage in pu
With existing positive sequence controller	0.953
With improved positive sequence controller	0.987
With improved positive and negative sequence controller	0.98



(a) THD spectrum of voltage at bus 5 with existing positive sequence controller



(b) THD spectrum of voltage at bus 5 with improved positive sequence controller

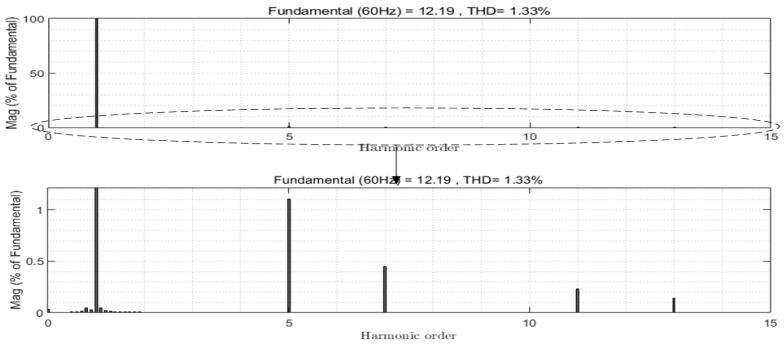


(c) THD spectrum of voltage at bus 5 with improved positive sequence controller

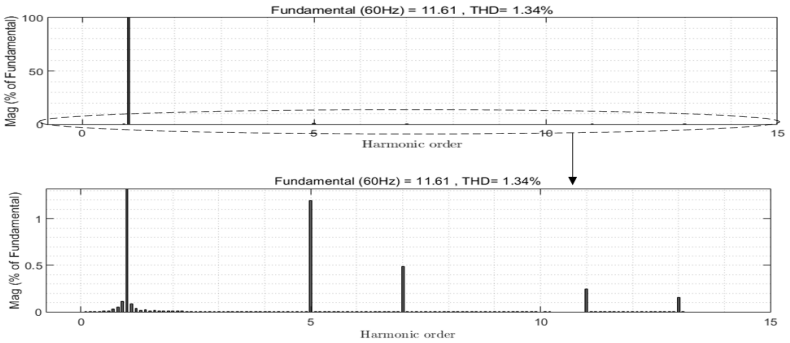
Figure 2.32: THD spectrum of voltage at bus 5 with different scenario

2.5.2.3 Comparison of Negative Sequence Voltage at PCC with Improved Positive and Negative Sequence Controller

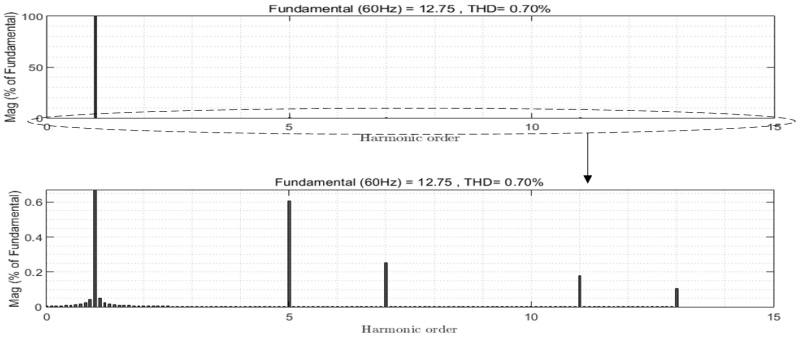
The table 2.17 shows the negative sequence component with improved positive sequence controller and improved positive and negative sequence controller. From the



(a) THD spectrum of current with existing positive sequence controller



(b) THD spectrum of current with improved positive sequence controller



(c) THD spectrum of current with improved positive sequence controller

Figure 2.33: THD spectrum of current with different scenario

table it is observed that, the magnitude of negative sequence component is decreased by 0.03 pu in the case of existing positive sequence controller. From the table 2.18, it is observed that performance of improved positive sequence controller is slightly better only in RMS voltage perception. But in the case of improved positive and

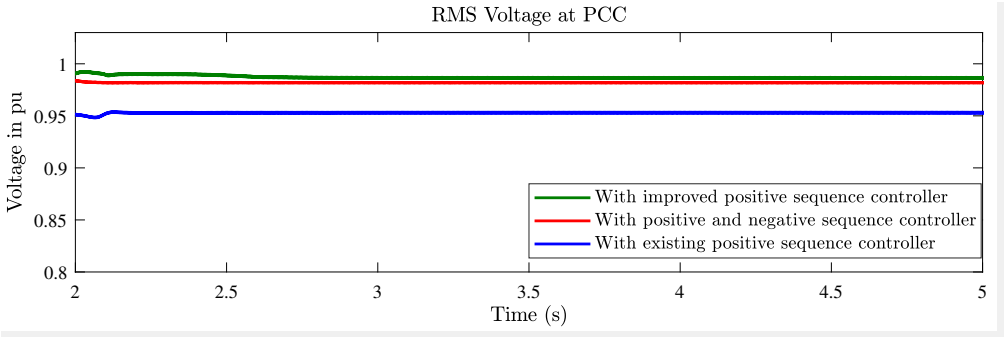


Figure 2.34: RMS voltage at bus 5

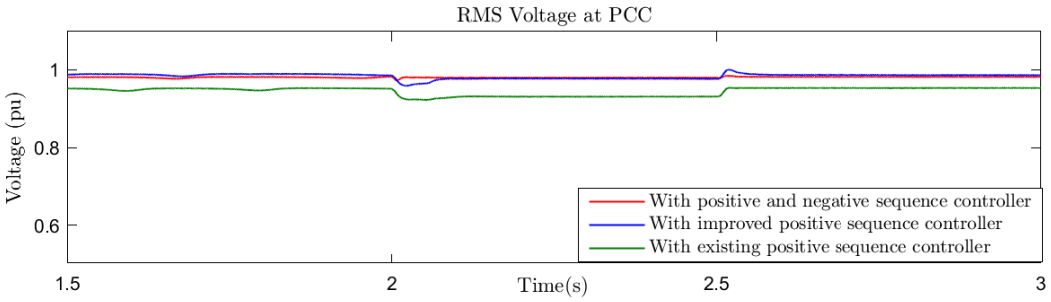


Figure 2.35: RMS voltage at bus 5 during increase in load

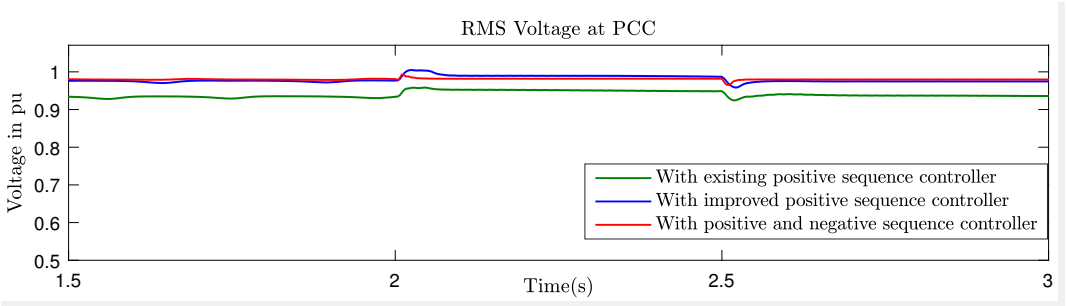


Figure 2.36: RMS voltage at bus 5 during decrease in load

negative sequence controller, performance is better in reduction of THD and negative sequence voltage. Also, the RMS voltage is maintained within the standard limit. From performance analysis with different control scenarios, it is observed that the improved positive sequence controller has better performance in terms of maintaining RMS voltage. But it is also observed that improved positive and negative sequence controller has better performance compared to improved positive sequence controller

Table 2.17: Magnitude of positive and negative sequence component with positive and negative sequence controlled DSTATCOM in IEEE 9 bus system

Parameter	**With existing positive sequence controller**	**With improved positive sequence controller**	**With improved positive and negative sequence controller**
Negative sequence voltage (pu)	0.24	0.24	0.04

Table 2.18: Summary of Results of 9 Bus system

Parameter	**With existing positive sequence controller**	**With improved positive sequence controller**	**With improved positive and negative sequence controller**
RMS Voltage in pu	0.953	0.987	0.98
% THD of PCC Voltage	8.4	7.8	4.7
% THD of Source Current	1.3	1.3	0.7
Negative sequence voltage (pu)	0.24	0.21	0.04

in negative sequence component and percentage THD perception. The improved positive and negative sequence controller is also able to maintain voltage within the standard limit of 0.95 to 1.05 pu.

2.6 Summary

The simulation was carried out by considering two different systems: a) Test system and b) IEEE 9 bus system without DSTATCOM, with existing positive sequence controller, improved positive sequence controller and improved positive and negative sequence controller. The analysis is summarized as below:

- Performance of improved positive sequence controller is found better in RMS voltage perception compared with existing positive sequence controller and improved positive and negative sequence controller which is summarized in ta-

ble 2.19. The figure 2.37 shows the voltage profile in IEEE 9 bus system with different controller.

Table 2.19: Performance in terms of RMS Voltage

	Test system	**IEEE 9 bus system**
Without DSTATCOM	0.84	0.834
With existing positive sequence controller	0.95	0.953
With improved positive sequence controller	1	0.987
With improved positive and negative sequence controller	0.96	0.98

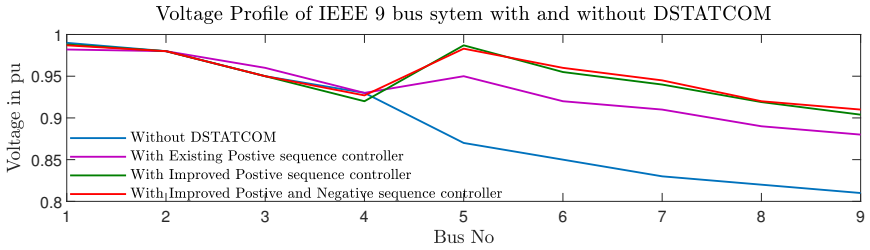


Figure 2.37: Voltage Profile of IEEE 9 bus system with and without DSTATCOM

- The PCC voltage and current THD are reduced using improved positive and negative sequence controller compared with existing positive sequence controller and improved positive sequence controller which is summarized in the table 2.20. In test system, there are only 2 buses. So it is near to the nonlinear load. But in IEEE 9 bus system its little away from PCC. Also the current THD is considered in the analysis is source current. So in perspective of THD, the location of DSTATCOM doesn't matter in small systems.

- In negative sequence voltage perception, it is found that the improved positive and negative sequence controller has better performance compared to existing positive sequence controller and improved positive sequence controller, which is given in table 2.21

Table 2.20: Performance in terms of THD

	Test system		IEEE 9 bus system	
	PCC Voltage THD (%)	Current THD (%)	PCC Voltage THD (%)	Current THD (%)
Without DSTATCOM	8.69	21.26	9.2	12.14
With existing positive sequence controller	7.98	17.53	8.4	1.3
With improved positive sequence controller	2.224	3.819	7.8	1.3
With improved positive and negative sequence controller	2.2	3.23	4.7	0.7

Table 2.21: Performance in terms of negative sequence Voltage

	Test system	**IEEE 9 bus system**
Without DSTATCOM	0.13	0.21
With existing positive sequence controller	0.13	0.24
With improved positive sequence controller	0.13	0.21
With improved positive and negative sequence controller	0.02	0.04

- From the performance analysis it is recommended that, the improved positive and negative sequence controller is better to maintain the voltage and THD within limits.

Chapter 3

Performance Analysis of DSTATCOM under Fault Scenario

In modern power system, the penetration of renewable energy sources has increased since there are no negative impact on environment. According to grid codes, renewable energy sources are not required to contribute to restore the voltage stability. As a result, the reliability and voltage stability of the power grid is negatively affected due to disturbances. The DSTATCOM device will help to enhance the penetration of renewable energy resources to the grid without having a negative impact on the grid reliability and voltage stability (Almutairi, 2017). The DSTATCOM can be used to improve the low voltage ride through behaviour of micro grids in both grid connected and islanded mode (Jayawardena et al., 2015). DSTATCOM is usually used to contribute to the positive sequence component, which does not help to balance the power grid in the event of unbalance fault. The compensation of positive and negative sequences components are required to support voltage restoration as well as the power grid stabilization. The positive and negative sequence controller is used in this work. In this chapter the performance of DSTATCOM in different fault scenario and low voltage ride through capacity of controller are studied.

In this chapter, the existing positive sequence controller and improved positive and negative sequence controllers are analysed under fault scenario. Three unsymmetrical disturbances are considered in the system such as, single line to ground fault, double line fault and double line to ground fault. These faults are applied with and without DSTATCOM for different control strategies such as existing positive sequence controller and proposed improved positive and negative sequence controller. The system

voltage drop is analysed with fault current contribution.
The investigation of performance of control strategy has been conducted on test system which is used in chapter 2. The system and DSTATCOM parameters are given in table 3.1. The simulation setup of DSTATCOM as well as fault location on test system is shown in figure 3.1.

Table 3.1: System parameters

Parameters	**Values**	
System Frequency	50Hz	
MS Line Voltage	220V	
Supply line resistance	0.85Ω	
Supply line inductance	2.25mH	
Load	Za	60+j62.73Ω
	Zb	40+j78.5Ω
	Zc	50+j50.24Ω
	Nonlinear load	25Ω , 0.01H
C_{dc}	700μF	
R_f	0.2Ω	
L_f	15mH	

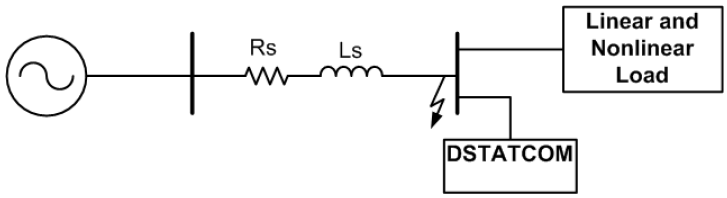


Figure 3.1: Test system with fault

During the evaluation of performance of DSTATCOM, three type of scenarios are considered for all the fault cases. They are:
Case 1: Two bus system without DSTATCOM, which is called "without DSTATCOM".
Case 2: Two bus system with DSTATCOM with existing positive sequence controller.
Case 3: Two bus system with DSTATCOM with improved positive and negative sequence control strategy.

3.1 Scenario 1 : Single Line to Ground Fault

The single line to ground fault is considered at phase 'A' with fault resistance of 1 ohm as shown in the figure 3.2. The fault is considered for the duration of 0.5s. The table 3.2 shows the voltage and current magnitude for different cases.

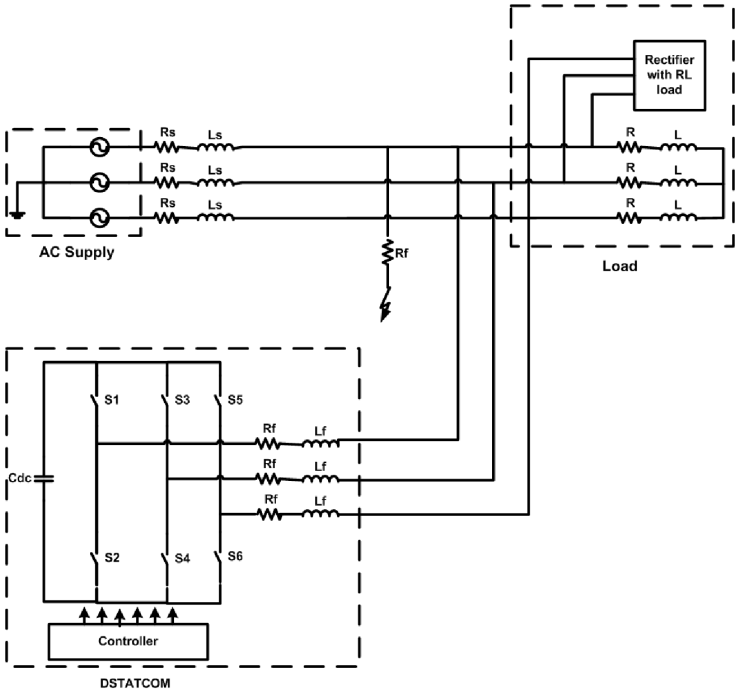


Figure 3.2: Test system with single line to ground fault

3.1.1 Case 1 : Without DSTATCOM

In the absence of DSTATCOM, the voltage drop across each phase and current during the fault is shown in the figure 3.3. From the table 3.2 it is observed that, during SLG fault the voltage at phase A is reduced to 0.43 pu and the fault current is observed as 3.43 pu i.e. source contribution. In this case, the magnitude of positive sequence component is 0.7 pu and magnitude of negative sequence component of the voltage is 0.18 pu during fault as shown in the table 3.3.

3.1.2 Case 2: With Existing Positive Sequence Controller

The voltage and current during fault is shown in the table 3.2. When fault occurs in the system, the DSTATCOM immediately responds and injects capacitive current. Because of this there will be increase in the voltage in other healthy phases which is observed in figure 3.4a. Due to increase in voltage in healthy phase, there is increase in unbalance in magnitude of negative sequence voltage which is observed in the table 3.3.

3.1.3 Case 3: With Improved Positive and Negative Sequence Controller

Figure 3.4 illustrates the voltage at PCC and current during the fault with positive and negative sequence control. From the figure 3.4 and table 3.2, it is observed that voltage in healthy phase is maintained same as the pre fault condition. From the table 3.3, it is also observed that the negative sequence component is reduced to 0.1 pu because this controller tries to increase the voltage in faulty phase also.

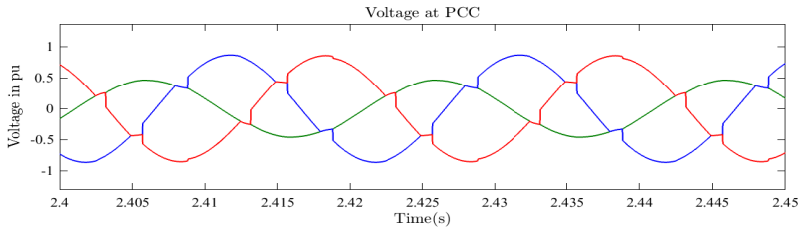
Table 3.2: Voltage and Current Magnitude during SLG fault at Phase A

Scenario	Pre Fault Peak Voltage (pu)			During Fault Peak Voltage (pu)			Fault current in (pu)
	A	B	C	A	B	C	
Without DSTATCOM	0.86	0.86	0.86	0.43	0.86	0.85	3.43
With existing positive sequence controller	0.95	0.95	0.96	0.48	0.99	1.005	3.61
With improved positive and negative sequence controller	0.95	0.95	0.96	0.59	0.95	0.96	3.56

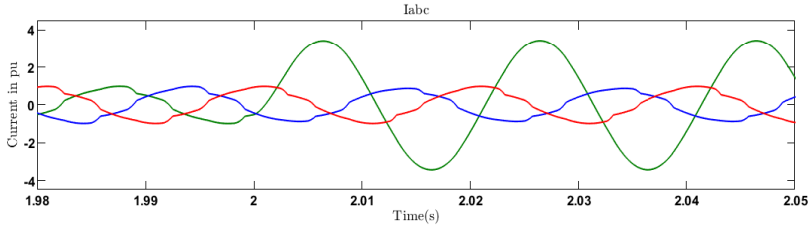
On the basis of evaluation of the performance of DSTATCOM with existing positive sequence controller and proposed positive and negative sequence controller as given in table 3.2 and table 3.3, it can be observed that with existing positive sequence control strategy, the controller tries to increase the voltage in healthy phase and tries to maintain the voltage at PCC. In the case of positive sequence controller, the faulty

Table 3.3: Positive and Negative sequence voltage during SLG fault at Phase A

Scenario	Positive sequence voltage (pu)	Negative sequence voltage (pu)
Without DSTATCOM	0.7	0.18
With existing positive sequence controller	0.84	0.2
With improved positive and negative sequence controller	0.8	0.1



(a) Instantaneous voltage at PCC without DSTATCOM

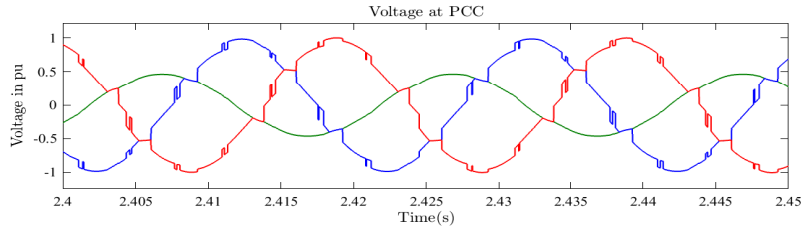


(b) Fault current at PCC without DSTATCOM

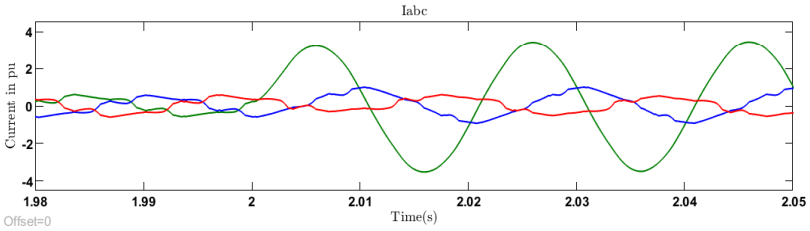
Figure 3.3: Instantaneous voltage at PCC and Fault Current without DSTATCOM during single line to ground fault

phase has the voltage of 0.48 pu. In healthy phase, the voltages are 0.99 and 1.06 pu. In this case the unbalance in the voltage magnitude is further increased and also it created a situation of over voltage in one healthy phase. But in positive and negative sequence controller, the unbalance in the voltage is less compared to the above case and the voltages in the healthy phases are within the limit. In this process, there is increase in negative sequence component, as well as which is a major drawback.

The above mentioned drawback has been overcome with the proposed positive and negative sequence controller wherein the voltage in fault phase increased and also the negative sequence components got reduced.



(a) Instantaneous voltage at PCC with positive sequence controller



(b) Fault current at PCC with positive sequence controller

Figure 3.4: Instantaneous voltage at PCC and Fault current with positive sequence controller with single line to ground fault

3.2 Scenario 2 : Double Line to Ground Fault

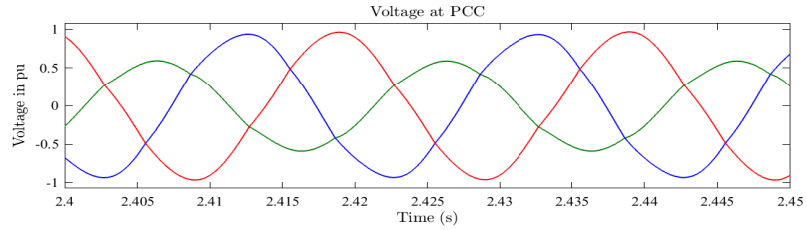
The fault is considered between phase A and phase B with a fault resistance of 1 ohm as shown in the figure 3.6. The duration of fault is 0.5s. Table 3.4 shows the voltage and current magnitudes during the fault.

3.2.1 Case 1: Without DSTATCOM

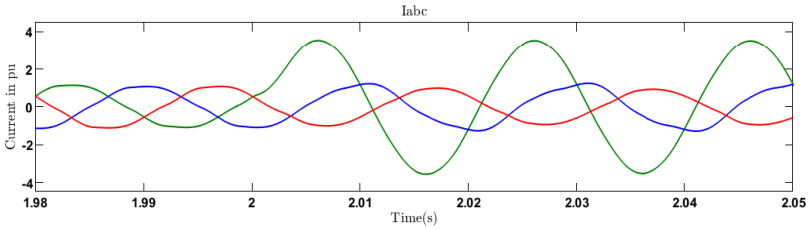
Figure 3.7 illustrates the voltage at PCC and current during DLG fault in the absence of compensation. From table 3.4 it is observed that the voltage at phase A and phase B is reduced to 0.46 pu. The current provided in the table is source current during the fault. The test system is already unbalanced. Hence when DLG faults occurs it worsens the unbalance. The magnitude of positive and negative sequence components are also given in the table 3.5.

3.2.2 Case 2: With Existing Positive Sequence Controller

When DSTATCOM is connected with positive sequence controller, the voltage across PCC and current during fault is shown in the figure 3.8. From the table 3.4 it is



(a) Instantaneous voltage at PCC with Positive and Negative sequence controller



(b) Fault current at PCC with Positive and Negative sequence controller

Figure 3.5: Instantaneous voltage at PCC and Fault Current without DSTATCOM during single line to ground fault

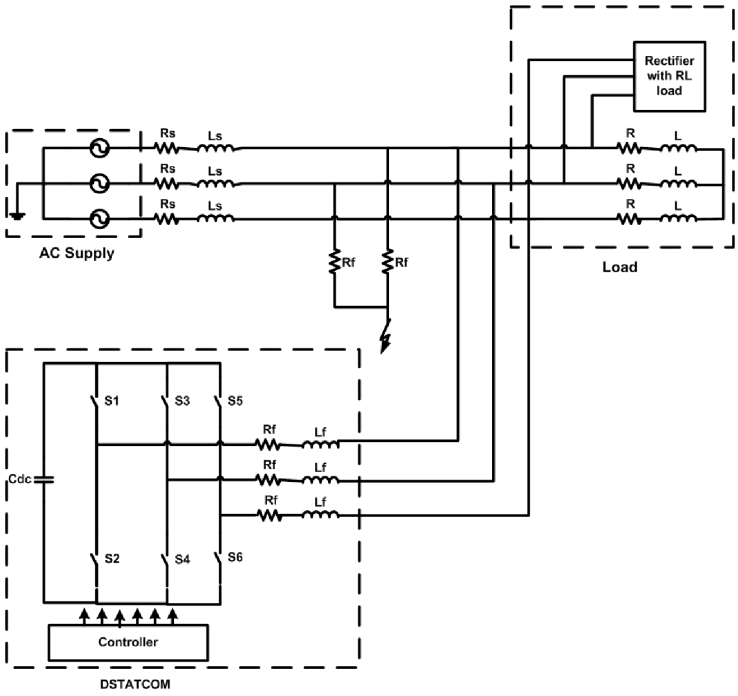


Figure 3.6: Test system with double line to ground fault

observed that, the voltage of healthy phase is increased to 1.002 pu. The magnitude of negative sequence voltage is increased to 0.18 pu which is shown in the table 3.5.

3.2.3 Case 3: With Improved Positive and Negative Sequence Controller

Figure 3.9 illustrates the analysis of performance of DSTATCOM with positive and negative sequence controller. From the table 3.5, it is observed that the magnitude of negative sequence component got reduced compared to the cases with positive sequence controller and without DSTATCOM.

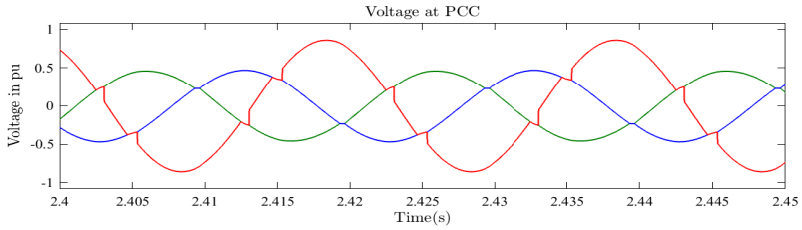
Table 3.4: Voltage and Current Magnitude during DLG fault between Phase A and B

Scenario	Pre Fault Peak Voltage (pu)			During Fault Peak Voltage (pu)			Fault current in (pu)	
	A	B	C	A	B	C	A	B
Without DSTATCOM	0.86	0.86	0.86	0.46	0.46	0.85	3.42	3.5
With existing positive sequence controller	0.95	0.95	0.96	0.52	0.49	1.002	3.88	4.11
With improved positive and negative sequence controller	0.95	0.95	0.96	0.59	0.58	0.96	3.46	3.66

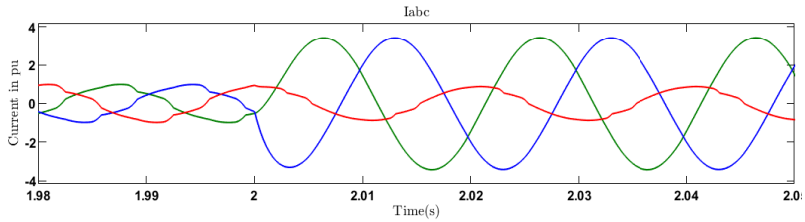
Table 3.5: Positive and Negative sequence voltage during DLG fault between Phase A and B

Scenario	**Positive sequence voltage (pu)**	**Negative sequence voltage (pu)**
Without DSTATCOM	0.58	0.16
With existing positive sequence controller	0.66	0.18
With improved positive and negative sequence controller	0.7	0.12

From table 3.4 and table 3.5 it is observed that during double line to ground fault, the positive sequence controller tries to maintain the RMS value voltage at 1 pu by increasing the voltage in healthy phase. This will increase the negative sequence

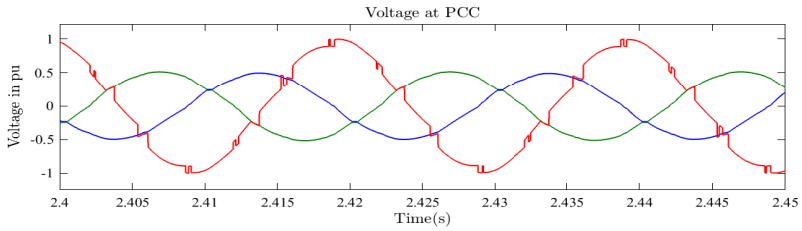


(a) Instantaneous voltage at PCC without DSTATCOM

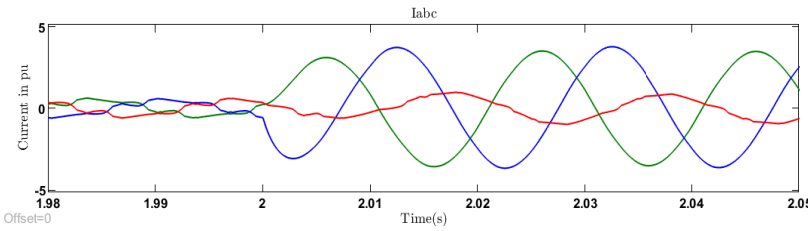


(b) Fault current at PCC without DSTATCOM

Figure 3.7: Instantaneous voltage at PCC and Fault current without DSTATCOM with DLG Fault



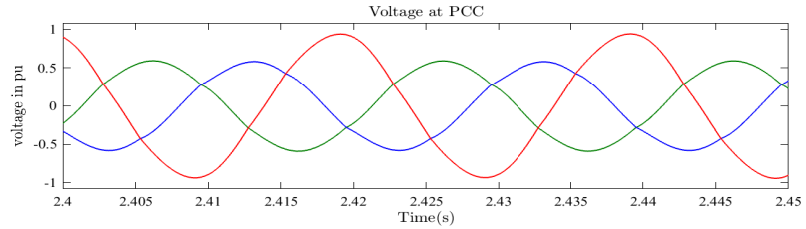
(a) Instantaneous voltage at PCC with positive sequence controller



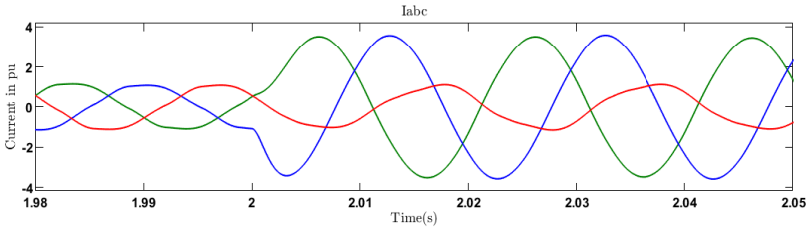
(b) Fault current at PCC with positive sequence controller

Figure 3.8: Instantaneous voltage at PCC and Fault current with positive sequence controller with DLG fault

component. But the performance of negative and positive sequence controller is found better in perception of voltage and negative sequence voltage. In the case of positive sequence controller, the faulty phase has the voltage of 0.52 pu and 0.49 pu. In healthy



(a) Instantaneous voltage at PCC with positive and negative sequence controller



(b) Fault current at PCC with positive and negative sequence controller

Figure 3.9: Instantaneous voltage at PCC and Fault current with positive and negative sequence controller with DLG fault

phase, the voltage is 1.002 pu. In this case the unbalance in the voltage magnitude is further increased. But in positive and negative sequence controller, the unbalance in the voltage is less compared to above case and the voltages in the healthy phases are within the limit and doesn't cause in any over voltage.

3.3 Scenario 3 : Double Line Fault

The fault is considered between phase A and phase B with a fault resistance of 1 ohm as shown in the figure 3.10. The duration of the fault is 0.5s. Table 3.6 shows the voltage and current magnitudes during the fault.

3.3.1 Case 1 : Without DSTATCOM

Figure 3.11 illustrates the voltage at PCC and current during DL fault in the absence of DSTATCOM. From the table 3.6 it is observed that the voltage at phase A is reduced to 0.64 pu and phase B is reduced to 0.46 pu. The magnitude of positive and negative sequence components are also given in the table 3.7.

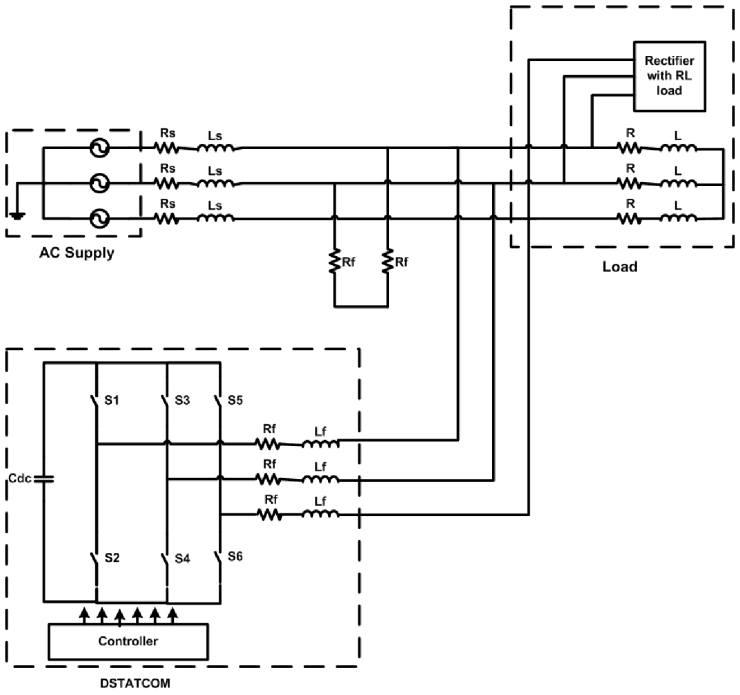


Figure 3.10: Test system with double line fault

3.3.2 Case 2: With Existing Positive Sequence Controller

When DSTATCOM is connected with positive sequence controller, the voltage across PCC and current during fault is shown in the figure 3.12. From the table 3.6 it is observed that, the voltage of healthy phase is increased to 0.99 pu and the magnitude of voltage in phase A and phase B are 0.73 pu and 0.50 pu respectively. The magnitude of negative sequence voltage is increased to 0.26 pu as shown in the table 3.7.

3.3.3 Case 3: With Improved Positive and Negative Sequence Controller

Figure 3.13 illustrates the voltage and current at PCC with positive and negative sequence controller. The voltage during fault is reduced to 0.7 pu and 0.58 pu in faulty phases which is shown in the table 3.6. From the table 3.7 it is observed that the magnitude of negative sequence component got reduced to 0.15 pu compared to the cases with positive sequence controller and without DSTATCOM.

During the double line fault, the presence of unbalance in the system increases

Table 3.6: Voltage and Current Magnitude during double line fault

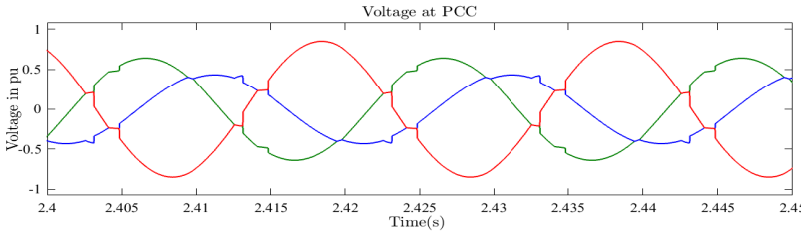
Scenario	Pre Fault Peak Voltage (pu)			During Fault Peak Voltage (pu)			Fault current in (pu)	
	A	B	C	A	B	C	A	B
Without DSTATCOM	0.86	0.86	0.86	0.64	0.46	0.85	3.12	2.92
With existing positive sequence controller	0.95	0.95	0.96	0.73	0.50	0.99	3.4	2.9
With improved positive and negative sequence controller	0.95	0.95	0.96	0.7	0.58	0.93	3.3	2.8

Table 3.7: Positive and Negative sequence voltage during double line fault

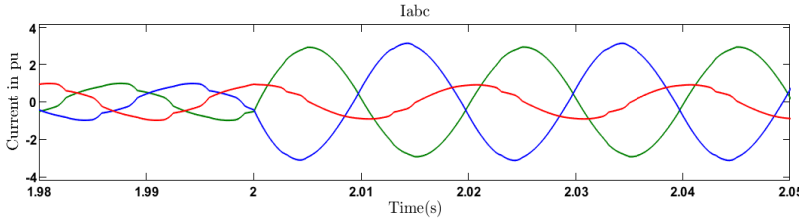
Scenario	**Positive sequence voltage (pu)**	**Negative sequence voltage (pu)**
Without DSTATCOM	0.62	0.23
With existing positive sequence controller	0.71	0.26
With improved positive and negative sequence controller	0.78	0.15

the negative sequence component for existing positive sequence controller. But in the case of proposed positive and negative sequence controller, it is observed that negative sequence component is less compared to other two cases.

Figure 3.14 shows the RMS voltage at PCC during different fault scenarios. From figure 3.14(a) , it is noted that during single line to ground fault, there is an improvement in depth of voltage sag with DSTATCOM. Similarly during double line to ground fault and double line fault, there is an improvement observed in depth of voltage sag with DSTATCOM, which is shown in the figure 3.14(b) and figure 3.14(c). From the figure it is observed that, by connecting DSTATCOM, the low voltage ride through capability of the system is increased. Investigations have been conducted to study the performance of DSTATCOM during different faults and its contribution for the short circuit current during the fault. Table 3.8 summarizes the short circuit current in different control strategies and without DSTATCOM for different faults. The current provided in the table is source current during fault. The test system is

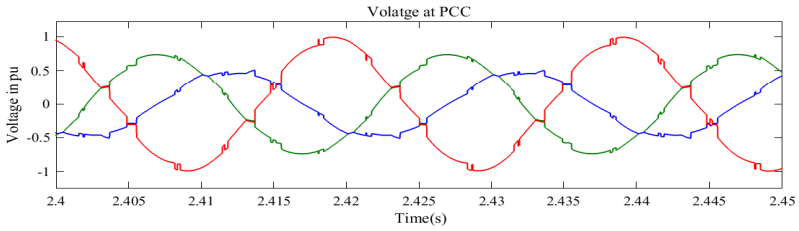


(a) Instantaneous voltage at PCC without DSTATCOM

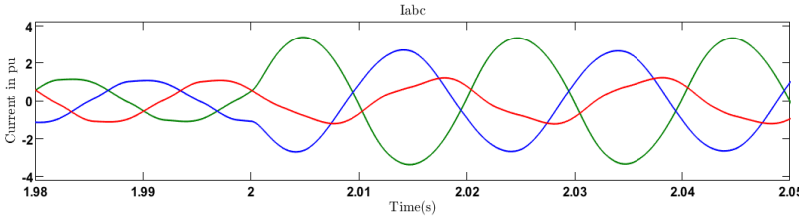


(b) Fault current at PCC without DSTATCOM

Figure 3.11: Instantaneous voltage at PCC and Fault Current without DSTATCOM during double line fault



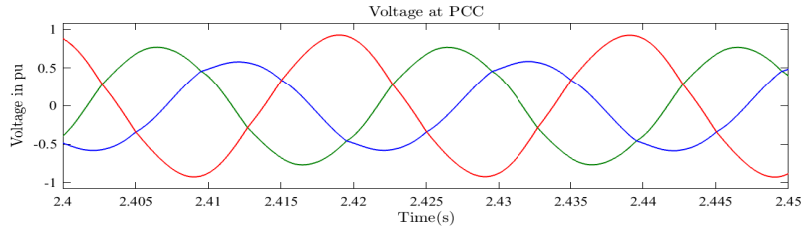
(a)) Instantaneous voltage at PCC with positive sequence controller



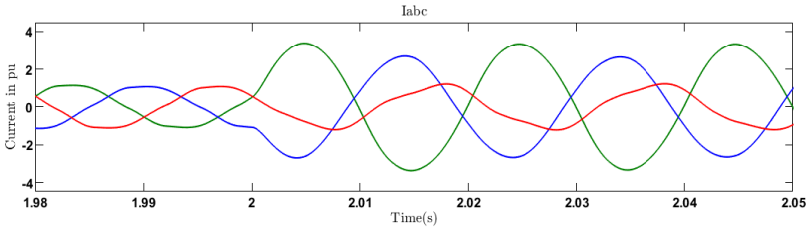
(b) Fault current at PCC with positive sequence controller

Figure 3.12: Instantaneous voltage at PCC and Fault current with positive sequence controller during double line fault

already unbalanced hence when DL and DLG faults occurs it worsens the unbalance in the case of without DSTATCOM condition. During fault condition, the short circuit current in faulted lines always increases with the connection of DSTATCOM.



(a) Instantaneous voltage at PCC with positive and negative sequence controller



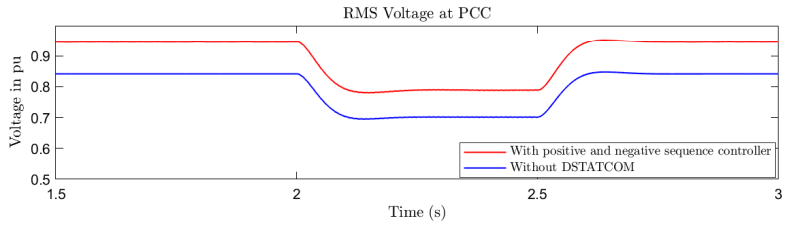
(b) Fault current at PCC with positive and negative sequence controller

Figure 3.13: Instantaneous voltage at PCC and Fault current with positive and negative sequence controller during double line fault

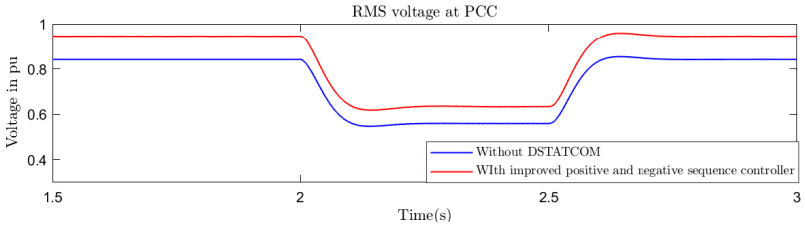
Table 3.8: Fault current in pu

Scenario	SLG Fault			DLG Fault			DL Fault		
	A	B	C	A	B	C	A	B	C
Without DSTATCOM	3.432	-	-	3.42	3.5	-	3.1	2.9	-
With existing positive sequence controller	3.612	-	-	3.88	4.11	-	3.4	2.9	-
With improved positive and negative sequence controller	3.564	-	-	3.46	3.66	-	3.3	2.8	-

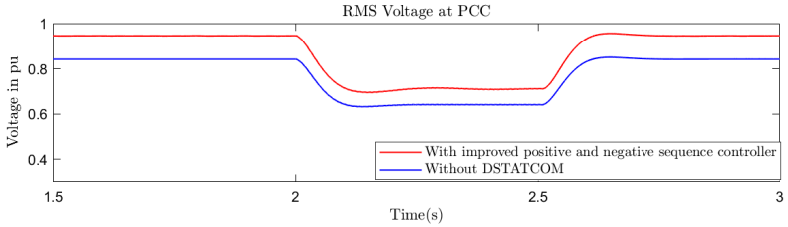
The increase in short circuit current depends on the types of control strategy used and types of fault. The proposed existing positive and negative sequence controller ensures lesser short circuit current than existing positive sequence controller. From table 3.9 it is observed that the total amount of short circuit current contribution from DSTATCOM is depends on the type of control strategy and type of fault. The existing positive sequence controller will increase the voltage in healthy line during



(a) RMS voltage at PCC with single line to ground fault



(b) RMS voltage at PCC with double line to ground fault



(c) RMS voltage at PCC with double line fault

Figure 3.14: RMS voltage at PCC with different fault scenarios

Table 3.9: DSTATCOM current in pu during fault

Scenario	SLG Fault	DLG Fault		DL Fault	
	A	A	B	A	B
With existing positive sequence controller	0.966	1.17	1.44	0.99	0.7
With improved positive and negative sequence controller	0.549	0.56	0.65	0.62	0.34

fault, which may cause over voltage problem in that healthy line. This issue of over voltage is eliminated in the proposed positive and negative sequence controller and also it manages to increase the voltage in the fault lines. This controller also tries to

reduce negative sequence voltage and provides less contribution to the short circuit current when compared to existing positive sequence controller.

3.4 Summary

The simulation was carried out by considering three unsymmetrical faults:
a) Single line to ground fault,
b) Double line to ground fault and
c) Double line fault without DSTATCOM, with existing positive sequence controller and proposed positive and negative sequence controller.

- The table 3.10 summarizes the peak voltage in all the three phases during all three faults. The performance of DSTATCOM with improved positive and negative sequence controller found better in perception of voltage in each phase.

Table 3.10: Performance in terms of Peak voltage (pu) during different faults

Scenario	SLG Fault			DLG Fault			DL Fault		
	A	B	C	A	B	C	A	B	C
Without DSTATCOM	0.43	0.86	0.85	0.46	0.46	0.85	0.64	0.46	0.85
With existing positive sequence controller	0.48	0.99	1.005	0.52	0.49	1.002	0.73	0.50	0.99
With improved positive and negative sequence controller	0.59	0.95	0.96	0.59	0.58	0.96	0.7	0.58	0.93

- From the analysis it is observed that during fault condition, DSTATCOM will contribute to the short circuit current. The contribution to short circuit current in the case of improved positive and negative sequence controller is less compared to the existing positive sequence controller, which is observed in table 3.8.

- From the results, it is observed that low voltage ride through capability of the system can be increased by connecting DSTATCOM.

- From the negative sequence voltage perspective, it is observed that the improved positive and negative sequence controller has better performance compared to existing positive sequence controller, which is given in table 3.11

Table 3.11: Performance in terms of negative sequence Voltage

	SLG fault	**DLG Fault**	**DL Fault**
Without DSTATCOM	0.16	0.16	0.23
With existing positive sequence controller	0.18	0.18	0.26
With improved positive and negative sequence controller	0.12	0.12	0.15

Chapter 4

Optimal Placement and Performance Analysis of DSTATCOM

To get efficient operation, the DSTATCOM should be optimally placed and size should be determined. The primary goal of this work is to lessen the active power loss of the radial distribution system with voltage profile improvement. In this work the main objective is to reduce the power loss by placing DSTATCOM in optimal location. In this section, optimal placement algorithm is discussed. In this work for load flow analysis of distribution system, the backward forward sweep method is used. For getting optimal location and size of DSTATCOM, ant colony method is used.

4.1 Backward – Forward Sweep Method:

Load flow analysis is the most important and essential approach to investigating problems in power system operating and planning. Power flow studies provide a well-organized mathematical procedure for obtaining of different bus voltages and their respective angles, active and reactive power flows through various buses, feeders, generators and loads under steady state form. The steady state nature of the power system is defined based on the tool known as power flow study. Power flow study is mainly utilized by power engineers at the time of planning, implementing and operation of a distribution system. The distribution system has some of the following

special features,

1. Radial or weakly meshed networks
2. High R/X ratios
3. Multi-phase, unbalanced operation
4. Unbalanced distributed load
5. Distributed generation

Due to the above factors, the Newton Raphson and other transmission system algorithms are failed with distribution network. So the backward forward sweeping method is introduced to analyse the distribution network. This method do not need Jacobian matrix unlike NR methods. However, conventional backward forward sweep method is not useful for modern active distribution networks. The Forward-Backward Sweep Method (FBSM) in (Lenhart and Workman, 2007) is easy to program and runs quickly. The method is designed to solve the differential algebraic system generated by the Maximum Principle that characterizes the solution (Wang et al., 1992).

4.1.1 Forward Sweep

In the forward sweep method, calculation of voltages at the buses and voltage drop are involved with permissible current updates. Bus voltages are obtained in a forward sweep starting from the root node in approaching those in the last node. The objective of the forward sweep is to determine the voltages at each node starting from the source node of the feeder. The feeder substation voltage is maintained at its nominal value. During the forward sweep, the active power in each branch is kept constant to the value gained in the backward propagation.

4.1.2 Backward Sweep

In the backward sweep, calculation of current or power flow takes place with permissible voltage updates. Starting from the branches in the last node of the feeder and propagating towards the branches attached to the source node. The active and reactive power flow updates in each branch are obtained in the backward sweep method calculation, by holding the node voltages at their respective values obtained in the

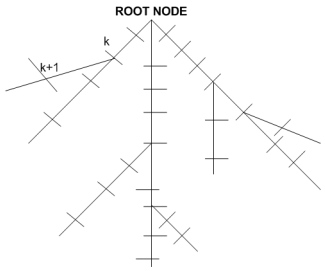


Figure 4.1: Radial Distribution System

previous iteration. It implies that the node voltage values obtained in the forward sweep are held fixed during the backward sweep and the renewed power flows in each branch, are transferred backward along the feeder using the backward sweep method. This emphasis that the backward sweep originates at the extreme end node and propagates towards source node. By comparing the calculated voltages in previous and present iterations, the successive iteration is obtained. The convergence can be achieved if the voltage mismatch is less than the defined threshold i.e., 0.0001. Else new operating power flows in each branch are determined through backward sweep with the already computed voltages and then the method is repeated until the solution is converged. The backward/forward sweep method is now reformulated in a way suitable for the analysis of the convergence of the iterative process. Consider figure 4.1, a branch is connected between the nodes 'k' and 'k+1'. The effective active power P_k and reactive power Q_k that are flowing through branch from node 'k' to node 'k+1'can be calculated backwards from the last node and is given as,

$$P_k = P'_{k+1} + R_k \frac{P'^2_{k+1} + Q'^2_{k+1}}{V^2_{k+1}} \tag{4.1}$$

$$Q_k = Q'_{k+1} + X_k \frac{P'^2_{k+1} + Q'^2_{k+1}}{V^2_{k+1}} \tag{4.2}$$

Where,
$P'_{k+1} = P_{k+1} + P_{Lk+1}$

$Q'_{k+1} = Q_{k+1} + Q_{Lk+1}$

P_{Lk+1} and Q_{Lk+1} are loads that are connected at node 'k+1'. P_{k+1} and Q_{k+1} are the effective real and reactive power flows from node 'k+1'. The voltage magnitude and its respective angles at each node are computed in forward propagation. For instance, consider a voltage $V_k\angle\delta_k$ at node 'k' and $V_{k+1}\angle\delta_{k+1}$ at node 'k+1', then the current passing through the branch having with an impedance, $Z_k = R_k + jX_k$ connected between 'k' and 'k+1'is given as,

$$I_k = \frac{V_k\angle\delta_k - V_{k+1}\angle\delta_{k+1}}{R_k + jX_k} \tag{4.3}$$

The magnitude and the phase angle equations can be used recursively in a forward propagation to determine the voltage and angle respectively of all bus nodes in radial distribution system.

$$V_k\angle\delta_k = V_{k+1}\angle\delta_{k+1} + I_k * R_k + jX_k \tag{4.4}$$

Before performing the load flow, a flat voltage profile of 1.0 pu is assumed at all nodes. The branch active and reactive powers are estimated recursively with the obtained updated voltages at each node. In the stated load flow mode, the summation of power is done in the backward propagation and voltages are computed in the forward walk. Figure 4.2 gives the detailed operation of the power flow calculation using backward forward sweeping algorithm.

4.2 Modelling of DSTATCOM

(Jain et al., 2014) proposed a method, where the total system losses and voltage profile of the system are used as an objective for the optimal location of DSTATCOM and the corresponding optimum size of DSTATCOM is found out by modelling it to maintain the voltage magnitude as 1 pu and to supply the required reactive power for compensation at the node where DSTATCOM is placed. This method is found out to be effective and easy to implement when compared with other methods and the objective of this paper is similar to the objective function of this chapter. For

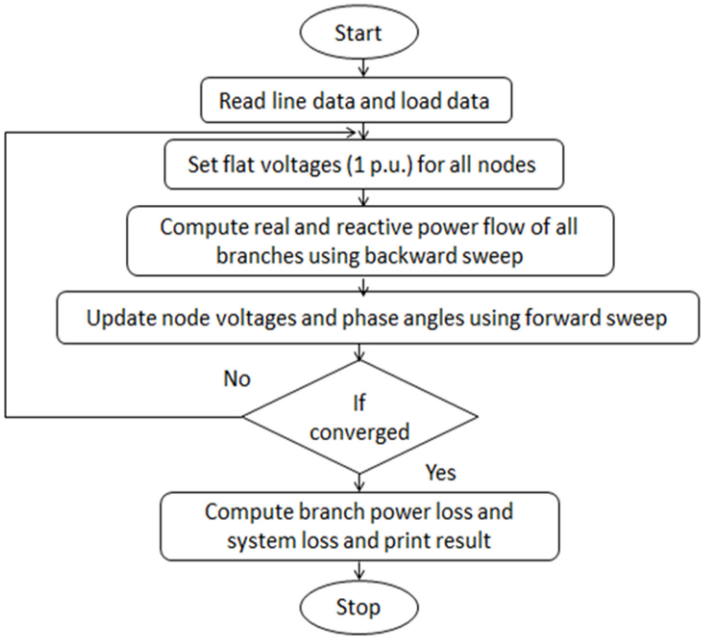


Figure 4.2: Flow chart for backward forward sweep method

steady state modelling of DSTATCOM, (Jain et al., 2014) it is located at the bus as displayed in the figure 4.3. By placing DSTATCOM, the voltage profiles will change at the bus where it is placed and at the adjacent buses. The new voltages are $V_n^{'}$ at the candidate bus and V_m at the previous bus. The current changes to I_m which is summation of I_m and I_{DS} . The DSTATCOM injected current is I_{DS} and is in quadrature with the voltage. Hence the expression for new voltage after connecting DSTATCOM is presented as follows,

$$V_n^{'}\angle\theta_n^{'} = V_m\angle\theta_m - (R_m + jX_m)(I_m\angle\delta) - (R_m + jX_m)(I_{DS}\angle(\frac{\pi}{2} + \theta_n^{'})) \tag{4.5}$$

Here θ_n, θ_m and δ are the phase angles of V_n, V_m, I_m respectively.

By isolating real and imaginary parts of equation 4.5 and manipulation of the equations will lead to:

$$h_1 = real(V_m\angle\theta_m) - real(Z_m I_m\angle\delta) \tag{4.6}$$

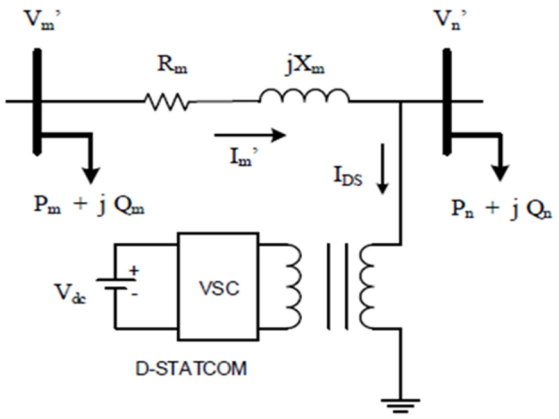


Figure 4.3: 2-bus system with DSTATCOM

$$h_2 = imag(V_m \angle \theta_m) - imag(Z_m I_m \angle \delta) \tag{4.7}$$

$$h_3 = -X_m \tag{4.8}$$

$$h_4 = -R_m \tag{4.9}$$

$$A = (h_1 h_3 - h_2 h_4)^2 + (h_1 h_4 + h_2 h_3)^2 \tag{4.10}$$

$$B = 2(h_1 h_3 - h_2 h_4)(V_n^{'})(h_4) \tag{4.11}$$

$$C = (V_n^{'} R_m)^2 - (h_1 h_4 + h_2 h_3)^2 \tag{4.12}$$

$$D = B^2 - 4AC \tag{4.13}$$

$$x = \frac{-B \pm \sqrt{D}}{2A} \tag{4.14}$$

$$\theta_n^{'} = \sin^{-1} x \tag{4.15}$$

Now the variable x has two values. For deciding the exact value of the root, the terminal conditions are analysed as:
$V_n^{'} = V_n \rightarrow I_{DS} = 0$ and $\theta_n = \theta_n^{'}$
it is found that $x = \frac{-B \pm \sqrt{D}}{2A}$ is the required root of the equation 4.6. Accordingly, the DSTATCOM current phase angle, magnitude and the reactive power introduced to

the system are provided by the equations 4.16, 4.17 and 4.18 respectively.

$$\angle I_{DS} = \frac{\pi}{2} + \theta_n^{'} = \frac{\pi}{2} + \sin^{-1} x \tag{4.16}$$

$$|I_{DS}| = \frac{V_n^{'} cos\theta_n^{'} - h_1}{-h_4 sin\theta_n^{'} - h_3 cos\theta_n^{'}} \tag{4.17}$$

$$jQ_{DS} = (V_n^{'} \angle \theta_n^{'}).(I_{DS}^{'} \angle (\frac{\pi}{2} + \theta_n^{'}))^{\star} \tag{4.18}$$

Where * denotes the complex conjugate. The DSTATCOM is designed such that, the magnitude of the bus voltage where DSTATCOM is placed, is set to 1.0 pu. The DSTATCOM current flow i.e. I_D is determined from equation 4.17. Eventually, the reactive power inserted by DSTATCOM is estimated by equation 4.18.

4.3 Algorithm for Obtaining Rating of DSTATCOM

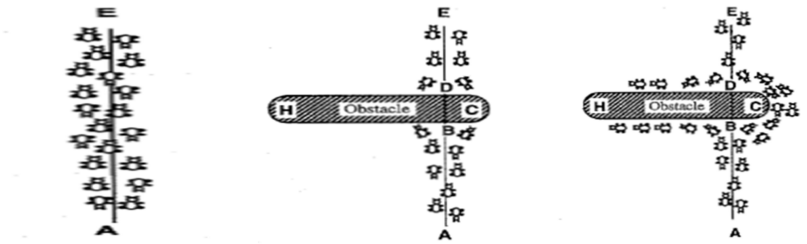
Following is the algorithm for obtaining rating of DSTATCOM (Hussain and Subbaramiah, 2013):
Step 1: Study the bus data, line data of the distribution system and tolerance constraint;
Step 2: Execute the backward forward load flow of the system;
Step 3: Position the DSTATCOM at required bus;
Step 4: The rating of DSTATCOM is acquired by considering voltage at the bus where DSTATCOM is situated as 1.0 pu;
Step 5: Calculate $\angle I_{DS}$ and I_{DS} using equation 4.16 and equation 4.17;
Step 6: Execute the load flow analysis with DSTATCOM and compute voltages;
Step 7: Check for convergence, if ΔV less than the tolerance value, print the results, else proceed to step 5;
Step 8: Compute losses and power flows.

4.4 Ant Colony Optimization

4.4.1 Introduction

Ant algorithms were first proposed by Dorigo and his colleagues (Colorni et al., 1992) as a solution to difficult combinatorial optimization problems like the traveling salesman problem (TSP) and the quadratic assignment problem (QAP). Research on the behaviour of real ants has greatly inspired many research works (Deneubourg et al., 1983, Deneubourg and Goss, 1989). Ant algorithm was motivated by the perception of genuine insect provinces. Ants are social insects (Dorigo et al., 1999) that is, insects reside in colonies and whose action is guided more to the existence of the settlement all in all than to that of a solitary individual segment of the province. An imperative and fascinating behaviour of ant community is their foraging strategy and specifically, how ants can discover briefest ways between food origins and their home while travelling from food sources to the home and the other way around, ants deposit on the ground a substance called pheromone, thus shaping a pheromone trail. Ants can notice pheromone and while picking their direction back home (or to the food source), they have a tendency to pick, in probability, ways set apart by dense pheromone trail. The pheromone trail permits the ants to discover their way back to the home (or to the food source). Likewise, it can be utilised by different ants to discover the area of the food sources. For example consider the experimental setting (Dorigo et al., 1996) shown in figure 4.4. There is a way along which ants are travelling (for case from food source A to the home E, and the other way around, see figure 4.4a). All of a sudden a barrier shows up on the way. So at position B the ants travelling from A to E (or at position D those travelling the other way) need to choose whether to turn right or left (figure 4.4b).The decision is affected by the density of the pheromone trails left by preceding ants. A larger amount of pheromone on the correct way gives an ant a more grounded jolt and in this manner a higher possibility to turn right. The initial ant on reaching point B (or D) has a similar likelihood to turn right or left (as there was no past pheromone trail on both the two ways). Since way BCD is shorter than BHD, the first ant tailing it will strike D before the first ant following the way BHD (figure 4.4c). The outcome is that an ant coming back from E to D will locate a more grounded trail on way DCB, because due to half of all the ants that by chance chosen to approach the barrier through DCBA and by this, as of now arrived ones coming through BCD: they will in this favour way DCB to that of the way DHB. As

a result, the mass of ants following way BCD in a certain period of time will be more than the mass of ants following EHD. This causes the quantity of pheromone trail on the shorter way to becoming quicker than on the long way, and hence the likelihood with which any single ant picks the way to take after is the shorter one without any uncertainty. The last outcome is that rapidly all ants will pick the shorter way.



a b c

Figure 4.4: A case with genuine ants

4.4.2 Ant Colony Optimization

In the ant colony optimization (ACO), a group of synthetic ants collaborate in discovering great answers for troublesome discrete optimization problems. Participation is a key outline segment of ACO algorithms. The algorithms described in the following segments are models inferred from the investigation of natural ant colonies. In this way, this framework is called as Ant System (AS) and the algorithm which is presented here is ant algorithm. Indeed, the ant colony optimization (ACO) to be a building approach for the answer to many complex optimization problems. Hence it is sensible to give unnatural ants a few capacities that their counterpart, the real ants do not possess, only to make them more effective and efficient. Unnatural ants have some capabilities which are not found in their counterpart, i.e. the real ants.

1. Artificial ants reside in an environment where time is discrete.
2. Artificial ants will have some memory.
3. Artificial ants deposit pheromone which is a function of the quality of the solution found.
4. They won't be completely blind.

4.4.3 ACO Procedure

In ACO algorithms a finite size colony of artificial ants searches for good quality solutions to the optimization problem. The merits of the ACO are parallel search and optimization capabilities. This method was inspired by the observation of the behaviours of ant colonies. The ACO used in this work uses artificial ants, which to some extent have memory and are not completely blind, thus can be applied to the network reconfiguration problem and placement of DG or DSTATCOM. The state transition rule, global and local updating rules are introduced to ensure the optimal solution. From the results presented in the literature, it is observed that the convergence property of the ACO method is better than other methods. Each ant builds a solution starting from an initial state selected according to some problem dependent criteria. Ant Colony Optimization procedure is given in the following section,

4.4.3.1 Appropriate Problem Representation

The objective function for the minimization of power loss (Rao et al., 2010) is described as follows:

$Minimize f = min(P_{T,LOSS})$

where: $P_{T,LOSS}$- Total real power loss of the system;

The Power flows in a distribution system are computed by the following set of sim-

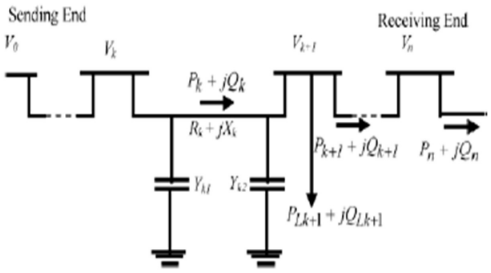


Figure 4.5: Single line diagram

plified recursive equations derived from the single-line diagram shown in figure 4.5.

$$P_{k+1} = P_k - P_{LOSS,k} - P_{Lk+1} \tag{4.19}$$

$$Q_{k+1} = Q_k - Q_{LOSS,k} - Q_{Lk+1} \tag{4.20}$$

where: P_k- Real power flowing out of bus;
Q_k- Reactive power flowing out of bus;
P_{Lk+1}- Real load power at bus k+1;
Q_{Lk+1}- Reactive load power at bus k+1.
The power loss in the line section connecting buses k and k+1 may be computed as

$$P_{LOSS}(k, k+1) = R_k \frac{P_k^2 + Q_k^2}{V_k^2} \tag{4.21}$$

$$Q_{LOSS}(k, k+1) = X_k \frac{P_k^2 + Q_k^2}{V_k^2} \tag{4.22}$$

Where
$P_{LOSS}(k, k+1)$ - Real power Loss in the line section connecting buses k and k+1 ;
$Q_{LOSS}(k, k+1)$- Reactive power Loss in the line section connecting buses k and k+1.
The total active power loss ($P_{T,Loss}$) and reactive power loss ($Q_{T,Loss}$) may then be obtained by losses summation of all the line sections of the feeder, which is given as

$$P_{T,LOSS} = \sum_{k=1}^{n} P_{LOSS}(k, k+1) \tag{4.23}$$

$$Q_{T,LOSS} = \sum_{k=1}^{n} Q_{LOSS}(k, k+1) \tag{4.24}$$

4.4.3.2 Probabilistic Transition Rule

If an ant is put on points of a chart, it sees a few ways to move, so picking next way implies picking the following way that has a probability nature (Su et al., 2005). Let k^{th} ant is located in i^{th} bus. For this situation the likelihood of picking j^{th} bus as a destination at a time t, is obtained by the following equation:

$$P_{i,j}^{k}(t) = \begin{cases} \frac{(\tau_{ij})^{\alpha}(\eta_{ij}^{\beta})}{\sum_{i\epsilon t}(\tau_{ij})^{\alpha}(\eta_{ij}^{\beta})} & \text{,if i,j} \in T \\ 0 & \text{,Otherwise} \end{cases} \tag{4.25}$$

$$\eta_{ij} = \frac{1}{P_{lij}} \tag{4.26}$$

where: α is pheromone decay parameter, β is relative importance of pheromone versus distance, τ_{ij} is pheromone intensity on the (i,j) path. $\eta_{i,j}$ is heuristic value for the (i,j) path. P_{lij} is observed losses between the (i,j) path. where τ is the pheromone, η is the inverse of the loss, T is the total number of buses that are yet to be attended by the ant k located on dot i, (to obtain the converged solution), and β is a parameter which decides the relative significance of pheromone versus loss. In equation 4.25, the pheromone tense is multiplied by the respective heuristic value. Hence by this way, it will support the selection of edges which are shorter and which have a more prominent measure of pheromone. To decide the succeeding bus from probability rates, the Roulette Wheel Algorithm is utilized in the sake of accomplishing likely picking of the way. Algorithm roulette wheel is a strategy to pick one state among numerous particular states in light of the event probable of that state (Colorni et al., 1996).

4.4.4 Global Updating Rule

Memory is required to execute ant algorithm. This memory is acquired by making a matrix with initial pheromone ($\tau_{i,j}(0)$). In ant system, the global updating rule is realized as shown in equation 4.27. When all ants have constructed their visits, pheromone is updated on all edges as per the following equation,

$$\tau_{i,j}(t+1) = (1-\rho) * \tau_{i,j}(t) + \sum_{k=1}^{m} \triangle\tau_{i,j}^{k}(t) \tag{4.27}$$

where $\rho \in (0,1)$ is the pheromone dissipation rate and m is the total number of ants. ρ is the parameter utilized to stay away from boundless gathering of the pheromone trails and empowers the calculation to overlook already done poor choices . $\triangle\tau_{i,j}^{k}(t)$,

is the measure of pheromone ant 'k' sediments on the way; it is characterized as,

$$\triangle\tau_{i,j}^{k}(t) = \begin{cases} \frac{1}{L^{k}(t)} & \text{,if path ij is adopted by ant k} \\ 0 & \text{,else} \end{cases} \tag{4.28}$$

where, $L^{k}(t)$ is the total loss of the k^{th} ant's tour. As per equation 4.28, smaller the insects journey, more pheromone is gotten by ways which are the part of the journey.

4.4.5 ACO Parameters

An experiment on the effectiveness of the ant-cycle algorithm for different combination of α and β parameters has been carried out (Dorigo et al., 1996). The conclusions are summed in figure 4.6, which was generated executing the algorithm ten to twenty times for each combination of parameters and portraying each outcome result to one of the three subsequent various classes.

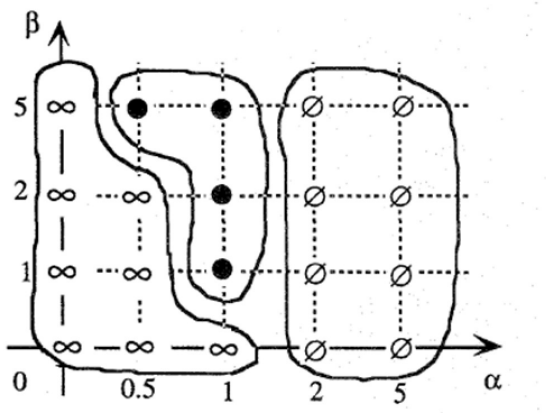


Figure 4.6: Ant-cycle behaviour for different combinations

1. Bad arrangements and stagnation: For high estimations of α, the algorithm enters the stagnation mode without finding desirable outcome rapidly. This condition is addressed to by the image Φ in figure 4.6;

2. Poor outcome and no stagnation: For low estimation of α, the algorithm does

not find the desired outcome. This condition is addressed to by the image ∞ in figure 4.6;

3. Good solutions: For the values of α and β in the central area (represented by the symbol $\circ$) very good solutions are found.

The results obtained in this investigation shows that, a high value of α means that trail is very important and therefore ants tend to choose edges chosen by other ants in the past.

It is noted that by extending the population of ants, the algorithm has demonstrated a more grounded seeking capacity, yet requires more calculation time. It is noted that we get good solution if the population of ant is in the range $30 \leq m \leq 50$. For low estimation of α and β, there is more likely that the ants may pick the ways that had already picked. In the event that the estimation of α and β is too low, i.e., under 0.5, the program may fall into local minima. On the other hand, the estimation of α and β is high, the focalized speed diminishes. In view of the simulation outcomes, it is observed that α and β lie in the scope of 1-5. Additionally, it is observed that, by extending the evaporation rate (ρ), the pheromone dissipates at higher rate and consequently, the global search capacity increases, yet the merged speed of the algorithm diminishes. The global search capacity of the ACO algorithm can be influenced by diminishing the evaporation rate (ρ) parameter. Thus, in light of the simulation outcomes, the result is the best if $0.02 \leq \rho \leq 0.1$.

4.4.6 Algorithm for Finding Optimal Position of DSTATCOM

Flow chart of ACO algorithm is shown in figure 4.7. Following are the steps involved in ACO algorithm,

Step 1: Run base case load flow.

Step 2: Find the optimum size of DSTATCOM for each bus using 4.3.

Step 3: Compute objective function by using Ant Colony algorithm for each bus by placing DSTATCOM of optimum size obtained in step 2 for that bus.

Step 4: Locate the bus at which the objective function value is minimum after DSTATCOM placement. This is the optimum location for placing DSTATCOM.

Step 5: Run the load flow with DSTATCOM and get final result.

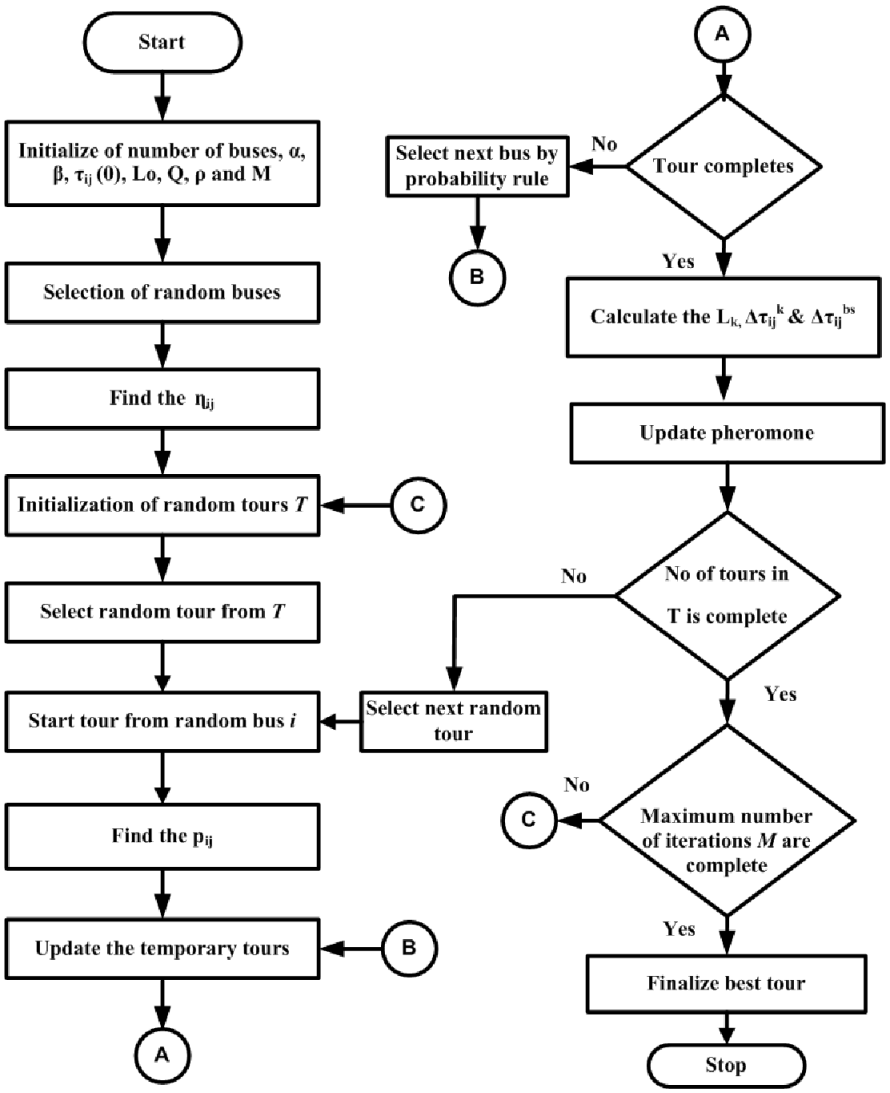


Figure 4.7: Flowchart of ACO algorithm

4.5 Optimal Placement of DSTATCOM

In this work, the ACO algorithm parameters m=40, α= 1, β= 3 and ρ= 0.05 are used. The Backward Forward sweep method is used for power flow analysis and the required DSTATCOM rating is obtained. ACO technique is applied to find the optimal location. To assess the viability and effectiveness of the algorithm, the algorithm has been implemented on two different test systems for the following configurations.

1. The base system without DSTATCOM,
2. The system with one DSTATCOM,
3. The system with two DSTATCOM.

4.5.1 Test System 1 : IEEE 33 Bus System

The ACO algorithm is tested on IEEE 33 bus network. The test system contains 5 tie switches and 32 sectionalizing switches. Figure 4.8 shows the single line diagram of IEEE 33 bus test system. In the network sectionalize switches (normally closed) are numbered from 1 to 32 and tie-switches (normally open) are numbered from 33 to 37. The line and load data of IEEE 33 bus system has given in Appendix-C (Dharageshwari and Nayanatara, 2015). The total active power load is 3.715 MW and reactive power load is 2.300 MVAR. Here, 12.66 kV is taken as base voltage and 10 kVA is taken as base MVA. The reduction in active and reactive power loss after placement of DSTATCOM, improvement in voltage profile at the respective bus and the amount of reactive power injection at the bus is shown in the following section.

For the test system IEEE 33 bus system, the results using MATLAB are listed in table 4.1. It is noted that for the above system without positioning of DSTATCOM, the real and reactive power delivered from grid is 3.9176 MW and 2.4351 MVAR respectively, with total real power loss of 0.2026 MW and the lowest voltage of 0.9131 pu is found at the bus number 18. From ACO algorithm presented in above section, it is found that, best location to place single DSTATCOM with minimum power loss is 28^{th} bus with rating of 1.988 MVAR. With the positioning of DSTATCOM at the bus number 28 it is found that the real power loss got reduced by 21.23% i.e. from 0.2026 MW to 0.1594 MW. The voltage profile got improved to 0.9321 pu. The active power supplied from the grid got reduced from 3.9176 to 3.8744 MW. In the case of placement of two DSTATCOM, obtained optimal locations are 26 and 32 with size of

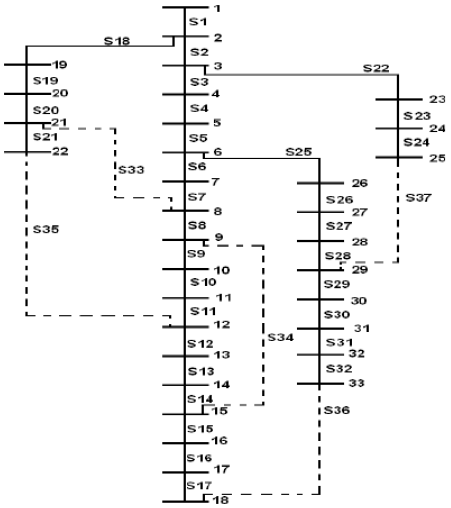


Figure 4.8: IEEE 33 bus system

1.058 MVAR and 0.620 MVAR. After positioning two DSTATCOMs at bus number 26 and 32, it is observed that, there is a further reduction in real power loss when compared to placement of one DSTATCOM by 11.73% from 0.1594 to 0.1407 MW as presented in the table 4.1. The voltage at 18^{th} bus is 0.9296 pu. The grid active power got reduced to 99.51% and to 99.52% compared to single DSTATCOM.

Table 4.1: IEEE 33 bus system using MATLAB software

Description	**Without DSTATCOM**	**With DSTATCOM**	
		one	two
Optical location of DSTATCOM	-	28	26,32
Optimal size of DSTATCOM in MVAR	-	1.988	1.058,0.620
Total active power in MW	3.9176	3.8744	3.8557
Total reactive power in MVAR	2.4351	0.421	0.7164
Minimum Voltage in pu (at 18^{th} bus)	0.9131	0.9321	0.9296
Total Real power loss in MW	0.2026	0.1594	0.1407
Total Reactive power loss in MVAR	0.1351	0.109	0.0944

4.5.2 Test System 2 : 207 Bus Practical Distribution System:

The second test system is a practical radial distribution network from the G Madegowda Institute of Technology (GMIT), Karnataka, India. Figure 4.9 shows the

single line diagram of GMIT 207 bus distribution network in MI power software environment. It consists of 11 kV system with 207 buses and 99 transformers. The loads are obtained by considering the rating of transformer. The active power loads are obtained by multiplying the rating of transformer by the power factor of 0.85. The total system active power load is 5.6856 MW and total reactive power load is 3.5231 MVAR. The power flow calculation is performed based on S_{base}=1 MVA and V_{base}=11 kV. GMIT 207 bus system is executed in MATLAB and the results are tabulated in the table 4.2. From the table 4.2, for the above system without positioning of DSTATCOM the real and reactive power generation is 6.4942 MW and 3.8563 MVAR respectively, with total real power loss of 0.8086 MW and the low voltage profile is 0.8147 pu at the bus number 207. The optimal location of DSTATCOM is 194^{th} bus, which is obtained by the ACO algorithm which is presented previous section. The corresponding rating of DSTATCOM is 1.909 MVAR. With DSTATCOM at the bus number 194, it is found that the real power loss got reduced by 23.32% that is from 0.8086 to 0.62 MW. The voltage profile got improved to 0.8639 pu. The generated active power got reduced to 97.09% and to 96.97%.

From ACO algorithm, it is found that bus number 111 and 197 are the optimal location to place two DSTATCOM with rating of 1.207 MVAR and 0.9505 MVAR. After placement of two DSTATCOM at bus number 197 and 111, it is observed that there is a further reduction in real power loss by 8.83% that is from 0.62 to 0.5652 MW as presented in the table 4.2. The voltage profile at 207^{th} bus is 0.8608 pu. From the results it is observed that, for small system, by usage of multiple DSTATCOM have only marginal benefits and so it is better to go for single DSTATCOM in terms of cost perspective. But for larger system, the usage of multiple DSTATCOM placement will be beneficial.

The results are associated with both the systems under consideration and the accompanying observations have been acquired.

1. For the positioning of single DSTATCOM the voltage profile is improved and the active power loss got reduced.

2. For the location of two DSTATCOM, there is a significant reduction in active power loss and also voltage profile is improved when compared to the base case without DSTATCOM.

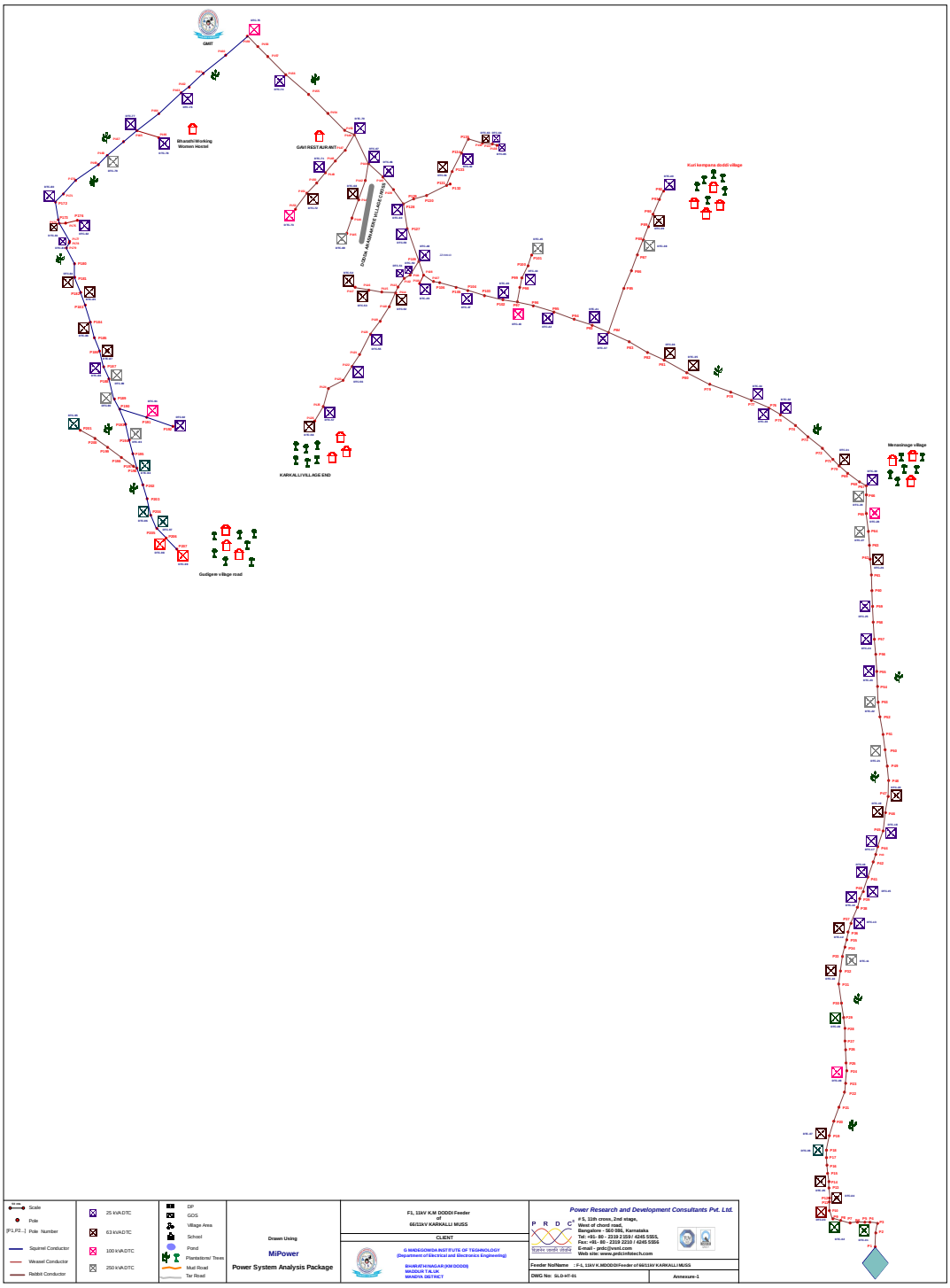


Figure 4.9: The single line diagram of GMIT 207 bus distribution network

Table 4.2: 207 bus system using MATLAB software

Description	Without DSTATCOM	With DSTATCOM	
		one	two
Optical location of DSTATCOM	-	194	111,197
Optimal size of DSTATCOM in MVAR	-	1.9093	1.2701,0.9505
Total active power in MW	6.4942	6.3056	6.2508
Total reactive power in MVAR	3.8563	1.8306	1.4954
Minimum Voltage in pu (at 207^{th} bus)	0.8147	0.8639	0.8608
Total Real power loss in MW	0.8086	0.6200	0.5652
Total Reactive power loss in MVAR	0.3332	0.2168	0.1929

4.5.3 Results Comparison

The following table shows the comparative investigation of the proposed strategy after establishment of DSTATCOM on an IEEE 33 bus system with single DSTATCOM From the table 4.3, it is clear that the ACO method has less active, reactive power

Table 4.3: Comparison of different algorithms on 33 system

Description	Base system	Immune algorithm	Stability Index method	ACO method
DSTATCOM size and location in (MVAR)		0.962(12)	1.993(30)	1.988(29)
Active power loss in MW	0.2026	0.171	0.169	0.1594
Reactive power loss in MVAR	0.1351	0.115	0.118	0.109
Minimum voltage in pu	0.9131(18)	0.9258(18)	0.923(18)	0.9321(18)

losses and good improvement in voltage profile when compared with other methods.

4.6 Performance Analysis of Improved Positive and Negative Sequence Controller

In this section, location and size obtained by above algorithm is used to place the DSTATCOM with improved positive and negative sequence controller and performance of controller for different cases have been analysed. IEEE 33 bus system and

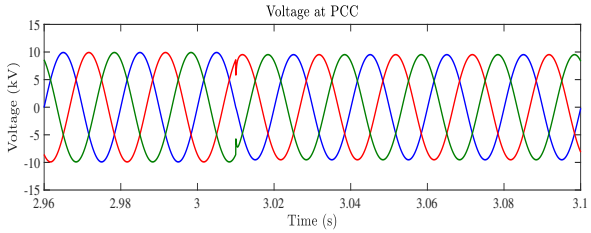
GMIT 207 bus systems are simulated in PSCAD software for performance analysis.

4.6.1 IEEE 33 Bus System:

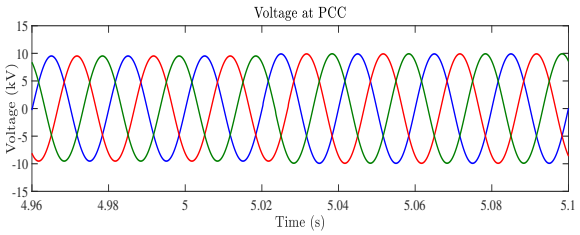
The IEEE 33 bus system is simulated in PSCAD with optimally placed DSTATCOM and the performance of controller used is analysed for different operating condition.

4.6.1.1 Case 1- Sag Without DSTATCOM

In this case, the IEEE 33 bus system without DSTATCOM is simulated. A line to ground fault is applied at 3s to create the voltage sag in the system, later it is cleared at 5s. The figure 4.10 shows the phase voltage waveform at 28^{th} bus of system. figure 4.11 and figure 4.12 shows the RMS value of voltage at different bus. At PCC, the RMS value of voltage during sag is 0.92 pu.



(a) Voltage waveform at PCC without DSTATCOM during starting of sag



(b) Voltage waveform at PCC without DSTATCOM during end of sag

Figure 4.10: Voltage waveform at PCC without DSTATCOM during sag

4.6.1.2 Case 2- Sag With DSTATCOM

In this case the IEEE 33 bus system with DSTATCOM is simulated. The DSTATCOM is placed at 28^{th} bus in the system; this location is obtained by using above

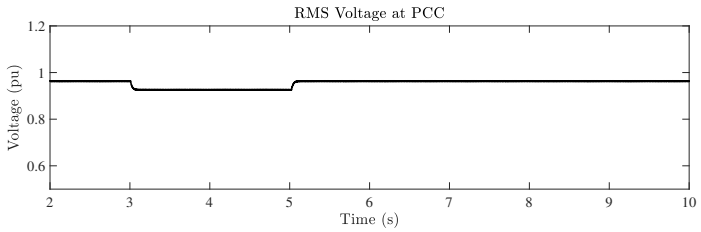


Figure 4.11: Voltage (RMS) at PCC without DSTATCOM with voltage sag in 33 bus system

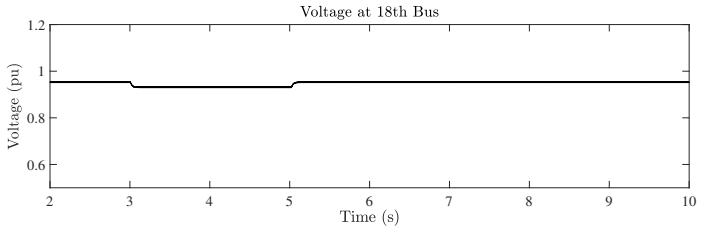


Figure 4.12: Voltage (RMS) at 18^{th} bus without DSTATCOM

ACO algorithm. In this case also, sag is created at 3s and it is cleared at 5s. Before sag occurs, the DSTATCOM tries to maintain the voltage at 1 pu at 28^{th} bus and when sag occurs, the DSTATCOM tries to overcome the sag and maintains the voltage near to 1 pu and during sag, voltage is 0.97 pu, which is shown in figure 4.13. Figure 4.14 shows the phase voltage waveform at 28^{th} bus. Figure 4.15 shows the reactive power absorbed by the DSTATCOM. During sag, the reactive power supplied by DSTATCOM is increased. The RMS value of voltage at 18^{th} bus is shown in figure 4.16.

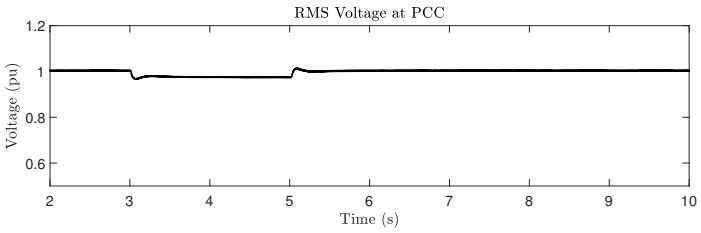
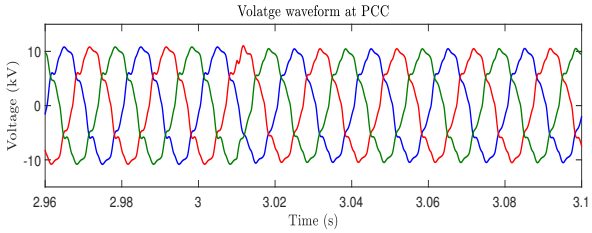
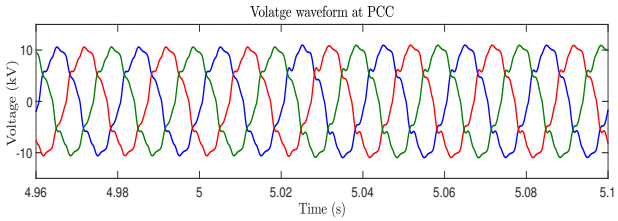


Figure 4.13: Voltage (RMS) at PCC with DSTATCOM with voltage sag in 33 bus system



(a) Voltage waveform at PCC with DSTATCOM at the starting of sag



(b) Voltage waveform at PCC with DSTATCOM at the end of sag

Figure 4.14: Voltage waveform at PCC with DSTATCOM

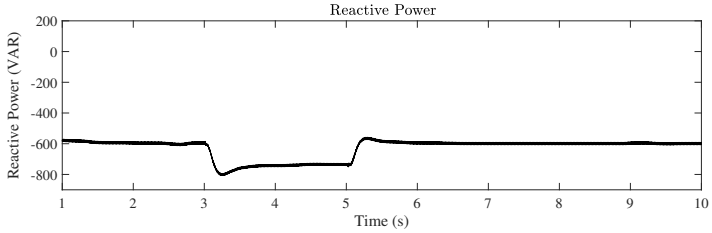


Figure 4.15: Reactive Power absorbed by DSTATCOM

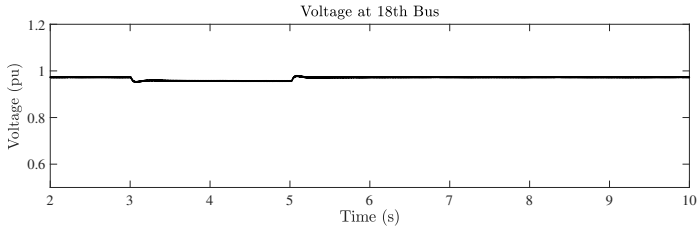


Figure 4.16: Voltage (RMS) at 18^{th} bus with DSTATCOM

4.6.1.3 Case 3- Swell Without DSTATCOM

In this case the IEEE 33 bus system without DSTATCOM is simulated. At 3s, a voltage swell is created which is shown in figure 4.17 and the RMS value of voltage

at PCC is 1.05 pu. The figure 4.18 shows the three phase voltage waveform at 28^{th} bus of system. Figure 4.19 shows the RMS value of voltage at 18^{th} bus.

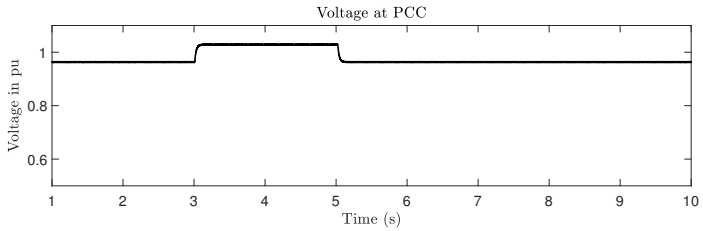
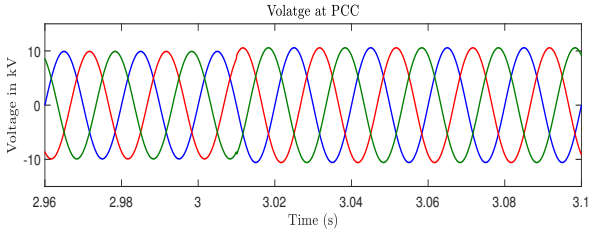
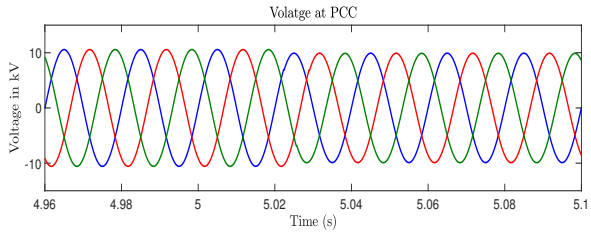


Figure 4.17: Voltage (RMS) at PCC without DSTATCOM with voltage swell in 33 bus system



(a) Voltage waveform at PCC without DSTATCOM at the starting of swell



(b) Voltage waveform at PCC without DSTATCOM at the end of swell

Figure 4.18: Voltage waveform at PCC without DSTATCOM with swell

4.6.1.4 Case 4- Swell With DSTATCOM

In this case the IEEE 33 bus system with DSTATCOM is simulated. The DSTATCOM is placed at 28^{th} bus in the system; this location is obtained by using above ACO algorithm. Before voltage swell, the DSTATCOM tries to maintain the voltage at 1 pu at 28^{th} bus. During the swell, the DSTATCOM tries to maintain the voltage

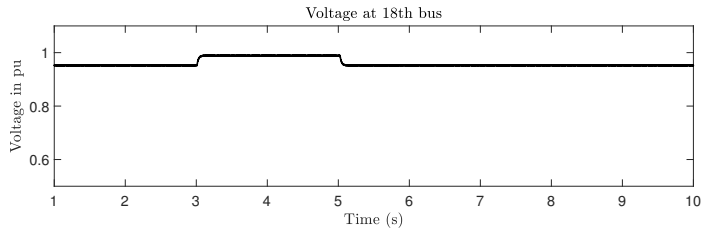


Figure 4.19: Voltage (RMS) at 18^{th} bus without DSTATCOM

near to 1 pu, which is shown in figure 4.20. Figure 4.21 shows the phase voltage waveform at 28^{th} bus. The reactive power absorbed by DSTATCOM is shown in figure 4.22. The RMS value of voltage at 18^{th} bus is shown in figure 4.23.

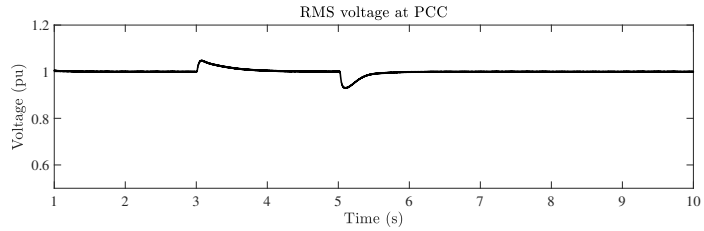


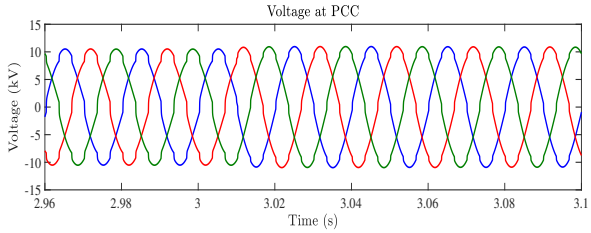
Figure 4.20: Voltage (RMS) at PCC with DSTATCOM with voltage swell in 33 bus system

4.6.2 GMIT 207 Bus System:

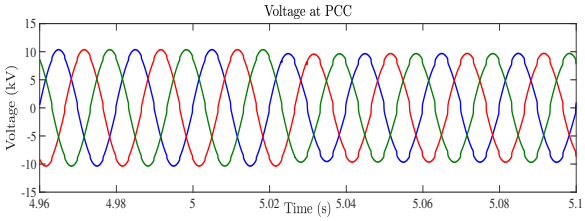
The GMIT 207 bus system is simulated in PSCAD with optimally placed DSTATCOM and the performance of proposed controller used is analysed for different operating condition.

4.6.2.1 Case 1- Sag Without DSTATCOM

In this case, the 207 bus system without DSTATCOM is simulated. A line to ground fault is applied at 2s to create the voltage sag in the system, later it is cleared at 2.5s. The figure 4.24 shows the phase voltage waveform at 194^{th} bus of system. Figure 4.25 and figure 4.26 shows the RMS value of voltage at different bus. At PCC, the RMS value of voltage during sag is 0.90 pu



(a) Voltage waveform at PCC with DSTATCOM at the starting of swell



(b) Voltage waveform at PCC with DSTATCOM at the end of swell

Figure 4.21: Voltage waveform at PCC with DSTATCOM during swell

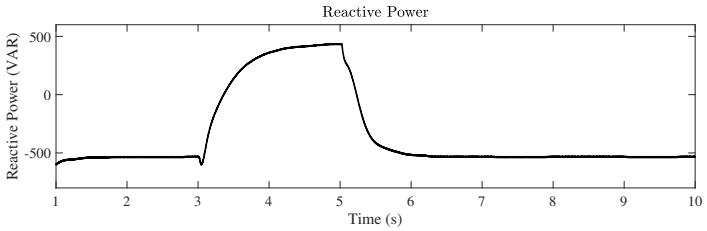


Figure 4.22: Reactive Power absorbed by DSTATCOM

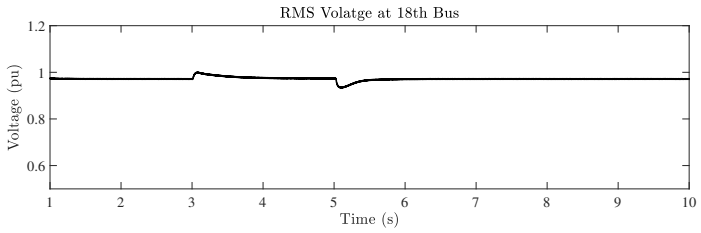
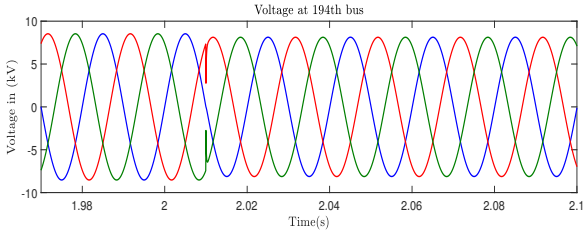


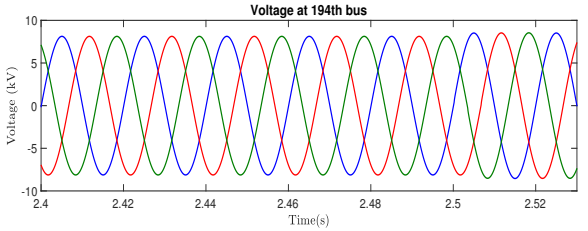
Figure 4.23: Voltage (RMS) at 18^{th} bus with DSTATCOM

4.6.2.2 Case 2- Sag With DSTATCOM

In this case the 207 bus system with DSTATCOM is simulated. The DSTATCOM is placed at 194^{th} bus in the system; this location is obtained by using above ACO



(a) Voltage waveform at PCC without DSTATCOM during starting of sag



(b) Voltage waveform at PCC without DSTATCOM during end of sag

Figure 4.24: Voltage waveform at PCC without DSTATCOM during sag

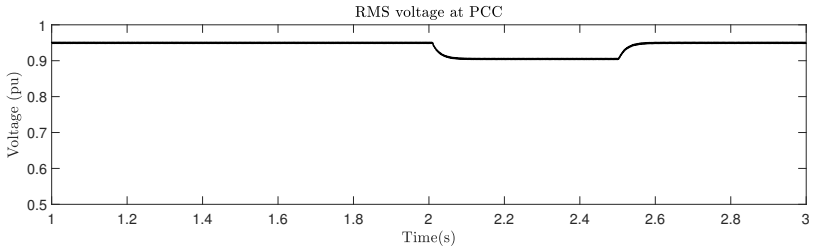


Figure 4.25: Voltage (RMS) at PCC without DSTATCOM with voltage sag in 207 bus system

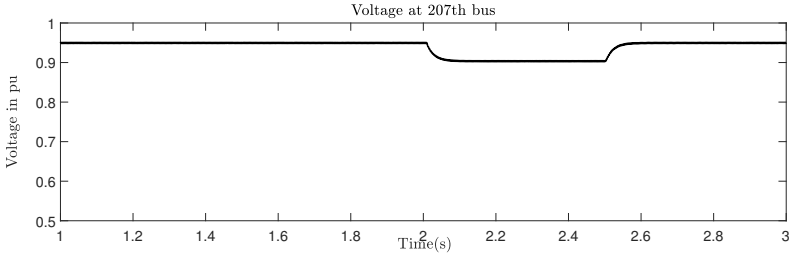


Figure 4.26: Voltage (RMS) at 207^{th} Bus without DSTATCOM

algorithm. In this case also, voltage sag is created at 196^{th} bus at 2s and sag is cleared at 2.5s. Before sag occurs, the DSTATCOM tries to maintain the voltage at 1 pu at 194^{th} bus and when sag occurs, the DSTATCOM tries to overcome the sag and maintains the voltage near to 1 pu and during sag, voltage is 0.95 pu, which is shown in figure 4.27. Figure 4.28 shows the phase voltage waveform at 194^{th} bus. Figure 4.29 shows the reactive power absorbed by the DSTATCOM. During sag, the reactive power supplied by DSTATCOM is increased. The RMS value of voltage at 207^{th} bus is shown in figure 4.30.

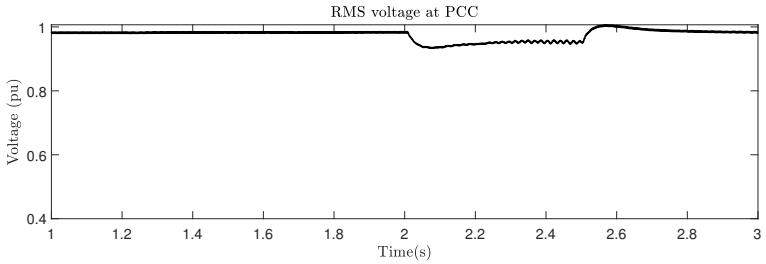
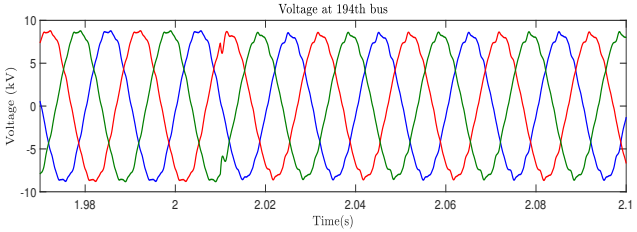
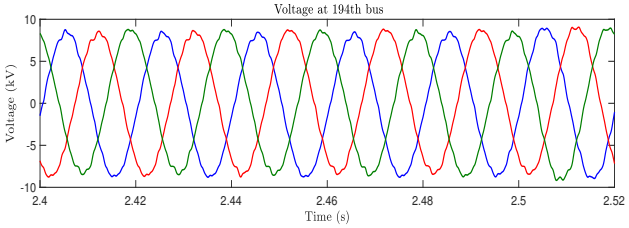


Figure 4.27: Voltage (RMS) at PCC with DSTATCOM with voltage sag in 207 bus system



(a) Voltage waveform at PCC with DSTATCOM at the starting of sag



(b) Voltage waveform at PCC with DSTATCOM at the end of sag

Figure 4.28: Voltage waveform at PCC with DSTATCOM

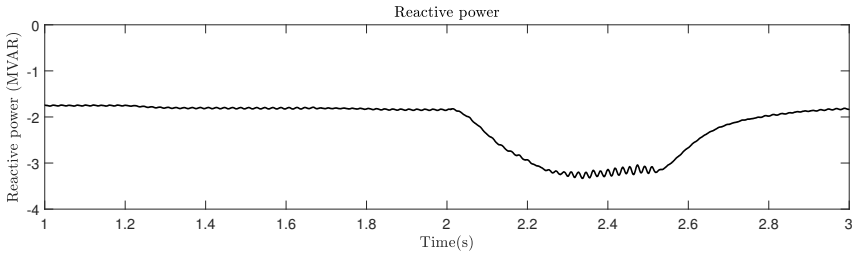


Figure 4.29: Reactive Power absorbed by DSTATCOM

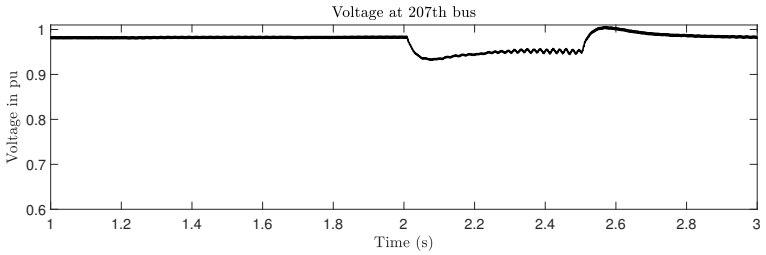


Figure 4.30: Voltage (RMS) at 207^{th} bus with DSTATCOM

4.6.2.3 Case 3- Swell Without DSTATCOM

In this case the GMIT 207 bus system without DSTATCOM is simulated. At 2s, a voltage swell is created which is shown in figure 4.31 and the RMS value of voltage at PCC is 0.98 pu. Figure 4.32 shows the three phase voltage waveform at 194^{th} bus of system. Figure 4.33 shows the RMS value of voltage at 207^{th} bus.

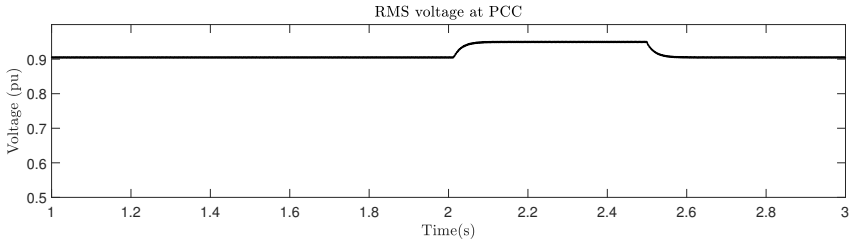
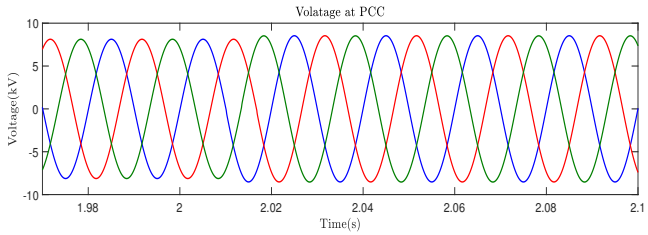
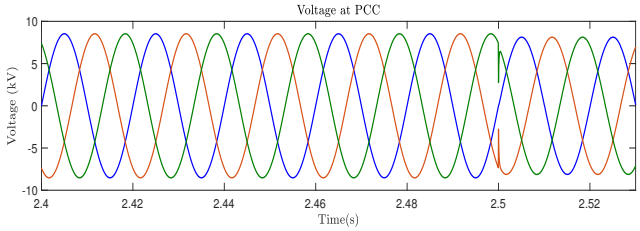


Figure 4.31: Voltage (RMS) at PCC without DSTATCOM with voltage swell in 207 bus system



(a) Voltage waveform at PCC without DSTATCOM at the starting of swell



(b) Voltage waveform at PCC without DSTATCOM at the end of swell

Figure 4.32: Voltage waveform at PCC without DSTATCOM with swell

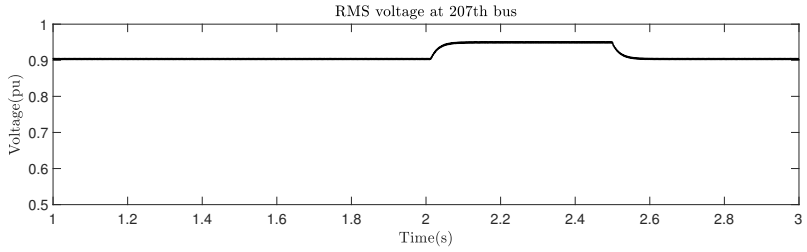


Figure 4.33: Voltage (RMS) at 207^{th} bus without DSTATCOM

4.6.2.4 Case 4- Swell With DSTATCOM

In this case the GMIT 207 bus system with DSTATCOM is simulated. The DSTATCOM is placed at 194^{th} bus in the system; this location is obtained by using above ACO algorithm. Before voltage swell, the DSTATCOM tries to maintain the voltage at 1 pu at 194^{th} bus. During the swell, the DSTATCOM tries to maintain the voltage constant which is shown in the figure 4.34. Figure 4.35 shows the phase voltage waveform at 194^{th} bus. The reactive power absorbed by DSTATCOM is shown in the figure 4.36. The RMS value of voltage at 207^{th} bus is shown in the figure 4.37. From above results it is observed that the improved controller works satisfactorily for

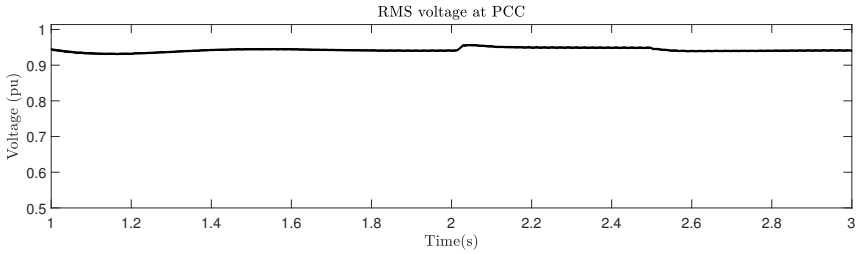
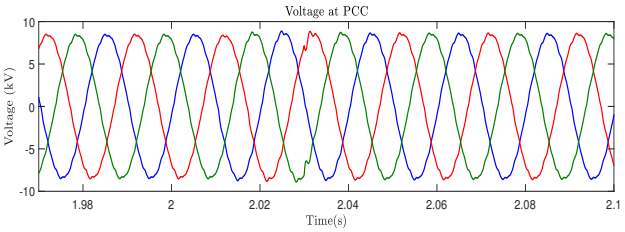
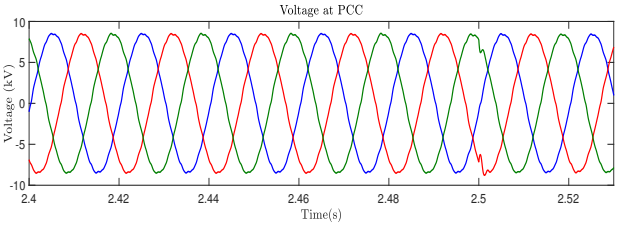


Figure 4.34: Voltage (RMS) at PCC with DSTATCOM with voltage swell in 207 bus system



(a) Voltage waveform at PCC with DSTATCOM at the starting of swell



(b) Voltage waveform at PCC with DSTATCOM at the end of swell

Figure 4.35: Voltage waveform at PCC with DSTATCOM during swell

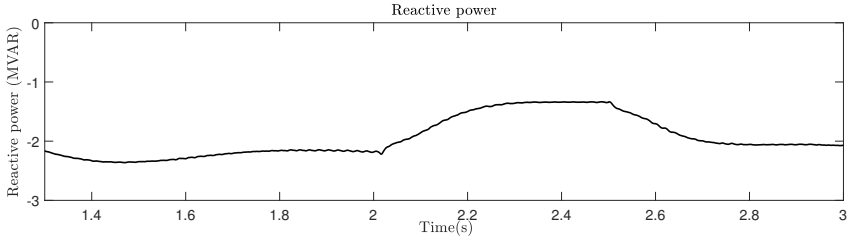


Figure 4.36: Reactive Power absorbed by DSTATCOM

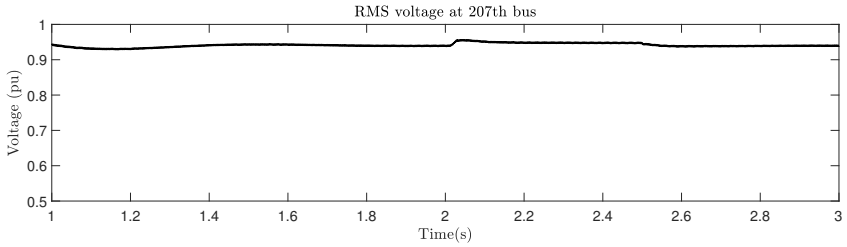


Figure 4.37: Voltage (RMS) at 207^{th} bus with DSTATCOM

IEEE 33 bus system for different conditions with placing in optimal location which is obtained by ACO algorithm. It is also observed that the controller will work satisfactorily when DSTATCOM is placed in a practical 11 kV system i.e. GMIT 207 bus system.

4.7 Summary

An effective method ACO for the placement of DSTATCOM in radial distribution system is presented. The presented method is validated for two different system: a) IEEE 33 bus system and b) GMIT 207 bus system which is presented in section 4.2

- The presented algorithm is tested on IEEE 33 bus system using MATLAB simulation which is summarised in table 4.4.

Table 4.4: Optimal location and size of DSTATCOM

Description	**IEEE 33 Bus system**		**GMIT 207 System**	
	One DSTATCOM	Two DSTATCOM	One DSTATCOM	Two DSTATCOM
Location	28	26,32	194	111,197
Size (MVAR)	1.988	1.058, 0.620	1.9093	1.2701, 0.9505

- After placing one DSTATCOM at optimal location in both the systems the load flow analysis are performed. The results show improvement in voltage profile and reduction in power loss using one DSTATCOM which is summarised in table 4.5.

Table 4.5: Voltage profile and power loss with one DSTATCOM

Description	IEEE 33 Bus system	GMIT 207 bus system
Minimum Voltage in pu	0.9321	0.8639
Power loss (MW)	0.1594	0.6200

- The load flow analysis with two DSTATCOM in IEEE 33 bus system and GMIT 207 bus system is performed and results are summarised in table 4.6. The voltage profile is increased compared to without DSTATCOM case and there is a significant reduction in power loss.

Table 4.6: Voltage profile and power loss with two DSTATCOM

Description	IEEE 33 Bus system	GMIT 207 bus system
Minimum Voltage in pu	0.9296	0.8608
Power loss (MW)	0.1407	0.5652

- The performance analysis of proposed positive and negative controller is performed in IEEE 33 bus system GMIT 207 bus system by placing DSTATCOM at optimal location which is discussed in section 4.3. From the results it is observed that using proposed controller the DSTATCOM is able to maintain the voltage 1 pu in both the systems.

Chapter 5

Impact of Addition of Distributed Energy Sources on the System Performance

The algorithm to find optimal location, size of DSTATCOM and performance analysis of DSTATCOM have been presented in the chapter 4. In modern power system, the need for interface of distribution generation sources to the distribution system are increasing day by day. When DG is integrated with the traditional system which is designed to operate in radial fashion, without considering new generation plant to integrate in future. In this new configuration, design considerations regarding the number, size location and technology of the DG connected must be taken into account as the short circuit levels are affected and miss-coordination problems with protection devices may arise. Therefore, to address these issues and increase penetration while avoiding the voltage rise issue on the LV distribution feeder, DSTATCOM is considered. This is because it is a mature device with fast dynamic response and can provide voltage stabilization and other power quality solutions at the distribution network. In literature, DSTATCOM is used to increase the DG penetration and control the voltage within the standard voltage limit PCC on a distribution feeder. So it is required to study the performance of DSTATCOM with the presence of DG. The impact of distributed energy sources on the system performance with and without DSTATCOM, are presented in this chapter.

5.1 Sizing of DG at Various Locations

In this section, the method to find size of the DG at various locations is discussed. The size of the DG is obtained according to method proposed by (Acharya et al., 2006). This is an analytical approach to calculate the size of the DG at particular location. The methodology is computationally less demanding. The objective of this method is also to reduce the power loss in the system. So this method is incorporated in the DG size calculation. To obtain the optimum size of DG at various locations, equation 5.1 is used.

$$P_{DGi} = P_{Di} + \frac{1}{\alpha_{ii}}[\beta_{ii}Q_i - \sum_{j=1 j\neq i}^{N} (\alpha_{ij}P_j - \beta_{ij}Q_j)] \tag{5.1}$$

The above equation gives the optimum size of DG for each bus i, for the loss to be minimum. Where, P_i and Q_i are the real power and reactive power injection at node i, P_{DGi} is the real power injection from DG placed at node i and P_{Di} is the load demand at node i. The α_{ij} and β_{ij} are given by equation 5.2 and equation 5.3,

$$\alpha_{ij} = \frac{r_{ij}}{v_i v_j} cos(\delta_i - \delta_j) \tag{5.2}$$

$$\beta_{ij} = \frac{r_{ij}}{v_i v_j} sin(\delta_i - \delta_j) \tag{5.3}$$

$$r_{ij} + jx_{ij} = z_{ij} \tag{5.4}$$

Where z_{ij} is ij^{th} element of Zbus matrix.

5.2 Performance Analysis

In this section, the performance analysis of IEEE 33 bus system with different scenario has been carried out. The performance analysis is done using MATLAB simulation. The single line diagram of IEEE 33 bus system is shown in figure 5.1. The size and optimal location of DSTATCOMs used for the simulation is obtained from the algorithm mentioned in the chapter 4. The performance analysis with different scenarios is presented below:

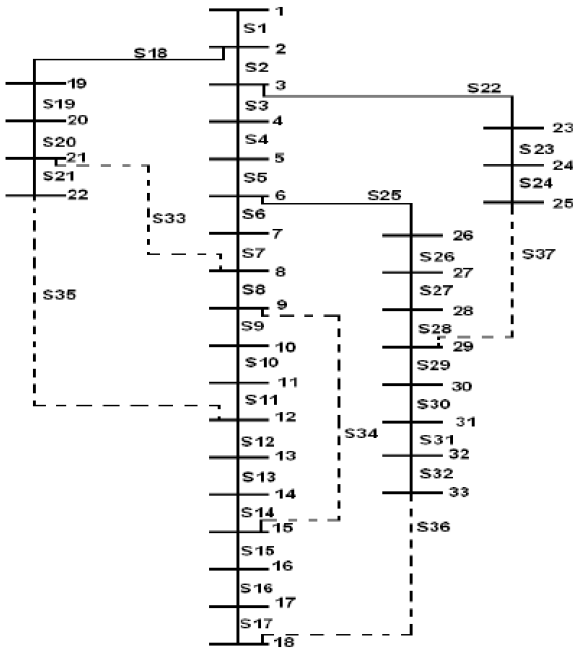


Figure 5.1: IEEE 33 bus System

5.2.1 Case1 : Without DG and DSTATCOM:

The table 5.1 shows the parameters obtained by conducting load flow study in 33 bus system with the absence of DSTATCOM and DG. The total active power load is 3.715 MW and reactive power load is 2.300 MVAR. Here 12.66 kV is taken as base voltage and 10 kVA is taken as base MVA. In the absence of DG and DSTATCOM, the total active power consumed from the grid is 3.9716 MW and the reactive power supplied from the grid is 2.4351 MVAR. The active power loss of 0.2026 MW is observed in the system. Figure 5.2 shows the voltage profile of IEEE 33 bus system in this case. The minimum voltage is observed at 18^{th} bus with the value of 0.9131 pu.

Table 5.1: Parameters without DSTATCOM and DG

Description	Values
Total active power in MW	3.9176
Total reactive power in MVAR	2.4351
Minimum voltage in pu (at 18^{th} bus)	0.9131
Total real power loss in MW	0.2026

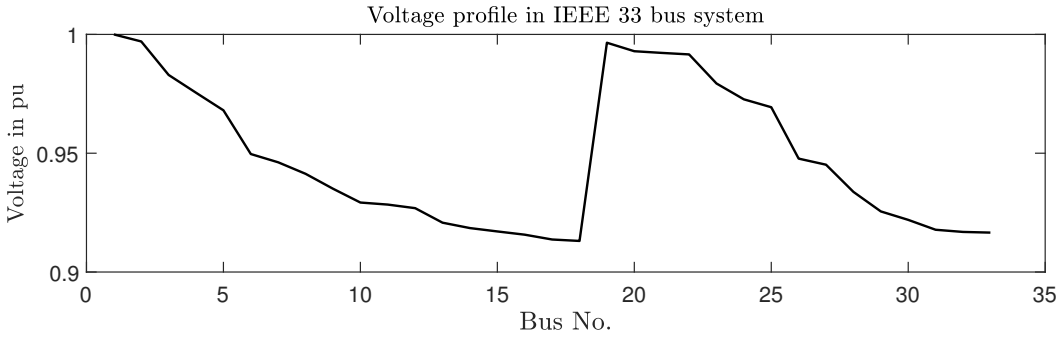


Figure 5.2: Voltage profile without DG and DSTATCOM

5.2.2 Case 2: With One DSTATCOM

Table 5.2 shows the load flow results of IEEE 33 bus system when a DSTATCOM of 1.918 MVAR is placed at 28^{th} bus. In this case, the total active power consumed from the grid is reduced to 3.8744 MW and the reactive power supplied from the grid is 0.4213 MVAR. The active power loss of 0.1594 MW is observed in the system. Figure 5.3 shows the voltage profile of IEEE 33 bus system in this case. The voltage at 18^{th} bus is increased to the value of 0.9351 pu.

Table 5.2: Parameters with one DSTATCOM

Description	Values
Total active power in MW	3.8744
Total reactive power in MVAR	0.4213
Minimum voltage in pu (at 18^{th} bus)	0.9351
Total real power loss in MW	0.1594

5.2.3 Case 3: With Two DSTATCOM

In this case, two DSTATCOMs are placed at bus 26 and 32 with the capacity of 1.058 MVAR and 0.62 MVAR respectively. The results obtained for this case is given in table 5.3 and voltage profile of 33 bus system when two DSTATCOMs are placed are given in figure 5.4. In this case, the total active power supplied from the grid is reduced to 3.854 MW and the reactive power supplied from the grid is 0.7188 MVAR. The active power loss of 0.1425 MW is observed in the system. The voltage at 18^{th}

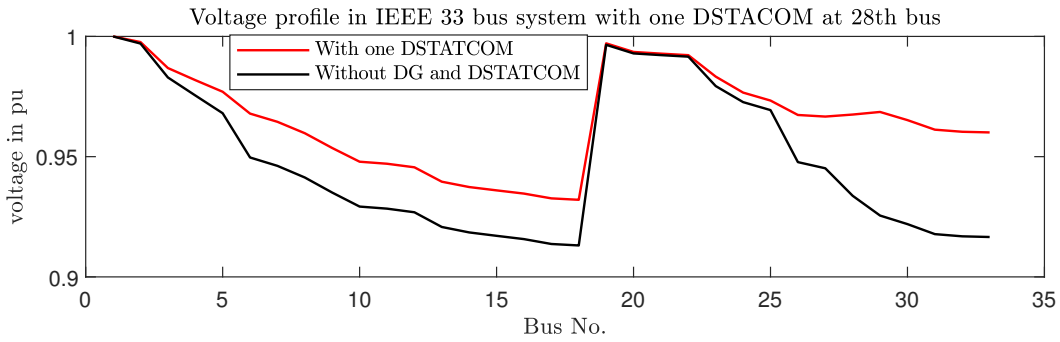


Figure 5.3: Voltage profile with one DSTATCOM

bus is increased to the value of 0.9295 pu which is less than the voltage obtained in one DSTATCOM case.

Table 5.3: Parameters with two DSTATCOM

Description	values
Total active power in MW	3.854
Total reactive power in MVAR	0.7188
Minimum voltage in pu (at 18^{th} bus)	0.9295
Total real power loss in MW	0.1425

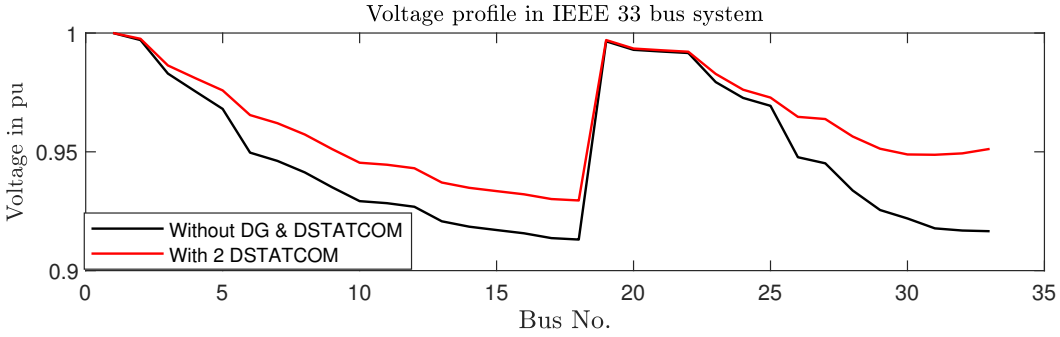


Figure 5.4: Voltage profile with two DSTATCOM

5.2.4 Case 4 : With One DG

In this case, one distributed generation source like photovoltaic plant having real power generation is placed at bus number 28, which is optimal location obtained for

the placement of DSTATCOM. The size of DG placed at 28^{th} bus is 1.8 MW, which is obtained according to method discussed in section 5.1. The results obtained for this case is given in table 5.4 and voltage profile of 33 bus system when one DG is placed is given in figure 5.5. In this case, the total active power supplied from the grid is reduced to 2.03 MW and the reactive power supplied from the grid is 2.3 MVAR. The active power loss of 0.1163 MW is observed in the system. The voltage at 18^{th} bus is increased to the value of 0.9398 pu.

Table 5.4: Parameters with One DG

Description	values
Total active power in MW	2.03
Total reactive power in MVAR	2.3
Minimum voltage in pu (at 18^{th} bus)	0.9398
Total real power loss in MW	0.1163

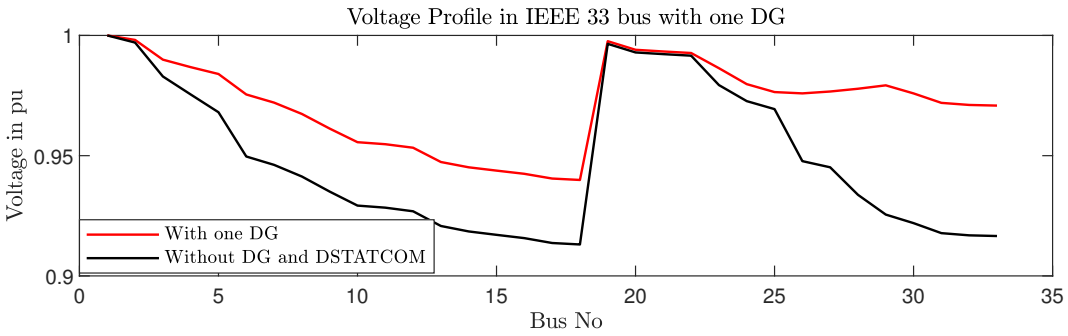


Figure 5.5: Voltage profile with one DG

5.2.5 Case 5: With One DG and One DSTATCOM

In this case, a DG and a DSTATCOM are placed at bus number 28, which is optimal location obtained for the placement of DSTATCOM. The size of DG and DSTATCOM placed at 28^{th} bus are 1.8 MW and 1.988 MVAR respectively. Size of DSTATCOM is obtained according to the algorithm presented in chapter 4 and capacity of DG is obtained according to method discussed in section 5.1. The results obtained for this case is given in table 5.5 and voltage profile of 33 bus system when one DSTATCOM and one DG are placed is given in figure 5.6. In this case, the total active power

supplied from the grid is reduced to 1.998 MW and the reactive power supplied from the grid is 0.3036 MVAR. The active power loss is reduced to 0.0798 MW. The voltage at 18^{th} bus is increased to the value of 0.9589 pu

Table 5.5: Parameters with one DG and one DSTATCOM

Description	values
Total active power in MW	1.998
Total reactive power in MVAR	0.3036
Minimum voltage in pu (at 18^{th} bus)	0.9589
Total real power loss in MW	0.0798

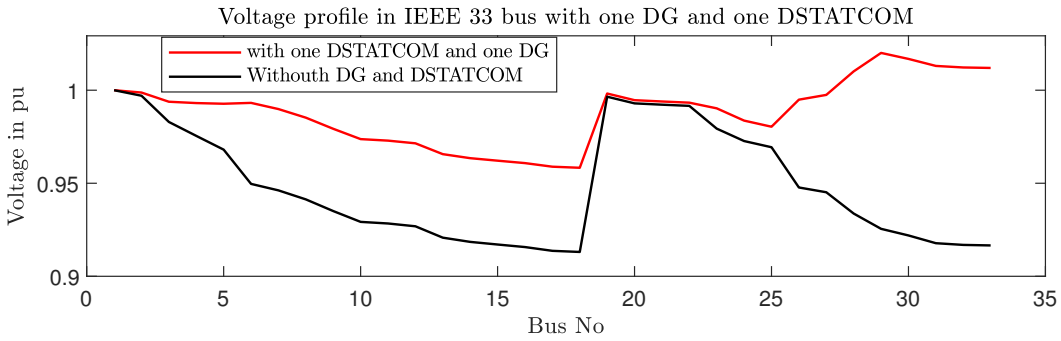


Figure 5.6: Voltage profile with one DG and one DSTATCOM

5.2.6 Case 6 : With One DG and Two DSTATCOM

One DG and two DSTATCOM are connected to IEEE 33 bus system with the optimal location obtained by the algorithm. The DG of size 1.8 MW is placed at bus 28 and DSTATCOMs of size 1.058 MVAR and 0.620 MVAR are placed at 26^{th} and 32^{nd} bus respectively. Size of DSTATCOM is obtained according to the algorithm presented in chapter 4 and capacity of DG is obtained according to method discussed in section 5.1. The results obtained for this case is given in table 5.6 and voltage profile of 33 bus system when one DG and two DSTATCOMs are placed are given in the figure 5.7. In this case, the total active power supplied from the grid is reduced to 1.9771 MW and the reactive power supplied from the grid is 0.6706 MVAR. The active power loss is reduced to 0.0625 MW. The voltage at 18^{th} bus is maintained at

0.9558 pu.

Table 5.6: Parameters with one DG and two DSTATCOM

Description	values
Total active power in MW	1.9771
Total reactive power in MVAR	0.6706
Minimum voltage in pu (at 18^{th} bus)	0.9558
Total real power loss in MW	0.0625

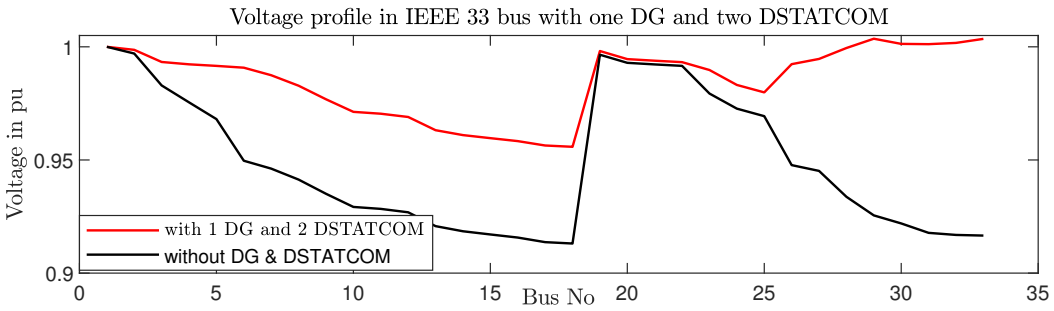


Figure 5.7: Voltage profile with one DG and two DSTATCOM

5.2.7 Case 7: With Two DG

Table 5.7 shows the results of load flow analysis of IEEE 33 bus system with two DG connected at 26^{th} and 32^{nd} bus. At 26^{th} bus, a DG of size 2.3 MW and at 32^{nd} bus, a DG of 1.2 MW is connected. Capacity of DG is obtained according to the method discussed in section 5.1. The voltage profile of 33 bus system when two DGs are placed is given in figure 5.8. In this case, the total active power supplied from the grid is further reduced to 0.4066 MW and the reactive power supplied from the grid is 2.39 MVAR. The active power loss is 0.1316 MW. The voltage at 18^{th} bus is maintained at 0.9627 pu.

Table 5.7: Parameters with two DG

Description	values
Total active power in MW	0.4066
Total reactive power in MVAR	2.39
Minimum voltage in pu (at 18^{th} bus)	0.9627
Total real power loss in MW	0.1316

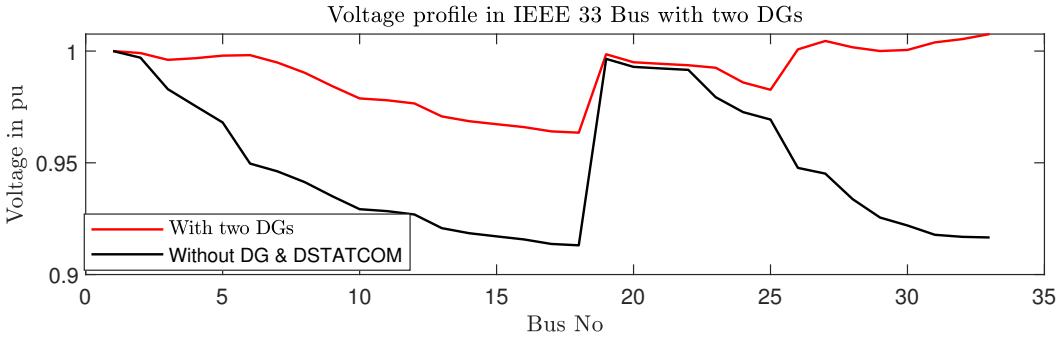


Figure 5.8: Voltage profile with two DG

5.2.8 Case 8: With Two DG and One DSTATCOM

In this analysis, two DG with one DSTATCOM are placed in IEEE 33 bus system. At 26^{th} bus, a DG of size 2.3 MW and at 32^{nd} bus, a DG of 1.2 MW is connected. A DSTATCOM is placed at 28^{th} bus with the capacity of 1.988 MVAR. Size of DSTATCOM is obtained according to the algorithm presented in chapter 4 and capacity of DG is obtained according to the method discussed in section 5.1. With this combination, the voltage at 18^{th} bus is increased to 0.9815 pu which is shown in figure 5.9 and active power loss is reduced to 0.0928 MW. From table 5.8, it is observed that the active and reactive power supplied from the grid is now reduced to 0.3092 MW and 0.3838 MVAR.

Table 5.8: Parameters with two DG and one DSTATCOM

Description	values
Total active power in MW	0.3092
Total reactive power in MVAR	0.3838
Minimum voltage in pu (at 18^{th} bus)	0.9815
Total real power loss in MW	0.0928

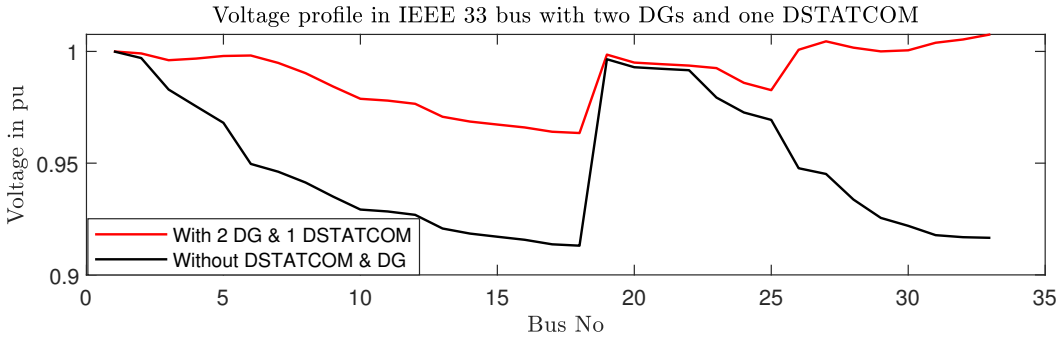


Figure 5.9: Voltage profile with two DG and one DSTATCOM

5.2.9 Case 9: With Two DG and Two DSTATCOM

Table 5.9 shows the results of load flow analysis of IEEE 33 bus system with 2 DGs and 2 DSTATCOMs placed at 26^{th} and 32^{nd} bus. The size of DG and DSTATCOM at 26^{th} bus is 2.3 MW and 1.058 MVAR respectively. Similarly the size of DG and DSTATCOM at 32^{nd} bus is 1.2 MW and 0.620 MVAR respectively. Size of DSTATCOM is obtained according to the algorithm presented in chapter 4 and capacity of DG is obtained according to the method discussed in section 5.1. After placing two DG and two DSTATCOMs, the voltage at 18^{th} bus is increased to 0.979 pu as shown in figure 5.10. The power loss in the system is reduced to 0.0810 MW.

Table 5.9: Parameters with two DG and two DSTATCOM

Description	values
Total active power in MW	0.2960
Total reactive power in MVAR	0.6839
Minimum voltage in pu (at 18^{th} bus)	0.979
Total real power loss in MW	0.0810

Figure 5.11 shows the voltage profile for all the nine scenarios. It is observed from the figure 5.11 that the voltage is found minimum at 18^{th} bus in base case, i.e. without DG and DSTATCOM.

The observations from the analysis are listed below:

(a) The voltage level at 18th bus increased to highest value of 0.9815 pu when the system is connected with two DG at 26^{th} and 32^{nd} bus and a DSTATCOM at 28^{th} bus.

(b) The active power loss is found maximum in base case and power loss found min-

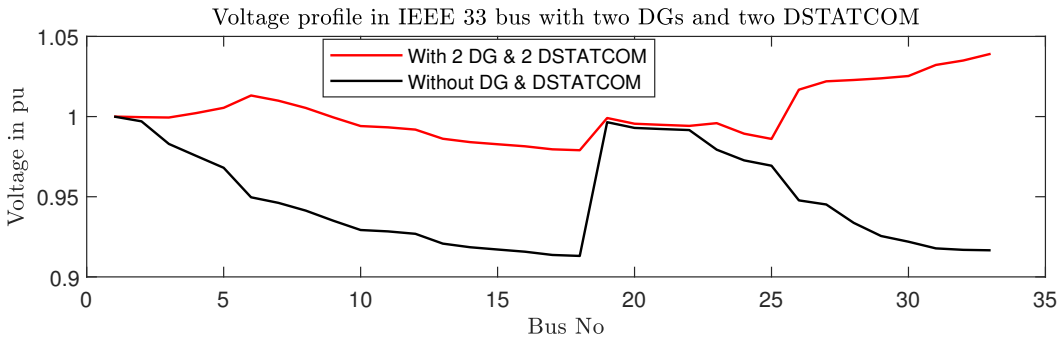


Figure 5.10: Voltage profile with two DG and two DSTATCOM

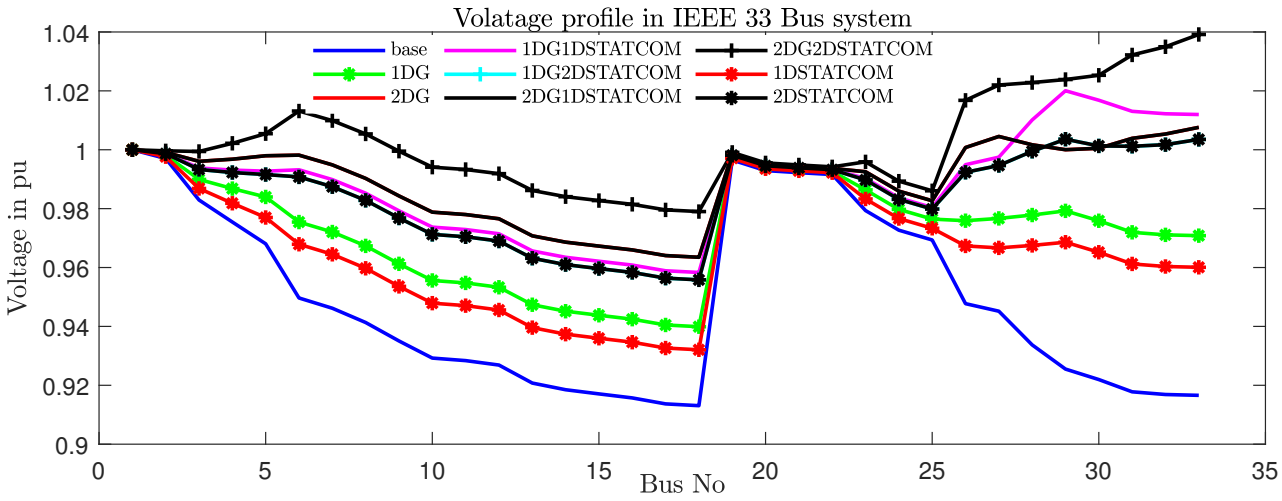


Figure 5.11: Voltage profile with different conditions

imum when one DG and two DSTATCOMs are placed. The DG is placed at 28^{th} bus and DSTATCOMs are placed at 26^{th} and 32^{nd} buses. But in this case voltage at 18^{th} bus is 0.9558 pu which is less than the voltage obtained in two DG and one DSTATCOM case.

(c) If only DSTATCOM is placed or only DG is placed, then reduction in power loss is less compared to the combination of both DG and DSTATCOM.

From the analysis it is observed that, the combination of one DG and two DSTATCOM was found better from power loss perspective. However, from voltage perspective, the combination of two DG with one DSTATCOM is found better compared to other combinations.

5.3 Summary

The investigations of impact of DSTATCOM and DG with different combinations are presented in the section 5.2. The location which is used for the analysis is obtained from chapter 4. From the analysis it is summarized as follows:

- On the perceptive of the voltage, performance with two DG and one DSTATCOM is found better compared to other combinations which is summarised in table 5.10. From the results it is observed that for the small system, by usage of multiple DSTATCOM have only marginal benefits and so it is better to go for single DSTATCOM in terms of cost perspective. But for larger system, the usage of multiple DSTATCOM placement would be beneficial. The optimisation is done considering power loss reduction, but from the performance analysis it is also observed that there is a possibility of improvement in voltage profile by selecting proper combination of DG and DSTATCOM.

Table 5.10: Voltage at 18^{th} bus of IEEE 33 bus system

Description	**Voltage in pu**
Without DG and DSTATCOM	0.9131
With one DSTATCOM	0.9351
With two DSTATCOM	0.9295
With one DG	0.9398
With one DG and one DSTATCOM	0.9589
With one DG and two DSTATCOM	0.9558
With two DG	0.9627
With two DG and one DSTATCOM	0.9815
With two DG and two DSTATCOM	0.979

- On the perceptive of the power loss, performance with one DG and two DSTATCOM is found better compared to other combinations. The power loss is found maximum in the system without DG and DSTATCOM, which is summarised in table 5.11.

Table 5.11: Power Loss in IEEE 33 bus system

Description	**Power loss in MW**
Without DG and DSTATCOM	0.2026
With one DSTATCOM	0.1594
With two DSTATCOM	0.1425
With one DG	0.1163
With one DG and one DSTATCOM	0.0798
With one DG and two DSTATCOM	0.0625
With two DG	0.1316
With two DG and one DSTATCOM	0.0928
With two DG and two DSTATCOM	0.0810

- As a trade-off to improve voltage as well as to reduce power loss, the performance with two DG and two DSTATCOM is found better compared to other combinations. In this case the voltage at 18^{th} bus is maintained at 0.979 pu and power loss is 0.081 MW.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In recent years, globally there is more concern for addressing power quality problems in modern distribution network. Custom power device is one of the solutions to solve power quality issues in distribution system. DSTATCOM is used in distribution system for performance improvement. The efficient working of DSTATCOM depends on the control algorithm which is used to generate switching pulses for controlling devices. Many control algorithms are found in literature which propose to mitigate different current related power quality issues using DSTATCOM. Most of controller proposed in the literature considers only positive sequence component. In this thesis, to overcome these problems, a control strategy is developed which has the ability to reduce negative sequence components. This thesis also presents an algorithm for optimal location for placement of DSTATCOM. The general conclusions of each chapter are as follows:

In chapter 1, the various topologies of DSTATCOM were reviewed. The issues related to power quality were discussed. To overcome these issues, many control algorithms for DSTATCOM from the literature were also discussed. In this chapter, the research gap identified from the literature were presented. A summary of work and the contents of the chapters that follow were presented.

In chapter 2, the design of existing positive sequence controller and improved positive sequence controller are discussed in the first section of this chapter. When system voltage is unbalanced, there will be both positive and negative sequence components. To compensate both the components, it is required for DSTATCOM to produce both

positive and negative sequence component in its output. To compensate both positive and negative sequence components, a modified controller is proposed in the later section of the chapter. The simulation was carried out by considering two different systems: a) Test system and b) IEEE 9 bus system using MATLAB Simulink. The analysis is summarized as below:

- Performance improved positive sequence controller is found better in RMS voltage perception.
- The PCC voltage and current THD are reduced using improved positive and negative sequence controller
- In negative sequence voltage perception, it is found that the improved positive and negative sequence controller has better performance
- From the performance analysis it is recommended that, the improved positive and negative sequence controller is better to maintain the voltage and THD as per limits of IEEE 519 standards.

In chapter 3, the existing positive sequence controller and improved positive and negative sequence controllers are analyzed under fault scenario. The simulation was carried out by considering three unsymmetrical faults: a) Single line to ground fault, b) Double line to ground fault and c) Double line fault without DSTATCOM, with existing positive sequence controller and proposed positive and negative sequence controller. The contribution to short circuit current in the case of improved positive and negative sequence controller is less and the performance of DSTATCOM with improved positive and negative sequence controller found better in perception of voltage in each phase. From the results, it is observed that, low voltage ride through capability of the system is increased by connecting DSTATCOM.
In chapter 4, an effective algorithm for optimal placement and sizing of the DSTATCOM using ant colony algorithm is presented. The present method is validated using MATLAB simulation for IEEE 33 bus system and GMIT 207 bus distribution system. The optimal location for placement of one DSTATCOM and two DSTATCOMs are obtained. Using obtained size and location, DSTATCOMs were placed and load flow analysis were performed. The results show improvement in voltage profile and reduction in power loss using one DSTATCOM and with two DSTATCOM, the voltage

profile is increased compared to without DSTATCOM case and there is a significant reduction in power loss.
In chapter 5, the investigations on impact of DG and DSTATCOM with different combinations were presented. The optimal locations were obtained from algorithm presented in chapter 4. From the analysis it is summarized as follows:

- On the perceptive of the voltage, performance with two DG and one DSTATCOM is found better compared to other combinations.

- On the perceptive of the power loss, performance with one DG and two DSTATCOM is found better compared to other combinations.

- As a trade-off to improve voltage as well as reduce to power loss, the performance with two DG and two DSTATCOM is found better compared to other combinations.

In modern distribution system, DSTATCOM is a affective solution for power quality problems. The proposed controller will work effectively in modern distribution system by compensating both positive and negative sequence components. It also helps to maintain the THD within IEEE 519 standards. It is observed that this work need to be extended on following key points:

- Design of controller is done by considering only voltage component. It also required to address current components.

- This controller is design for 3 phase 3 wire system. There is a scope to study and develop the controller for 3 phase 4 wire system.

- When multiple DSTATCOMs are used, then there is need to study on coordination of controller. This is not performed in this work.

From the above key points, the future scope of work is presented in next section.

6.2 Future scope

The future scope of this research work can be extended to study of:

- The controllers for neutral current compensation in three phase four wire system.
- Proper coordination of controller in the case of multiple DSTATCOM and other compensating devices.
- The performance DSTATCOM in terms of fault ride through capability in the presence of renewable energy source in grid connected mode and islanding mode.
- Optimal placement and sizing algorithm for different combinations DG and DSTATCOM in modern power system.

Appendix A

Design of DSTATCOM Components

Basic circuit diagram of VSC based DSTATCOM connected to the system is shown in figure A.1. It consists of interfacing inductor, control algorithm and other auxiliary components. R_s and L_s are considered as line resistance and inductance respectively. L_f is interfacing inductor. The three phase diode rectifier is used as nonlinear load. The power circuit components are designed using following mathematical equations.

The DC bus voltage is given as

$$V_{dc} = \frac{2\sqrt{(2)}v_{LL}}{\sqrt{3}m} \tag{A.1}$$

Where, m is the modulation index and is considered as 1 and v_{LL} is the AC line output voltage of VSC used in DSTATCOM. The value of capacitor of VSC of DSTATCOM is computed as DC link capacitor, which is given by equation A.2. (Singh et al., 2014)

$$\frac{1}{2}C_{dc}(V_{dc}^2 - V_{dc1}^2) = 3gv_{ph}(aI)t \tag{A.2}$$

Where, V_{dc} is nominal DC voltage, V_{dc1} is the minimum voltage level of DC bus, a is the overloading factor which is taken as 1.2, v_{ph} is the supply phase voltage, factor g is varying between 0.04 and 0.15, I is the phase current of VSC and t is the time for which DC bus voltage is to be recovered. Here t=0.08s, g=0.07 is used to calculate the DC bus capacitance. The value of interfacing inductor is estimated as AC inductance,

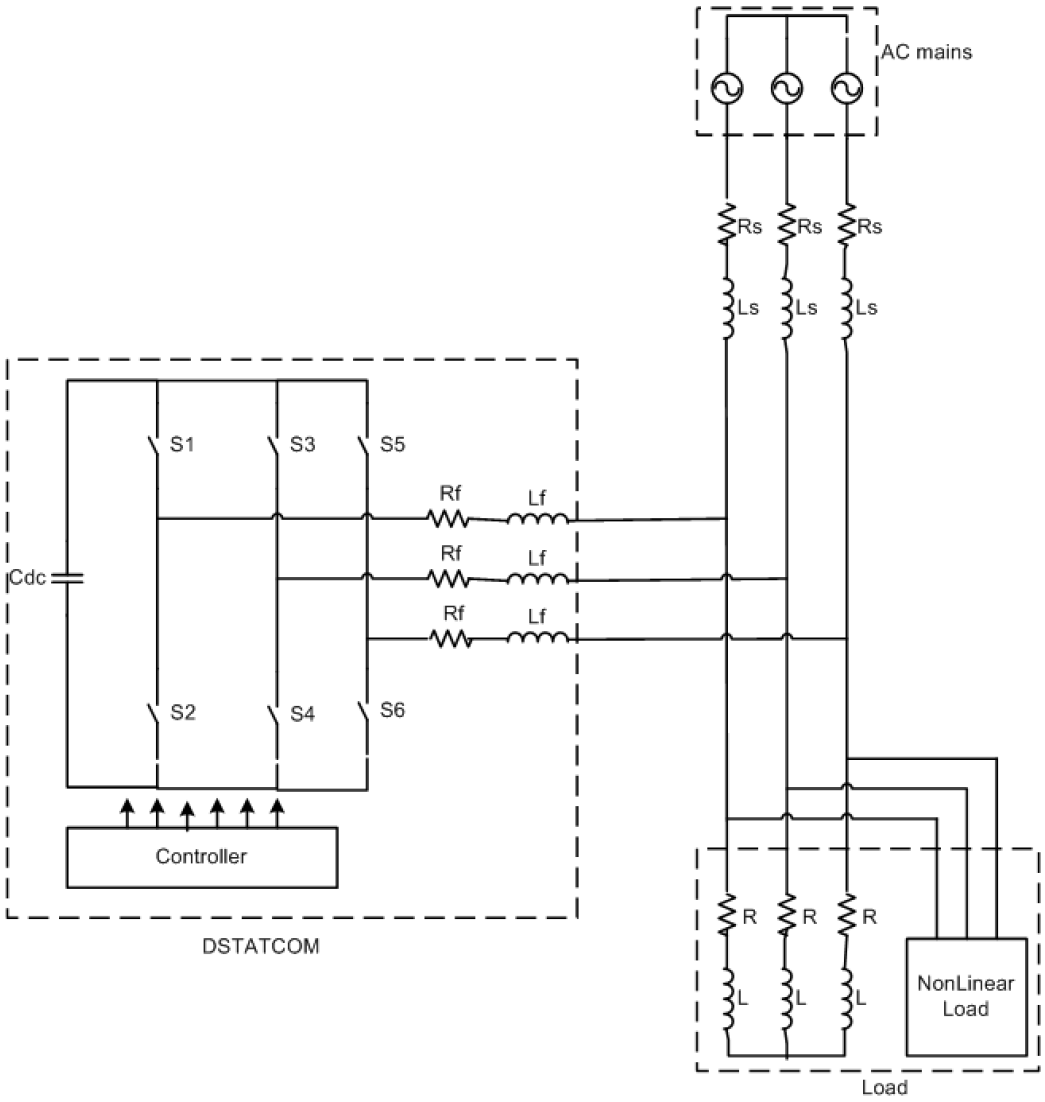


Figure A.1: DSTATCOM system configuration

which is given by equation A.3,(Singh et al., 2014)

$$L_f = \frac{\sqrt{3}mV_{dc}}{12af_s i_{cr}} \tag{A.3}$$

Where, V_{dc} is the DC bus voltage, a=1.2, m=1, f_s is the switching frequency and i_{cr} is the acceptable percentage range of current ripple in VSC output current (Singh et al., 2014).

Appendix B

Details of Test Systems

B.1 9 Bus System

The IEEE 9 bus system is a 9 bus single feeder radial distribution system which is shown in figure B.1 (Rao and Narasimham, 2008). This system has zero laterals. The rated line voltage of the system is 23 kV. The details of the feeder and load characteristics are given in table B.1 and B.2 respectively.

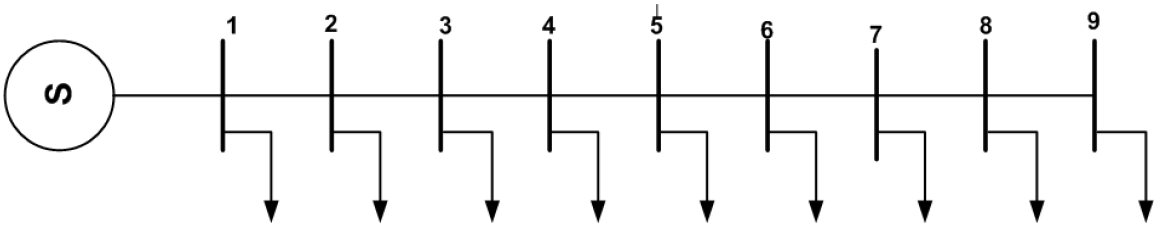


Figure B.1: 9 Bus System

B.2 GMIT 207 Bus System

This test system is a practical radial distribution network from the G Madegowda Institute of Technology (GMIT), Karnataka, India. Figure B.2 shows the single line diagram of GMIT 207 bus distribution network in MI power software environment. It consists of 11 kV system with 207 buses and 99 transformers. The loads are obtained by considering the rating of transformer. The active power loads are obtained by multiplying the rating of transformer by the power factor of 0.85. The total system

Table B.1: Line data of 9 bus system

line No	From bus	To bus	R(Ω)	X(Ω)
1	0	1	0.1233	0.4127
2	1	2	0.0140	0.6057
3	2	3	0.7463	1.2050
4	3	4	0.6984	0.6084
5	4	5	1.9831	1.7276
6	5	6	0.9053	0.7886
7	6	7	2.0552	1.1640
8	7	8	4.7953	2.7160
9	8	9	5.3434	3.0264

Table B.2: Load data of 9 bus system

Bus	P(kW)	Q (kVAR)
1	1840	460
3	980	340
4	1790	446
5	1598	1840
6	1610	600
7	780	110
8	980	130
9	1640	200

active power load is 5.6856 MW and total reactive power load is 3.5231 MVAR. (The data is obtained from PRDC Bangalore). Table B.3 shows the line and load data of 207 bus system. The base value are 1 MVA and 11 kV are taken for per unit calculations.

Table B.3: Line and Load Data of GMIT 207 bus system

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
1	1	2	0.00026	0.00015	0	0
2	2	3	0.00014	0.00008	0	0
3	3	4	0.00013	0.00008	0	0
4	4	5	0.00009	0.00006	21.25	13.167
5	5	6	0.00011	0.00007	0	0
6	6	7	0.00011	0.00007	0	0
7	7	8	0.00015	0.00009	21.25	13.167

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
8	8	9	0.00013	0.00008	0	0
9	9	10	0.00013	0.00008	53.55	33.18
10	10	11	0.00013	0.00008	0	0
11	11	12	0.00006	0.00003	53.55	33.18
12	12	13	0.00016	0.00010	0	0
13	13	14	0.00009	0.00005	53.55	33.18
14	14	15	0.00012	0.00007	0	0
15	15	16	0.00012	0.00007	0	0
16	16	17	0.00011	0.00007	0	0
17	17	18	0.00011	0.00007	21.25	13.167
18	18	19	0.00022	0.00013	53.55	33.18
19	19	20	0.00024	0.00014	0	0
20	20	21	0.00022	0.00013	0	0
21	21	22	0.00023	0.00014	0	0
22	22	23	0.00014	0.00009	0	0
23	23	24	0.00019	0.00011	85	52.67
24	24	25	0.00012	0.00007	0	0
25	25	26	0.00019	0.00011	0	0
26	26	27	0.00013	0.00008	0	0
27	27	28	0.00019	0.00011	0	0
28	28	29	0.00016	0.00010	21.25	13.167
29	29	30	0.00022	0.00013	0	0
30	30	31	0.00027	0.00016	0	0
31	31	32	0.00021	0.00013	53.55	33.18
32	32	33	0.00022	0.00013	212.5	13.167
33	33	34	0.00015	0.00009	0	0
34	34	35	0.00011	0.00006	0	0
35	35	36	0.00012	0.00007	53.55	33.18
36	36	37	0.00014	0.00008	21.25	131.67
37	37	38	0.00026	0.00015	0	0
38	38	39	0.00014	0.00008	21.25	13.167
39	39	40	0.00011	0.00007	21.25	13.167

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
40	40	41	0.00024	0.00014	21.25	13.167
41	41	42	0.00024	0.00014	0	0
42	42	43	0.00012	0.00007	0	0
43	43	44	0.00012	0.00007	21.25	13.167
44	44	45	0.00025	0.00015	21.25	13.167
45	45	46	0.00027	0.00016	53.55	33.18
46	46	47	0.00024	0.00014	53.55	33.18
47	47	48	0.00025	0.00015	0	0
48	48	49	0.00022	0.00013	0	0
49	49	50	0.00025	0.00015	212.5	131.67
50	50	51	0.00023	0.00014	0	0
51	51	52	0.00027	0.00016	0	0
52	52	53	0.00022	0.00013	212.5	131.67
53	53	54	0.00024	0.00014	0	0
54	54	55	0.00022	0.00013	21.25	13.167
55	55	56	0.00026	0.00015	0	0
56	56	57	0.00022	0.00013	21.25	13.167
57	57	58	0.00026	0.00015	0	0
58	58	59	0.00023	0.00014	21.25	13.167
59	59	60	0.00023	0.00014	0	0
60	60	61	0.00023	0.00014	0	0
61	61	62	0.00024	0.00014	53.55	33.18
62	62	63	0.00020	0.00012	0	0
63	63	64	0.00021	0.00012	212.5	0.132
64	64	65	0.00028	0.00017	85	52.67
65	65	66	0.00027	0.00016	212.5	131.67
66	66	67	0.00012	0.00007	21.25	13.167
67	67	68	0.00019	0.00011	0	0
68	68	69	0.00022	0.00013	0	0
69	69	70	0.00019	0.00011	53.55	33.18
70	70	71	0.00018	0.00011	0	0
71	71	72	0.00023	0.00014	0	0

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
72	72	73	0.00028	0.00017	0	0
73	73	74	0.00026	0.00015	0	0
74	74	75	0.00028	0.00017	21.25	13.167
75	75	76	0.00020	0.00012	21.25	13.167
76	76	77	0.00029	0.00017	21.25	13.167
77	77	78	0.00034	0.00020	0	0
78	78	79	0.00035	0.00021	0	0
79	79	80	0.00039	0.00023	53.55	33.18
80	80	81	0.00039	0.00023	53.55	33.18
81	81	82	0.00028	0.00017	0	0
82	82	83	0.00033	0.00019	0	0
83	83	84	0.00033	0.00020	21.25	13.167
84	84	85	0.00069	0.00041	0	0
85	85	86	0.00029	0.00017	0	0
86	86	87	0.00026	0.00016	0	0
87	87	88	0.00025	0.00015	212.5	131.67
88	88	89	0.00021	0.00013	0	0
89	89	90	0.00020	0.00012	53.55	33.18
90	90	91	0.00023	0.00014	0	0
91	91	92	0.00014	0.00008	21.25	13.167
92	84	93	0.00029	0.00017	21.25	13.167
93	93	94	0.00029	0.00017	0	0
94	94	95	0.00033	0.00020	21.25	13.167
95	95	96	0.00033	0.00020	0	0
96	96	97	0.00023	0.00014	85	52.67
97	97	98	0.00024	0.00014	0	0
98	98	99	0.00012	0.00007	21.25	13.167
99	99	100	0.00021	0.00013	0	0
100	100	101	0.00017	0.00010	212.5	131.67
101	97	102	0.00024	0.00014	21.25	13.167
102	102	103	0.00029	0.00017	0	0
103	103	104	0.00027	0.00016	21.25	13.167

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
104	104	105	0.00018	0.00011	0	0
105	105	106	0.00027	0.00016	0	0
106	106	107	0.00009	0.00005	0	0
107	107	108	0.00018	0.00011	0	0
108	108	109	0.00022	0.00013	21.25	13.167
109	108	110	0.00015	0.00009	21.25	13.167
110	109	111	0.00042	0.00015	21.25	13.167
111	110	112	0.00024	0.00015	21.25	13.167
112	112	113	0.00017	0.00010	0	0
113	113	114	0.00009	0.00005	53.55	33.18
114	114	115	0.00021	0.00012	0	0
115	115	116	0.00022	0.00013	53.55	33.18
116	116	117	0.00020	0.00012	53.55	33.18
117	114	118	0.00024	0.00014	0	0
118	118	119	0.00026	0.00015	0	0
119	119	120	0.00025	0.00015	21.25	13.167
120	120	121	0.00034	0.00020	0	0
121	121	122	0.00020	0.00012	21.25	13.167
122	122	123	0.00026	0.00015	0	0
123	123	124	0.00025	0.00015	0	0
124	124	125	0.00029	0.00017	21.25	13.167
125	125	126	0.00025	0.00015	53.55	33.18
126	109	127	0.00053	0.00031	21.25	13.167
127	127	128	0.00037	0.00022	21.25	13.167
128	128	129	0.00016	0.00009	0	0
129	129	130	0.00021	0.00013	0	0
130	130	131	0.00035	0.00021	0	0
131	131	132	0.00006	0.00004	0	0
132	132	133	0.00020	0.00012	53.55	33.18
133	132	134	0.00050	0.00030	21.25	13.167
134	134	135	0.00023	0.00014	0	0
135	135	136	0.00023	0.00014	53.55	33.18

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
136	136	137	0.00015	0.00009	21.25	13.167
137	137	138	0.00006	0.00003	21.25	13.167
138	128	139	0.00030	0.00018	0	0
139	139	140	0.00025	0.00015	21.25	13.167
140	140	141	0.00028	0.00017	21.25	13.167
141	141	142	0.00026	0.00015	0	0
142	142	143	0.00030	0.00018	53.55	33.18
143	143	144	0.00028	0.00016	0	0
144	144	145	0.00025	0.00015	212.5	131.67
145	141	146	0.00055	0.00032	21.25	13.167
146	146	147	0.00030	0.00018	0	0
147	147	148	0.00023	0.00014	0	0
148	148	149	0.00023	0.00013	21.25	13.167
149	149	150	0.00023	0.00014	0	0
150	150	151	0.00022	0.00013	53.55	33.18
151	151	152	0.00029	0.00017	85	52.67
152	146	153	0.00036	0.00022	0	0
153	153	154	0.00045	0.00027	0	0
154	154	155	0.00044	0.00026	0	0
155	155	156	0.00045	0.00027	21.25	13.167
156	156	157	0.00039	0.00023	0	0
157	157	158	0.00022	0.00013	0	0
158	158	159	0.00019	0.00012	85	52.67
159	159	160	0.00043	0.00026	0	0
160	160	161	0.00116	0.00035	0	0
161	161	162	0.00074	0.00023	0	0
162	162	163	0.00035	0.00011	21.25	13.167
163	163	164	0.00114	0.00035	0	0
164	164	165	0.00111	0.00034	21.25	13.167
165	165	166	0.00090	0.00027	21.25	13.167
166	165	167	0.00045	0.00016	0	0
167	167	168	0.00083	0.00025	212.5	131.67

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
168	168	169	0.00047	0.00014	0	0
169	169	170	0.00108	0.00033	0	0
170	170	171	0.00068	0.00021	0	0
171	171	172	0.00045	0.00014	21.25	13.167
172	172	173	0.00063	0.00019	0	0
173	173	174	0.00029	0.00009	53.55	33.18
174	174	175	0.00024	0.00007	0	0
175	175	176	0.00033	0.00012	21.25	13.167
176	174	177	0.00050	0.00018	21.25	13.167
177	177	178	0.00009	0.00003	0	0
178	178	179	0.00028	0.00009	0	0
179	179	180	0.00068	0.00021	0	0
180	180	181	0.00052	0.00016	53.55	33.18
181	181	182	0.00058	0.00018	53.55	33.18
182	182	183	0.00051	0.00016	0	0
183	183	184	0.00066	0.00020	53.55	33.18
184	184	185	0.00062	0.00019	0	0
185	185	186	0.00055	0.00017	53.55	33.18
186	186	187	0.00064	0.00019	21.25	13.167
187	187	188	0.00050	0.00015	212.5	131.67
188	188	189	0.00078	0.00024	212.5	131.67
189	189	190	0.00046	0.00014	0	0
190	190	191	0.00107	0.00033	85	52.67
191	191	192	0.00111	0.00034	21.25	13.167
192	190	193	0.00061	0.00018	0	0
193	193	194	0.00061	0.00019	212.5	131.67
194	194	195	0.00054	0.00016	0	0
195	195	196	0.00060	0.00018	21.25	13.167
196	196	197	0.00017	0.00005	0	0
197	197	198	0.00025	0.00015	0	0
198	198	199	0.00025	0.00015	0	0
199	199	200	0.00024	0.00014	0	0

S.No	From (bus)	To (bus)	R (pu)	X (pu)	P (kW)	Q (kVAR)
200	200	201	0.00024	0.00014	21.25	13.167
201	196	202	0.00027	0.00016	0	0
202	202	203	0.00058	0.00018	0	0
203	203	204	0.00064	0.00020	21.25	13.167
204	204	205	0.00057	0.00017	21.25	13.167
205	205	206	0.00058	0.00018	53.55	33.18
206	206	207	0.00058	0.00018	53.55	33.18

B.3 IEEE 33 Bus System

The IEEE 33 Bus system contains 5 tie switches and 32 sectionalizing switches. Figure B.3 shows the single line diagram of IEEE 33 bus test system. In the network, sectionalize switches (normally closed) are numbered from 1 to 32 and tie-switches (normally open) are numbered from 33 to 37. The line and load data of IEEE 33 bus system is given in table B.4 (Dharageshwari and Nayanatara, 2015).

Table B.4: Details of line and load data of IEEE 33 bus system

From Bus	To Bus	P (kW)	Q (kVAR)	R (Ω)	X (Ω)
1	2	100	60	0.0922	0.0470
2	3	90	40	0.4930	0.251 1
3	4	120	80	0.3660	0.1 864
4	5	60	30	0.3811	0.1941
5	6	60	20	0.8190	0.7070
6	7	200	100	0.1872	0.6188
7	8	200	100	1.7114	1.2351
8	9	60	20	1.0300	0.7400
9	10	60	20	1.0440	0.7400
10	11	45	30	0.1966	0.0650
11	12	60	35	0.3744	0.1238
12	13	60	35	1.4680	1.1550
13	14	120	80	0.5416	0.7129
14	15	60	10	0.5910	0.5260

From Bus	To Bus	P (kW)	Q (kVAR)	R (Ω)	X (Ω)
15	16	60	20	0.7463	0.5450
16	17	60	20	1.2890	1.7210
17	18	90	40	0.7320	0.5740
2	19	90	40	0.1640	0.1565
19	20	90	40	1.5042	1.3554
20	21	90	40	0.4095	0.4784
21	22	90	40	0.7089	0.9373
3	23	90	50	0.4512	0.3083
23	24	420	200	0.8980	0.7091
24	25	420	200	0.8960	0.7011
5	26	60	25	0.2030	0.1034
26	27	60	25	0.2842	0.1447
27	28	60	20	1.0590	0.9337
28	29	120	70	0.8042	0.7006
29	30	200	600	0.5075	0.2585
30	31	150	70	0.9744	0.9630
31	32	210	100	0.3105	0.3619
32	33	60	40	0.3410	0.5302

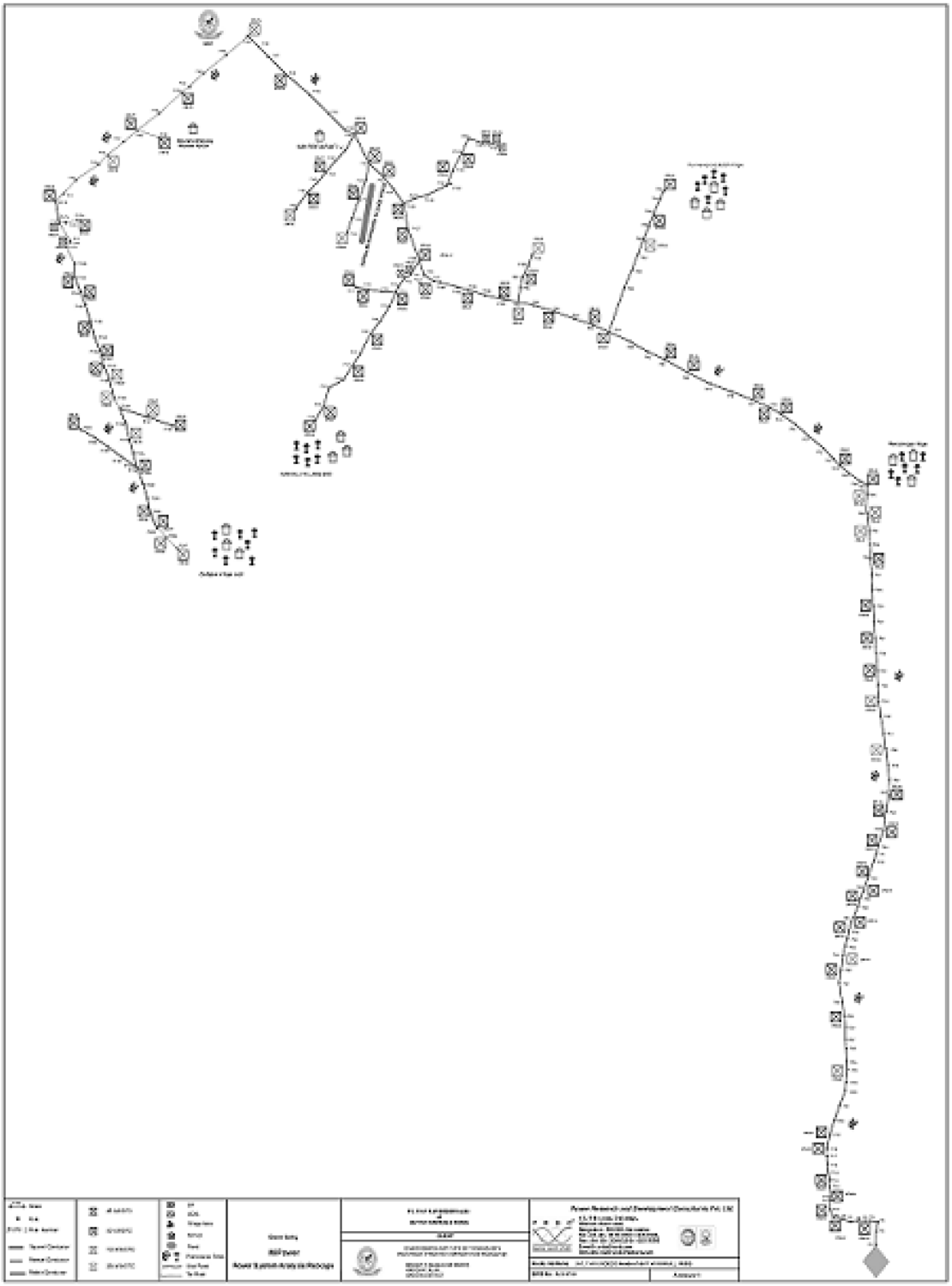


Figure B.2: Single line diagram of GMIT 207 bus system

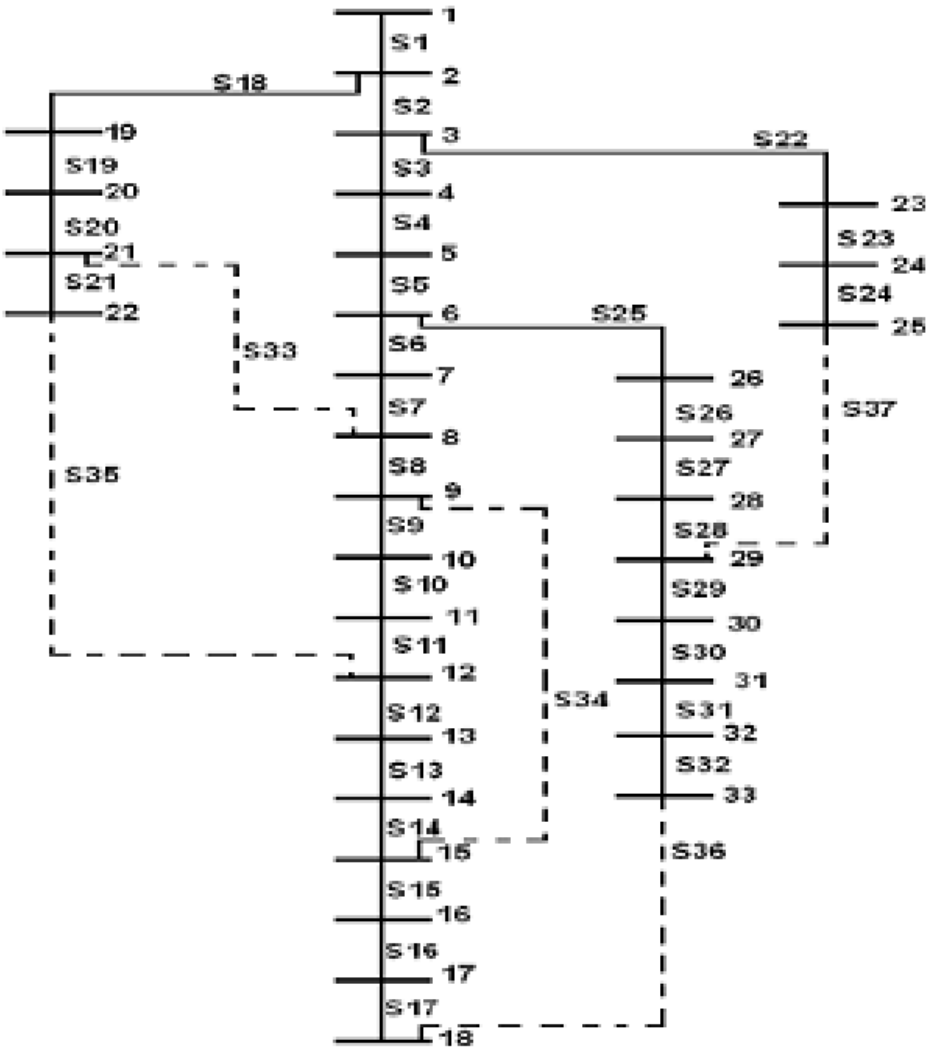


Figure B.3: Single line diagram of IEEE 33 bus system

Bibliography

Acharya, N., Mahat, P., and Mithulananthan, N. (2006). An analytical approach for dg allocation in primary distribution network. *International Journal of Electrical Power & Energy Systems*, 28(10):669–678.

Almutairi, O. (2017). Fault current generation by statcom. Master's thesis, Chalmers University of Technology, Sweden.

Amoozegar, D. (2016). Dstatcom modelling for voltage stability with fuzzy logic pi current controller. *International Journal of Electrical Power & Energy Systems*, 76:129–135.

Arya, S. R. and Singh, B. (2013a). Implementation of distribution static compensator for power quality enhancement using learning vector quantisation. *IET Generation, Transmission & Distribution*, 7(11):1244–1252.

Arya, S. R. and Singh, B. (2013b). Neural network based conductance estimation control algorithm for shunt compensation. *IEEE Transactions on Industrial Informatics*, 10(1):569–577.

Arya, S. R. and Singh, B. (2013c). Performance of dstatcom using leaky lms control algorithm. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 1(2):104–113.

Badoni, M., Singh, A., and Singh, B. (2015). Variable forgetting factor recursive least square control algorithm for dstatcom. *IEEE Transactions on Power Delivery*, 30(5):2353–2361.

Colorni, A., Dorigo, M., Maffioli, F., Maniezzo, V., Righini, G., and Trubian, M. (1996). Heuristics from nature for hard combinatorial optimization problems. *International Transactions in Operational Research*, 3(1):1–21.

Colorni, A., Dorigo, M., and Maniezzo, V. (1992). A genetic algorithm to solve the timetable problem. *Politecnico di Milano, Milan, Italy TR*, pages 90–060.

Comparatore, L., Renault, A., Pacher, J., Rodas, J., and Gregor, R. (2018). Finite control set model predictive control strategies for a three-phase seven-level cascade h-bridge dstatcom. In *2018 7th International Conference on Renewable Energy Research and Applications (ICRERA)*, pages 779–784.

Deneubourg, J.-L. and Goss, S. (1989). Collective patterns and decision-making. *Ethology Ecology & Evolution*, 1(4):295–311.

Deneubourg, J.-L., Pasteels, J. M., and Verhaeghe, J.-C. (1983). Probabilistic behaviour in ants: a strategy of errors? *Journal of theoretical Biology*, 105(2):259–271.

Dharageshwari, K. and Nayanatara, C. (2015). Multiobjective optimal placement of multiple distributed generations in ieee 33 bus radial system using simulated annealing. In *2015 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2015]*, pages 1–7. IEEE.

Dorigo, M., Caro, G. D., and Gambardella, L. M. (1999). Ant algorithms for discrete optimization. *Artificial life*, 5(2):137–172.

Dorigo, M., Maniezzo, V., and Colorni, A. (1996). Ant system: optimization by a colony of cooperating agents. *IEEE Transactions on Systems, Man, and Cybernetics, Part B (Cybernetics)*, 26(1):29–41.

Hussain, S. S. and Subbaramiah, M. (2013). An analytical approach for optimal location of dstatcom in radial distribution system. In *2013 International Conference on Energy Efficient Technologies for Sustainability*, pages 1365–1369. IEEE.

Jain, A., Gupta, A., and Kumar, A. (2014). An efficient method for d-statcom placement in radial distribution system. In *2014 IEEE 6th India International Conference on Power Electronics (IICPE)*, pages 1–6. IEEE.

Jayawardena, A., Meegahapola, L. G., Robinson, D. A., and Perera, S. (2015). Low-voltage ride-through characteristics of microgrids with distribution static synchronous compensator (dstatcom). In *2015 Australasian Universities Power Engineering Conference (AUPEC)*, pages 1–6. IEEE.

Kannan, V. K. and Rengarajan, N. (2012). Photovoltaic based distribution static compensator for power quality improvement. *International Journal of Electrical Power & Energy Systems*, 42(1):685–692.

Kumar, C. and Mishra, M. K. (2013). A multifunctional dstatcom operating under stiff source. *IEEE Transactions on Industrial Electronics*, 61(7):3131–3136.

Kumar, C. and Mishra, M. K. (2014a). An improved hybrid dstatcom topology to compensate reactive and nonlinear loads. *IEEE transactions on Industrial Electronics*, 61(12):6517–6527.

Kumar, C. and Mishra, M. K. (2014b). A voltage-controlled dstatcom for power-quality improvement. *IEEE transactions on power delivery*, 29(3):1499–1507.

Kumar, P. M., Sumanth, Y., and Ganesh, S. (2010). Improving the power quality by mlci type dstatcom. *International Journal of Computer Applications*, 975:8887.

Lei, E., Yin, X., Zhang, Z., and Chen, Y. (2017). An improved transformer winding tap injection dstatcom topology for medium-voltage reactive power compensation. *IEEE Transactions on Power Electronics*, 33(3):2113–2126.

Lenhart, S. and Workman, J. T. (2007). *Optimal control applied to biological models*. CRC press.

Mahela, O. P. and Shaik, A. G. (2016). Power quality improvement in distribution network using dstatcom with battery energy storage system. *International Journal of Electrical Power & Energy Systems*, 83:229–240.

Mangaraj, M. and Panda, A. K. (2018). Dstatcom deploying cgbp based icos ϕ neural network technique for power conditioning. *Ain Shams Engineering Journal*, 9(4):1535–1546.

Mishra, M. K., Ghosh, A., and Joshi, A. (2003). Operation of a dstatcom in voltage control mode. *IEEE transactions on power delivery*, 18(1):258–264.

Padiyar, K. (2007). *FACTS controllers in power transmission and distribution*. New Age International.

Rao, R. S. and Narasimham, S. (2008). Optimal capacitor placement in a radial distribution system using plant growth simulation algorithm. *World Academy of Science, Engineering and Technology*, 45(120):715–722.

Rao, R. S., Narasimham, S. V. L., Raju, M. R., and Rao, A. S. (2010). Optimal network reconfiguration of large-scale distribution system using harmony search algorithm. *IEEE Transactions on power systems*, 26(3):1080–1088.

Singh, B., Dube, S. K., and Arya, S. R. (2015). An improved control algorithm of dstatcom for power quality improvement. *International Journal of Electrical Power & Energy Systems*, 64:493–504.

Singh, B., Jayaprakash, P., Kothari, D. P., Chandra, A., and Al Haddad, K. (2014). Comprehensive study of dstatcom configurations. *IEEE Transactions on Industrial Informatics*, 10(2):854–870.

Singh, B., Jayaprakash, P., Kumar, S., and Kothari, D. P. (2011). Implementation of neural-network-controlled three-leg vsc and a transformer as three-phase four-wire dstatcom. *IEEE transactions on industry applications*, 47(4):1892–1901.

Su, C.-T., Chang, C.-F., and Chiou, J.-P. (2005). Distribution network reconfiguration for loss reduction by ant colony search algorithm. *Electric Power Systems Research*, 75(2-3):190–199.

Sundarabalan, C. and Selvi, K. (2014). Pem fuel cell supported distribution static compensator for power quality enhancement in three-phase four-wire distribution system. *International journal of hydrogen energy*, 39(33):19051–19066.

Thirupathaiah, M. (2018). Enhancement of power quality in wind power distribution system by using hybrid pso-firefly based dstatcom. *International Journal of Renewable Energy Research (IJRER)*, 8(2):1138–1154.

Wang, Y., Xie, L., and De Souza, C. E. (1992). Robust control of a class of uncertain nonlinear systems. *Systems & control letters*, 19(2):139–149.

Woei-Luen Chen and Yuan-Yih Hsu (2003). Direct output voltage control of a static synchronous compensator using current sensorless d-q vector-based power balancing scheme. In *2003 IEEE PES Transmission and Distribution Conference and Exposition (IEEE Cat. No.03CH37495)*, volume 2, pages 545–549 vol.2.

Publications Based on The Research Work

Refereed Journal Publications

1. **Sanath Saralaya**. and K. Manjunatha Sharma. (2019) 'An improved voltage controller for Distribution Static Compensator', *International Journal of Renewable Energy Research*,vol. 9, no. 1, pp. 393-400.

2. **Sanath Saralaya**. and K Manjunatha Sharma. (2018) 'An improved control strategy without current sensors for DSTATCOM', *International Journal of Power Electronics,*,vol. 9, no. 2, pp.214–228.

3. **Sanath Saralaya**. and K Manjunatha Sharma. (2016) 'Performance Analysis of Distribution Static Compensator for Power Quality Perspective', *The Journal of CPRI*,vol. 12, no. 1, pp. 51-58.

Refereed Papers in Conference Proceedings

1. **Sanath Saralaya** and K Manjunatha Sharma. 'Optimal Sizing, Placement and Performance Analysis of DSTATCOM with Improved Controller without Current Sensors', *Proceedings of the 3021 International Symposium on Devices, Circuits and Systems (ISDCS)*, Hiroshima, Japan, 2021, pp. 1-4, doi: 10.1109/ISDCS52006.2021.9397892.

2. **Sanath Saralaya** and K Manjunatha Sharma. 'Investigation of Performance of DSTATCOM with Improved Current Sensorless Controller', *Proceedings of the 3rd IEEE International Conference on RTEICT*, Bengaluru, India, 2018, pp. 1786-1790.

3. **Sanath Saralaya** and K Manjunatha Sharma. 'Performance Analysis of Three Leg DSTATCOM Under Distributed Geneartion and Fault Scenario', *Proceedings of the 3rd IEEE International Conference on AEEICB*, Chennai, India, 2017, pp. 222-226.

4. **Sanath Saralaya** and K Manjunatha Sharma. Performance Analysis of Distribution Static Compensator', *Poster presentation at National conference on Recent Trends in Power Engineering*, Chennai, 2016.

Bio-data

Name: Sanath Saralaya
Date of birth: 23-03-1988
Marital status: Married
E-mail:sanathėe13f05@nitk.edu.in, sanathsaralaya@gmail.com
Mobile:+91-9743080918

Permanent Address
S/o: Krishna
Kayarthimar House
Adoor Village, Urdur Post
Kasaragod District
Kerala, 671543, India.

Education Qualification

- **Ph.D.** in Electrical and Electronics Engineering (Pursuing)
  Institute: National Institute of Technology Karnataka (Deemed University), Surathkal
- **M.Tech.** in Power Electronic Systems and Control (2011)
  Institute: Manipal Institute of Technology, Manipal
  University: Manipal University
  CGPA: 9.28
- **B.E.** in Electrical and Electronics Engineering (2009)
  Institute: K V G college of engineering, Sullia
  University: Visvesvaraya Technological University, Belagavi
  Percentage: 80.2