DESIGN OF ENERGY EFFICIENT, VARIABLE RESOLUTION, HYBRID ANALOG TO DIGITAL CONVERTERS FOR LOW FREQUENCY APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by

SREENIVASULU POLINENI

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA
SURATHKAL, MANGALORE -575025

September 2021

DECLARATION

I hereby ***declare*** that the Research Thesis entitled **DESIGN OF ENERGY EFFICIENT, VARIABLE RESOLUTION, HYBRID ANALOG TO DIGITAL CONVERTERS FOR LOW FREQUENCY APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this research Thesis has not been submitted to any University or Institution for the award of any degree.

SREENIVASULU POLINENI
Reg. No. 155080 EC15FV04
Department of Electronics and
Communication Engineering.

Place: NITK Surathkal.
Date : 03/09/2021.

CERTIFICATE

This is to certify that the Research Thesis entitled **DESIGN OF ENERGY EFFICIENT, VARIABLE RESOLUTION, HYBRID ANALOG TO DIGITAL CONVERTERS FOR LOW FREQUENCY APPLICATIONS** submitted by **SREENIVASULU POLINENI** (Register Number: EC15FV04) as the record of the research work carried out by him, is accepted as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

Prof. M. S. Bhat
Reserach Supervisor
Professor
Dept. of E&C Engg.
NITK Surathkal - 575025.

Dr. Rekha S.
Reserach Supervisor
Assistant Professor
Dept. of E&C Engg.
NITK Surathkal - 575025.

Chairman-DRPC
(Signature with Date and Seal)

Acknowledgements

Firstly, I would like to express my sincere gratitude and deep regards to my research advisors Prof. M. S. Bhat and Dr. Rekha S. for their constant guidance and support provided throughout the course of this research work. Their patience, motivation and immense knowledge made me to accomplish this. I owe my deepest gratitude to them, also for bringing this thesis in the present form. I could not have imagined having better advisors for my Ph.D.

Beside my advisors, I express my gratitude to Dr. M. R. Arulalan, one of my advisors during my enrollment for Ph.D. program for his help and invaluable suggestions throughout the course of research work. I extend my heartfelt gratitude to Prof. Ashvini Chaturvedi, Head, ECE Dept., for his support and help. My sincere thanks to Prof. Laxminidhi T., for his technical advice and constant support through out my research. Also, I thank Prof. U. Shripathi Acharya, Head, Dept. of ECE, during my research work for his support and help. My sincere thanks to RPAC members, Dr. Rathnamala Rao, Dept. of ECE, Dr. Dattatraya N Gaonkar, Dept. of E&E Engg. and Dr. Sheron Figarado, Dept. of E&E Engg., for their invaluable suggestions during every step of my progress in the research work. I thank the journal and conference reviewers for their valuable suggestions in improving the quality of research work. I express my sincere gratitude to the thesis examiners for their valuable suggestions to improve the thesis. I extend my sincere gratitude to the DTAC panel members for valuable suggestions. Also, I express my deepest gratitude to Prof. T. Kishore Kumar, Dept. of ECE, NIT Warangal, for examining the thesis defence seminar.

I take this opportunity to thank Dr. Ramesh Kini for his help during my course work and also for helping me with cadence tools. I am very grateful to Mr. Thilak for maintaining servers in VLSI lab. I also take this opportunity to thank all the faculty and staff of ECE department, NITK Surathkal. I also thank the staff in Academic, Admission and Cash sections of NITK for their assistance. My sincere thanks to my course work instructors Prof. Laxminidhi T., Dr. Ramesh Kini, Dr. Rekaha S. and A.V. Narasimhadhan. Also, I thank Prof. A. H. Sequeria for teaching research methodology course.

I would like to express my gratitude to all friends and colleagues at NITK for encouraging me in good and bad times making a memorable stay in NITK. Thanks to Jagadish D. N., Jayaram Reddy MK, Yajunath Kaliyath, Deepu S. P. and Kalpana Bhat for their support and help. Special thanks to my labmates, Kiran Kumar Lad and Gottam Hanumantha Rao for their help in circuit designing and in solving tool related issues. I would like to thank research premier league (RPL) founders and organizers which helped scholars to interact across departments. I thank all of my team members who contributed to won the RPL tournament in successive years(2015-17). I express my sincere gratitude to Dr. Deepu Vijayasenan who inspired and trained me to run a half marathon. I thank my cycling companions Reddy Prasad, Yajunath, Ramu, Venkataramana (JV), Raviteja. I thank my trekking partners Dr. Raghavendra Bobbi S. and Reddy Prasad who helped me to refresh in western ghats of India. Also, I thank Gowtham, Raghavendra, Shareef Babu, Prasad Naik, Shrutakirti, Lakshmi Poola, Balaram, Srinath, Srikanth.

I would like to thank Ministry of Electronics and Information Technology (MeitY), Govt. of India, for providing EDA tools support under SMDP-VLSI project. Also, I express my gratitude to MeitY, for providing financial assistance under Visvesvaraya PhD Scheme for Electronics & IT (funded by Digital India Corporation).

My heartfelt thanks to my lovely parents Venkateswarlu and Seshamma for their endless support and help throughout. I recall with immense gratitude the unconditional love and support rendered by my family members and friends in my education and in my career throughout.

I am deeply indebted to all my teachers throughout the life, who have guided, encouraged and inspired me to grow in both technical and personal aspects. Finally, I would like to thank God for giving me good health, strength and bliss during my research work. I would like to dedicate this thesis to my parents and family as a token of love and gratitude.

Dedicated to

My Dear Parents & Family

Abstract

The advancements in digital technologies made signal processing much easier and provide complex functionalities. The analog to digital converter (ADC) helps to convert the real time data obtained through sensors into digital data. The power consumed by these sensor nodes should be as low as possible in order to improve the battery life. Thus, this research mainly focuses on the design techniques, methodologies, and circuit topologies of ADC with emphasis on minimization of energy consumption and area.

Initially, a fully differential most significant bit (MSB) capacitor splitting switching technique for binary weighted capacitive digital to analog converter (DAC) in successive approximation register (SAR) ADC is proposed to reduce the energy consumption and area. Also, with this switching technique, one can achieve the same dynamic range as the conventional one, with half of the supply voltage as compared to the existing techniques. This makes the proposed switching method suitable for ultra low voltage SAR ADCs, which are widely used in biomedical applications. The proposed method is modelled in MATLAB. The results show that the proposed switching technique reduces energy consumption of DAC by 97 % and the capacitance area by 50 % over the conventional one. The circuit level implementation of 10-bit SAR ADC is simulated in UMC 90 nm CMOS 1P9M process technology with a supply voltage of $0.5\,V$. It achieved signal to noise and distortion ratio (SNDR) of 55.93 dB, spurious free dynamic range (SFDR) of 77.17 dB. The Walden figure of merit (FoMW) is calculated as 38.67 fJ/conv.

Furthermore, this research presents a switched capacitor based SAR ADC using a passive reference charge sharing and charge accumulation. For N-bit resolution, the fully differential version of this architecture needs only 6 capacitors, which is a significant improvement over conventional binary weighted SAR ADC. The proposed SAR ADC is designed and laid out in UMC 180 nm 1P6M CMOS technology with a supply voltage of $1.8\,V$ for a target resolution of 11 bit. The total design occupies an area of $568\,\mu m$ x $298\,\mu m$ and consumes a power as less as $0.28\,\mu$W. It is found that the integral non-linearity (INL) and differential non-linearity (DNL) of this

ADC are in the range +0.35/-0.84 least significant bit (LSB) and +0.1/-0.6 LSB, respectively. In addition, dynamic performance test shows that the proposed SAR ADC offers an effective number of bits (ENoB) of 10.14 and FoMW of 0.12 pJ/conv-step.

Finally, a novel switched capacitor integrator based variable resolution hybrid ADC architecture is proposed. The ADC resolution is programmable from 8-15 bit using a 3- bit control bus ($res[2:0]$). It operates in SAR mode for 8-11 bit resolutions and as the first-order delta sigma modulator (DSM) with a multi-bit quantizer in 12-15 bit resolutions. A mathematical relationship showing the effect of mismatch of capacitors on ADC linearity is derived. A fully differential folded cascode (FC) OTA is designed with programmable unity gain bandwidth (UGB) and slew rate. The proposed ADC, designed and laid out in UMC 180 nm standard CMOS technology with a supply voltage of $1.8\,V$, occupies an area of $0.228\,mm^2$. It exhibits SNDR of 45–86 dB and consumes a power of 0.86–98 μW across target resolutions (8–15 bits).

Keywords: Analog to Digital Converter (ADC); Binary weighted DAC; Biomedical; Folded Cascode Operational Transconductance Amplifier (FC OTA); Successive Approximation Register (SAR); Switched Capacitor Integrator; Variable Resolution; Delta Sigma Modulation (DSM);

Contents

List of Figures

List of Tables

Abbreviations

ADC	Analog to Digital Converter
CAD	Computer Aided Design
CMFB	Common Mode Feedback
CMOS	Complementary Metal–Oxide–Semiconductor
CRP	C-reactive protein
DAC	Digital to Analog Converter
DACP	DAC connected to the positive terminal of comparator
DACN	DAC connected to the negative terminal of comparator
DNL	Differential Non-Linearity
DR	Dynamic Range
DSM	Delta Sigma Modulator
DSP	Digital Signal Processor
ECG	Electrocardiogram
EDA	Electronic Design Automation
EEG	Electroencephalogram
EoC	End of Conversion
ENoB	Effective Number of Bits
ESR	Erythrocyte Sedimentation Rate
FC	Folded Cascode
FF	Flip Flop
ff	fast NMOS fast PMOS
FFT	Fast Fourier Transform
fnsp	fast NMOS slow PMOS
FoM	Figure of Merit
FoMS	Figure of Merit by Schreier
FoMW	Figure of Merit by Walden
FPGA	Field Programmable Gate Array

FS	Full Signal swing
fs	fast NMOS and slow PMOS
GSPs	Giga Samples per Second
HDL	Hardware Description Language
IC	Integrated Circuit
INL	Integral Non-Linearity
LDO	Low drop-Out regulator
LSB	Least Significant Bit
MCS	Merged Capacitor Switching
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal–Oxide–Semiconductor
MSB	Most Significant Bit
MSPs	Mega Samples per second
NMOS	n-channel Metal–Oxide–Semiconductor
NTF	Noise Transfer Function
OSR	Over Sampling Ratio
OTA	Operational Transconductance Amplifier
PADC	Programmable resolution ADC
PIP	polysilicon-insulator-polysilicon
PIPO	Parallel In Parallel Out
PMOS	p-channel Metal–Oxide–Semiconductor
PSD	Power Spectral Density
PVT	Process, Voltage and Temperature
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
sf	slow NMOS and fast PMOS
S/H	Sample and Hold

SIPO	Serial In Parallel Out
SINAD	Signal to Noise and Distortion
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio
snfp	slow NMOS fast PMOS
ss	slow NMOS slow PMOS
STF	Signal Transfer Function
TH	Track and Hold
THD	Total Harmonic Distortion
tt	Typical NMOS Typical PMOS
UGB	Unity Gain Bandwidth
UMC	United Microelectronics Corporation
WBSN	Wireless Body Sensor Network
1P6M	1 Poly and 6 Metal
1P9M	1 Poly and 9 Metal

Notations

T	Absolute temperature
N	ADC Resolution
Ω	Angular frequency
k	Boltzmann constant
C	Capacitor
q	Charge
L	Channel length of the MOSFET
W	Channel width of the MOSFET
clk	Clock signal
f_{clk}	Clock signal frequency
V_{cm}	Common mode voltage
dB	Decibel
dBc	Decibels with respect to carrier
^oC	degree Celsius
Δ	Difference
V_{ip}, V_{im}	Differential input signals
D_i	i^{th} digital bit
Gnd	Ground *
f_{in}	Input signal frequency
f_{inB}	Input signal frequency Bandwidth
V_{in}	Input voltage signal
μ	Mean
β	MOS transistor current factor
α	Normalized deviation of capacitor
f_{nyq}	Nyquist frequency
V_{op}, V_{om}	OTA differential output signals
Q	Quantization noise

V_{ref}	Reference voltage
R	Resistor
f_s	Sampling frequency
σ	Standard deviation
V_{dd}	Supply voltage
S	Switch
E	Switching energy
V_{th}	Threshold voltage of the MOSFET
τ	Time constant
T_{clk}	Time period of clock signal
σ_q^2	Total quantization noise power
g_m	Transconductance of MOS transistor
V	Volts

Chapter 1

INTRODUCTION

1.1 Motivation

The 21^{st} century is marked as digital era by electronic industries which brought revolution in all walks of life through digital technologies. The modern electronic systems employ sophisticated functional blocks which make analog circuit design more complex. This impacts power consumption and cost, performance and reliability of the system. Digital Signal Processor (DSP) is one such system that leveraged the benefits of digital technologies to implement complex algorithms and functions with high computational power and accuracy. This, along with the improved noise margin, error detecting and correcting codes made the transmission and storage of digital signals less prone to noise. Hence the analog circuit techniques in many applications were replaced by reliable, cost effective, fast and flexible digital technologies.

The evolution of complementary metal–oxide–semiconductor (CMOS) fabrication technology has resulted in improved performance, power efficiency and the integration density of digital systems at a tremendous rate as anticipated by Moore's law. However, technology scaling has not benefited analog circuits to the same extent. Moreover, features like hardware description languages (HDLs), synthesis, automatic layout generation using standard cell libraries and place and route algorithms availed in computer aided design (CAD) tools and testability using field programmable gate arrays (FPGAs) made the digital system design easy. Coupled with this, a robust and systematic digital logic design flow using electronic design automation (EDA) tools has helped to speed up the product design, debugging and testing processes leading to quicker time to market. All these qualities of digital technologies shifted most of

the signal processing functions into digital domain while restricting analog circuits for amplification, filtering and supply references.

Basically the world is analog in nature i.e. continuous in time and amplitude. Thus there is a need for analog to digital converters (ADCs) and digital to analog converters (DACs) to avail benefits of digital signal processing. A typical block diagram of the present day electronic system is shown in figure 1.1. The sensor transforms a physical signal into electrical signal. The amplification and filtering are carried out in analog signal conditioning block. The ADC block digitizes the analog signal. DSP block performs required functionality on digital signal and the output of DSP block is converted back to analog signal by DAC. The actuator transforms/ feeds this analog signal to outside world. Here, the overall system accuracy depends on the accuracy of each block.

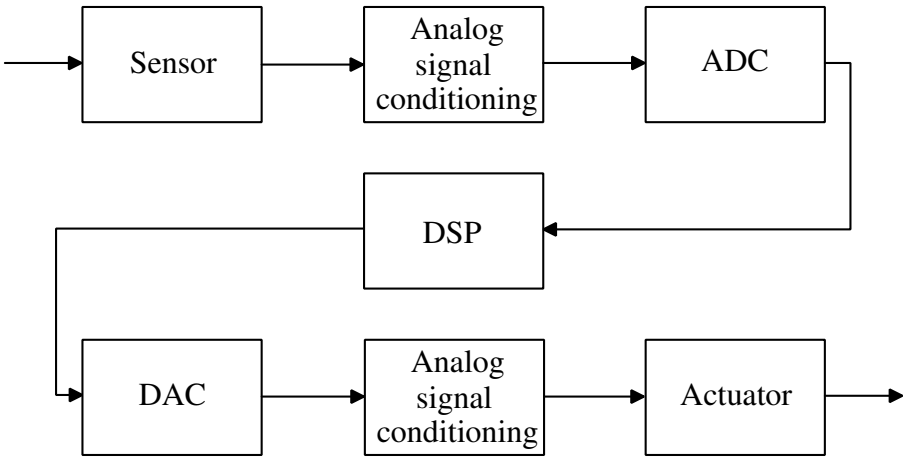
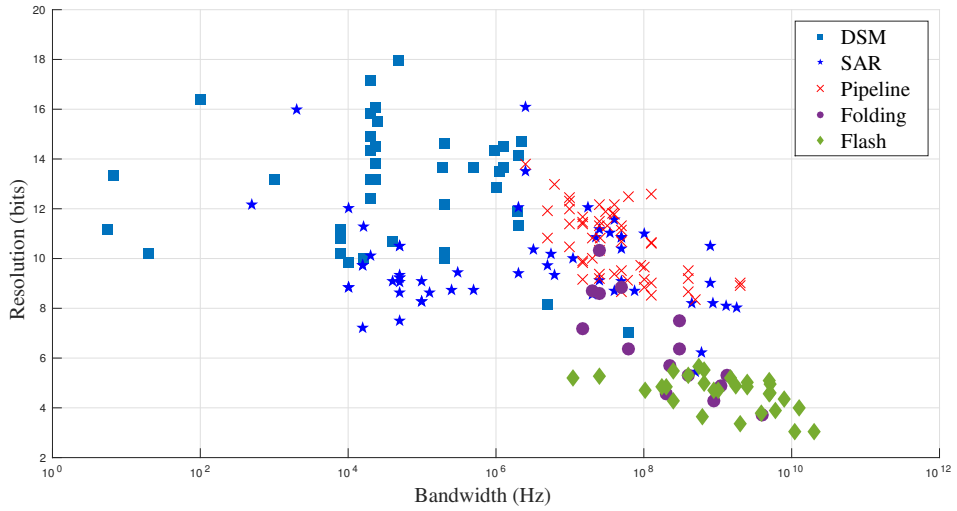


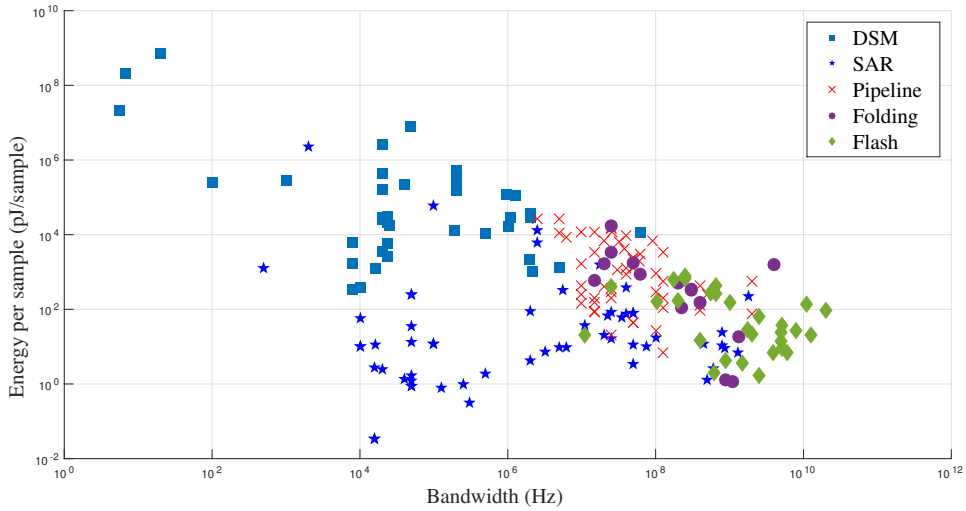
Figure 1.1: A typical block diagram of the present day electronic system.

1.2 Overview of ADC

Sampler and quantizer are the basic building blocks of ADC. Sampler produces a discrete signal at a rate, not less than Nyquist rate. Quantizer rounds off those discrete signals to the nearest quantization levels and gives out the equivalent digital values. A large variety of ADC architectures have been reported in the literature which have trade-offs between speed, resolution and power efficiency. Figure 1.2a illustrates the trade-off between resolution and bandwidth. As can be seen, the resolution of ADC decreases as bandwidth increases.



(a)



(b)

Figure 1.2: (a) Resolution versus Input frequency of ADCs (b) Energy consumption per conversion versus Input frequency of ADCs (Murmann *et al.* 2016).

Among the various ADC architectures, flash ADCs are the fastest as they compare the input with all reference levels simultaneously. However, for each bit increase, the number of comparators increases by a factor of 2. This leads to increased input capacitance and kickback noise that affect the accuracy of reference levels. As a result, the resolution of flash ADCs is limited to 6-bits. However, the resolution can

Table 1.1: A brief comparison of different ADC architectures (Çikan and Aksoy 2016).

	Flash ADC	Pipeline ADC	SAR ADC	DSM ADC
Conversion Principle	Uses 2^N-1 comparators to compare input signal with references.	Small parallel structure, each stage works on one to a few bits	Binary search algorithm	Oversampling and Noise shaping
Encoding Method	Thermometer Code	Digital Correction Logic	Successive Approximation	Decimation Filter
Sampling rates	up to 1ĠSPs	$\leq$ 500 MSPs	$\leq$ 3 MSPs	$\leq$ 10 MSPs
Resolution (bits)	6–8	10–14	8–18	16–24
Power Consumption	High	High	Low	Moderate
Area	Large	Medium	Low	Medium
Cost	High	High	Low	Moderate

be slightly improved by employing interleaving and folding techniques.

The pipelined ADCs achieve moderate resolution at the cost of longer conversion time. In this, the analog signal is quantized coarsely by each stage and the residue is sampled by the next stage. Although, the number of comparators required is reduced, additional blocks like summing amplifiers increase the power consumption.

The successive approximation register (SAR) ADC is widely used in energy efficient applications, as shown in figure 1.2b. However, the resolution of SAR ADC is restricted by circuit noise. Thus SAR ADCs operate at moderate speeds with low to medium resolutions (8-bit to 18-bit).

Delta sigma modulator (DSM) ADCs attain high resolution ($\geq$ 20-bits) by employing oversampling and noise shaping techniques. Oversampling makes the internal elements of DSM ADC operate at faster rates, resulting in an increase in power consumption. A brief comparison of different ADC architectures is given in Table 1.1.

The performance and accuracy of overall system are restricted by the speed and noise floor of data converters (ADC and DAC). The design of ADCs for low frequency applications is the objective of this research. The key design challenges of these ADCs are discussed here.

- The energy consumption of each building block of the system should be minimized as much as possible in order to improve the battery life of portable battery operated devices. Thus it is imperative to design low power and area efficient ADCs in such systems.

- SAR ADC is well suited for moderate resolution and energy efficient applications with their simple architecture. The feedback DAC in SAR ADC occupies large area because of the exponential relation between capacitor spread and resolution of ADC. Also, the switches used in this DAC cause distortion and reduce accuracy of ADC.

- The DSM ADCs are quite popular in achieving higher resolutions using low resolution quantizers by employing oversampling and noise shaping techniques. The power consumption is one of the main limitations of DSM ADCs due to their high sampling speeds.

- Biomedical signals such as the electroencephalogram (EEG), electrocardiogram (ECG), breathing quality, measures of blood parameters such as oxygenation, glucose, cholesterol, c-reactive protein (CRP), erythrocyte sedimentation rate (ESR), platelet count etc., have varying dynamic range and bandwidth. A variable resolution ADC would be required to optimize energy consumption at different intervals based on signal activity.

Designing ADCs with desired performance parameters, under the influence of above mentioned issues is quite challenging. Any further advancements in the design of ADCs either in terms of power consumption, signal to noise and distortion ratio (SNDR) or area efficiency can be a significant contribution to the field of mixed signal integrated circuit design. This research is the result of attempts to improve ADC designs in this direction.

1.2.1 Successive Approximation Register (SAR) ADC

SAR ADC detects an equivalent digital output of a sampled signal using binary search algorithm (Baker 2008*a*). In general, a binary search algorithm is used to detect position of a number from an array of sorted numbers. Initially, the target value is compared with middle number of array and then the output of comparator decides

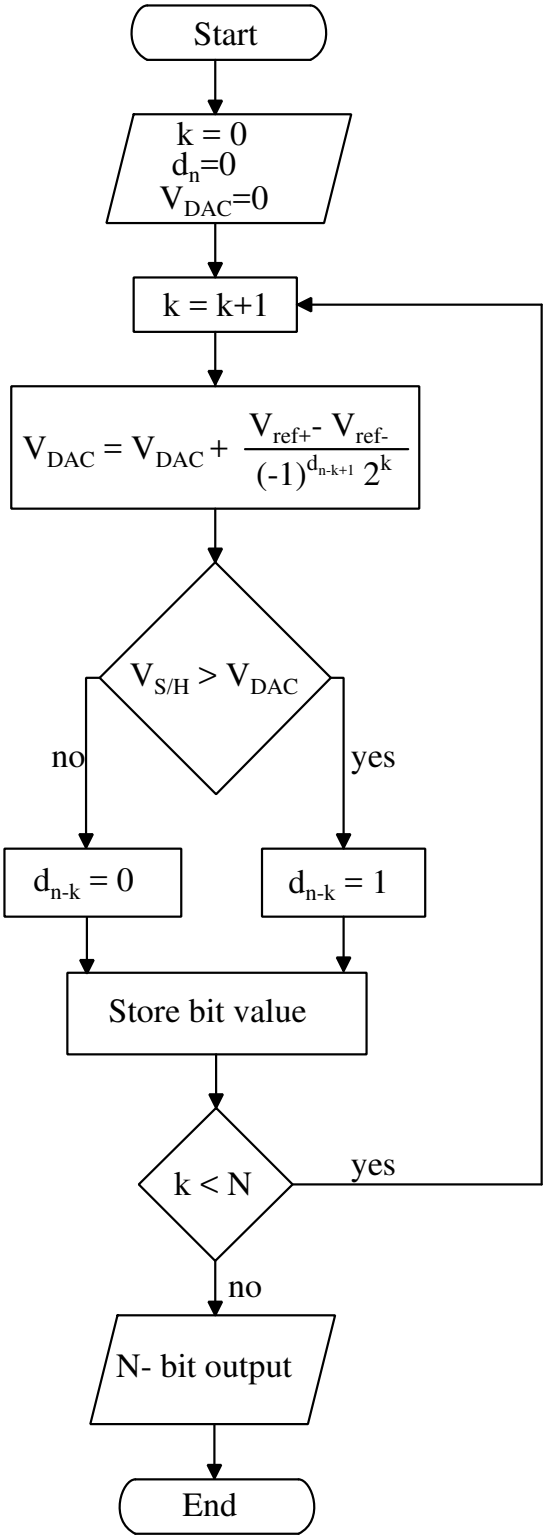


Figure 1.3: Flow chart showing SAR ADC operation.

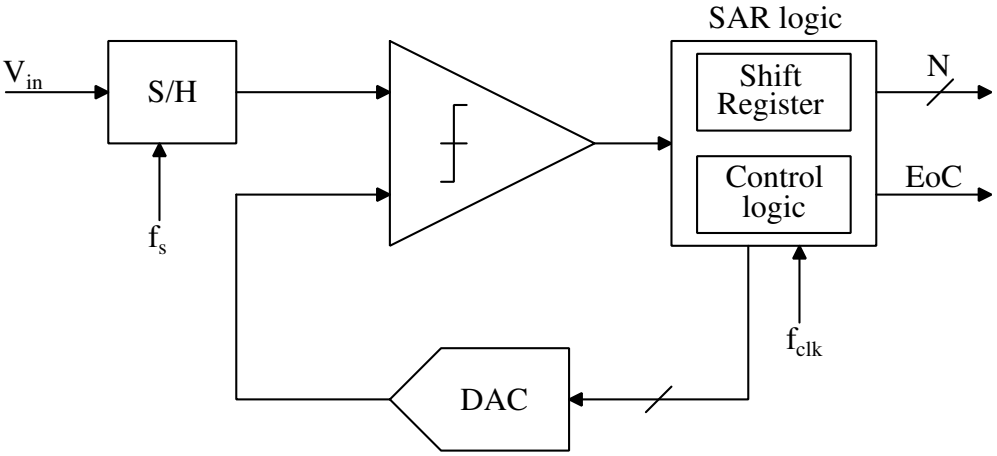


Figure 1.4: SAR ADC block diagram.

which half has to be considered for next comparison. This search continues until successful detection or array size becomes zero. If the array size is N, then $log_2(N)$ comparisons take place in binary search. In SAR ADC, the number of reference levels reflect the array size. The sampled input is approximated to nearest reference level by the search algorithm. SAR ADC is named so because of successive determination of digital output from most significant bit (MSB) to least significant bit (LSB) by comparison with reference levels and employs a shift register to store bits serially till the end of conversion. The reference levels used in comparisons are generated through a feedback DAC. The working of a SAR ADC is depicted through the flow chart shown in figure 1.3.

In general, a typical SAR ADC is implemented using only three main blocks, as shown in figure 1.4. The comparison in each cycle is performed by comparator and its output is processed by SAR logic. It controls timing of all blocks and determines next reference level which is fed back through DAC. The comparator and SAR logic blocks are simple, adaptive to technology scaling and also consume less energy. Thus, most research efforts and explorations focus on improving the performance of DAC.

1.2.2 Delta Sigma Modulator (DSM) ADCs

DSM ADCs achieve a higher resolution by taking advantage of oversampling, noise shaping and decimation filter. This ADC operation can be interpreted easily by using spectrum analysis. Bennett's criteria says that the total quantization noise power (σ_q^2) introduced by ADC is spread all over in spectrum. Thus, the power spectral density

of noise is inversely proportional to the sampling frequency $\left(\sigma_q^2/f_s\right)$. Hence, oversampling followed by low pass filtering reduces the total noise power. This phenomenon improves the signal to noise ratio (SNR) which leads to increase in effective number of bits (ENoB). The ratio of sampling frequency to Nyquist frequency is known as over sampling ratio (OSR). Equation (1.2) illustrates that, a 3 dB improvement in SNR can be achieved by doubling OSR (Baker 2008*b*, Schreier *et al.* 2005).

$$OSR = \frac{f_s}{2f_{in}}$$

$$Q_{in-band}^2 = \int_{-f_{in}}^{f_{in}} \frac{\sigma_q^2}{f_s}\, df = \frac{\sigma_q^2}{OSR} \tag{1.1}$$

$$SNR_{dB} = 6.02N + 1.76 + 10\log_{10}(OSR) \tag{1.2}$$

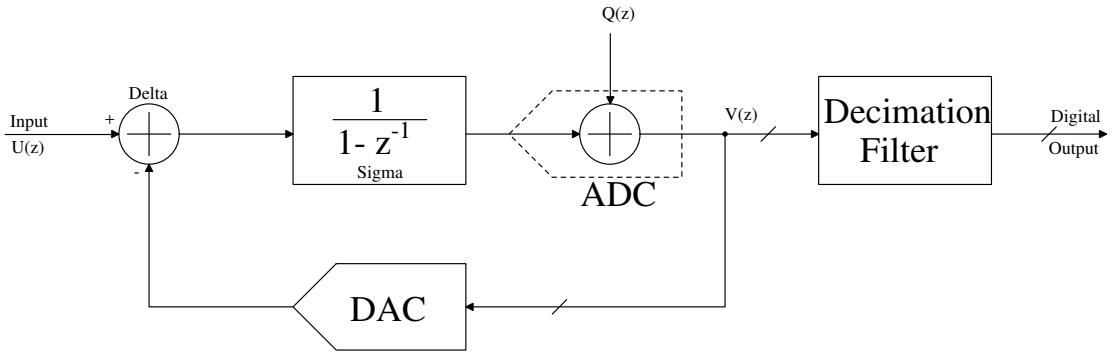


Figure 1.5: 1^{st} order DSM ADC block diagram.

For further improvement in SNR, the noise is shifted from input signal bandwidth to higher frequencies using feedback technique. This phenomenon is known as noise shaping. Figure 1.5 shows the block diagram of first order DSM. The derivations for signal transfer function (STF) and noise transfer function (NTF) are as follows.

$$V(z) = (U(z) - z^{-1}V(z))\frac{1}{1-z^{-1}} + Q(z) \tag{1.3}$$

$$V(z) - z^{-1}V(z) = U(z) - z^{-1}V(z) + (1-z^{-1})Q(z)$$

$$V(z) = U(z) + (1-z^{-1})Q(z) \tag{1.4}$$

From equation (1.4), it can be seen that, STF=1 and NTF=$(1 - z^{-1})$

$$\begin{aligned} |NTF|^2 &= |1 - z^{-1}|^2 = |1 - e^{-j\Omega}|^2 = |1 - \cos\Omega + j\sin\Omega|^2 \\ &= (1 - \cos\Omega)^2 + \sin^2\Omega = 2 - 2\cos\Omega \\ |NTF|^2 &= 2\sin^2\frac{\Omega}{2} \end{aligned} \tag{1.5}$$

where $\Omega = 2\pi\dfrac{f}{f_s}$, is known as normalized angular frequency. Figure 1.6 shows the pictorial representation of noise power spectral density. The ratio of signal power to total noise power within signal bandwidth is called as in-band SNR. The total in-band noise power and SNR are calculated as follows.

$$\begin{aligned} Q^2_{in-band} &= \int_{-\frac{\pi}{OSR}}^{\frac{\pi}{OSR}} \frac{\sigma_q^2}{2\pi}|NTF|^2\, d\Omega \qquad (1.6) \\ &= \int_{-\frac{\pi}{OSR}}^{\frac{\pi}{OSR}} \frac{\sigma_q^2}{2\pi} 2\sin^2\frac{\Omega}{2}\, d\Omega \\ &= \int_{-\frac{\pi}{OSR}}^{\frac{\pi}{OSR}} \frac{\sigma_q^2}{2\pi}\,\Omega^2\, d\Omega \qquad (\because 2\sin\frac{\Omega}{2} \approx \Omega \quad for \quad \Omega << \pi) \\ Q^2_{in-band} &= \frac{\sigma_q^2\pi^2}{3\ OSR^3} \qquad (1.7) \\ SNR_{dB} &= 6.02N\ +\ 1.76\ + 30\log_{10}(OSR) - 10\log_{10}\left(\frac{\pi^2}{3}\right) \qquad (1.8) \end{aligned}$$

Equation (1.8) shows that there is 9 dB improvement in SNR for every doubling of OSR which results in the increase in ENOB by 1.5 bits. Further, more noise shaping can be achieved by increasing the order of NTF.

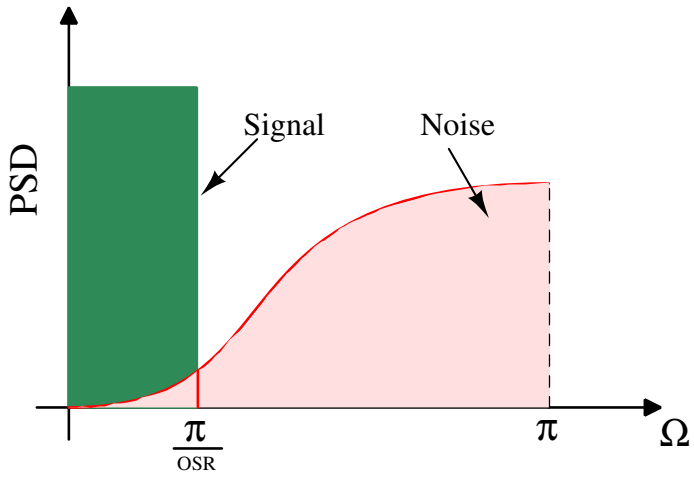


Figure 1.6: DSM ADC spectrum response.

1.3 Prior Work

1.3.1 Conventional SAR ADC architectures

SAR ADC is well suited for moderate resolution and energy efficient applications as discussed earlier. The accuracy and power consumption of SAR ADCs are limited by the DAC. The quality and area of capacitor used in the DAC is improved by the evolution of CMOS technology. Along with this, the techniques such as capacitance calibration and trimming make the charge redistribution and charge sharing based capacitive DACs popular in terms of power consumption and control logic complexity.

McCreary and Gray (1975) introduced binary weighted capacitor array DAC with charge redistribution technique for the first time. All capacitors with value ranging from C to $2^{N-1}C$ are connected in parallel as shown in figure 1.7. The input voltage is sampled through bottom plates, and the resultant voltage on top plate is conserved to $-V_{in}$ in hold mode. By connecting the bottom plate of largest capacitor ($2^{N-1}C$) to V_{ref}, charge redistribution takes place and the voltage V_x becomes $-V_{in} + \frac{V_{ref}}{2}$. In this case the total energy consumed from supply voltage is $2^{N-2}CV_{ref}^2$. Next, the comparator outputs MSB, which decides next switching. If MSB is 1, the bottom plate of $2^{N-2}C$ is switched to V_{ref}. Thus, the resultant voltage V_x becomes $-V_{in}+\frac{3V_{ref}}{4}$ and the switching energy is $2^{N-4}CV_{ref}^2$. On the other hand, when MSB is 0, the bottom plates of $2^{N-2}C$ & $2^{N-1}C$ are switched to V_{ref} and Gnd respectively. In this case, the voltage V_x becomes $-V_{in} + \frac{V_{ref}}{4}$ and the switching energy is $5\left(2^{N-4}CV_{ref}^2\right)$. This

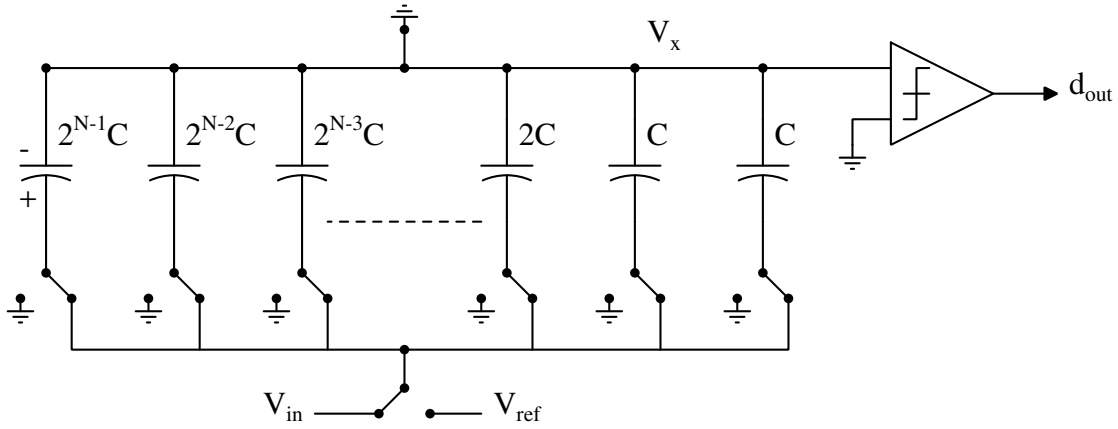


Figure 1.7: Charge redistribution Capacitive DAC in sample mode.

procedure continues till the end of conversion. The parasitic capacitance of bottom plate has no effect on accuracy of conversion while top plate causes a little offset. Differential implementation suppresses all these errors. By assuming all codes are equiprobable, the average switching energy consumed by differential binary weighted DAC is calculated as

$$\begin{aligned} E_{Conventional} &= \sum_{i=1}^{N} (2^i - 1) 2^{N+1-2i} \; CV_{ref}^2 \quad J \\ &\approx \left(\frac{2^{N+2}}{3} \right) \; CV_{ref}^2 \quad J \end{aligned} \tag{1.9}$$

Ginsburg and Chandrakasan (2005) reported three new switching techniques for differential DACs namely two step switching, charge sharing and capacitor splitting to reduce the switching energy. Among them, capacitor splitting is more efficient. In this, the largest capacitor ($2^{N-2}C$) is split into binary weighted capacitors ($2^{N-3}C$, $2^{N-4}C$, ... , $2C$, C, C). When MSB is 0, only $2^{N-3}C$ switched to Gnd which results $V_x = -V_{in} + \frac{V_{ref}}{4}$. In other case, it is similar to conventional switching. Thus, total capacitance is reduced by 50 % and the switching energy consumed for N-bit DAC is

$$\begin{aligned} E_{cap\_split} &= \left(2^{N-1} + \sum_{i=2}^{N} (2^{i-1} - 1) 2^{N+1-2i} \right) \; CV_{ref}^2 \quad J \\ &\approx \left(\frac{5}{3} \right) \; 2^{N-1} CV_{ref}^2 \quad J \end{aligned} \tag{1.10}$$

Chang *et al.* (2007) proposed energy saving switching scheme that achieved 56 % reduction in switching energy compared to the conventional one. In first two cycles, the DAC consumes less energy, compared to capacitor splitting technique.

$$\begin{aligned} E_{energy\_saving} &= \left(3\left(2^{N-3}\right) + \sum_{i=3}^{N}(2^{i-1}-1)2^{N+1-2i}\right)\ CV_{ref}^2\ \ J \\ &\approx \left(\frac{14}{3}\right)\ 2^{N-3}CV_{ref}^2\ \ J \end{aligned} \tag{1.11}$$

Liu *et al.* (2010) reported monotonic switching procedure, in which only one of differential branch works at a time. The voltage on the differential branch either continues to increase or decrease. Thus, the common mode voltage at differential ends keeps on changing from $\frac{V_{ref}}{2}$ to 0.

$$\begin{aligned} E_{monotonic} &= \sum_{i=1}^{N-1}(2^{N-2-i})\ CV_{ref}^2\ \ J \\ &\approx \left(2^{N-2}\right)CV_{ref}^2\ \ J \end{aligned} \tag{1.12}$$

Zhu *et al.* (2010) reported a $V_{cm}\left(\frac{V_{ref}}{2}\right)$ based charge recovery switching procedure, in which bottom plates of all capacitors are connected to V_{cm} instead of Gnd. It achieved 87.5 % switching energy saving compared to the conventional one.

$$\begin{aligned} E_{V_{cm}-based} &= \sum_{i=1}^{N}(2^{i-1}-1)2^{N-2i}\ CV_{ref}^2\ \ J \\ &\approx \left(\frac{2^{N-1}}{3}\right)CV_{ref}^2\ \ J \end{aligned} \tag{1.13}$$

Hariprasath *et al.* (2010) proposed merged capacitor switching scheme (MCS) which resulted in 93.4 % less energy consumption. In this, input signal is sampled on top plates while bottom plates are connected to V_{cm}. No energy is consumed during first comparison. Based on output bit $(N-1)$, the higher voltage side DAC capacitor$(2^{N-2}C)$ bottom plate is switched to Gnd and lower voltage side DAC bottom plate is switched to V_{ref}. This gives higher accuracy and energy efficiency compared

to monotonic switching scheme, at the cost of additional reference voltage.

$$\begin{aligned} E_{MCS} &= \sum_{i=1}^{N-1} (2^i - 1) 2^{N-3-2i} \; CV_{ref}^2 \quad J \\ &\approx \left(\frac{2^{N-2}}{3} \right) CV_{ref}^2 \quad J \end{aligned} \tag{1.14}$$

Yuan and Lam (2012) proposed three level switching scheme, that reduces capacitor spread by 75 % and energy by 96.89 %. The sampled differential inputs V_{ip} & V_{im} are compared directly without any switching. The output MSB bit chooses DAC to perform switching throughout conversion. In second cycle, the lower voltage side DAC bottom plates switch to V_{cm}. Thus, the first two switchings consume zero energy. Based on the output bit $(N-2)$ being 1 or 0, the capacitor $(2^{N-3}C)$ is either switch to V_{ref} or Gnd respectively. This leads to variation in common mode voltage at differential ends.

$$\begin{aligned} E_{Yuan} &= \sum_{i=1}^{N-2} (2^i - 1) 2^{N-2i-4} \; CV_{ref}^2 \quad J \\ &\approx \left(\frac{2^{N-3}}{3} \right) CV_{ref}^2 \quad J \end{aligned} \tag{1.15}$$

Sanyal and Sun (2013) reported that most of the switching energy contribution is from first few comparison cycles only. They developed a new switching scheme, which could achieve 98.4 % reduction in energy. The complexity of digital logic is increased and also common mode voltage is not constant.

$$E_{Sanyal} \approx \left(\frac{11}{8} \right) 2^{N-6} CV_{ref}^2$$

Zhu *et al.* (2013) succeeded in achieving 97.66 % energy efficiency as well as 75 % reduction in capacitance area by combining V_{cm} based and monotonic switching procedures.

$$\begin{aligned} E_{V_{cm} \; based \; monotonic} &= \sum_{i=1}^{N-2} 2^{N-i-5} \; CV_{ref}^2 \quad J \\ &\approx \left(2^{N-5}\right) CV_{ref}^2 \quad J \end{aligned} \tag{1.16}$$

Xie *et al.* (2014) proposed a hybrid switching procedure, in which zero switching energy is achieved in first three cycles. Afterwards, it follows monotonic switching procedure. Although it achieves 98.83 % energy saving and 75 % capacitance reduction compared to the conventional one, it has the same disadvantages as monotonic switching scheme.

$$\begin{aligned} E_{Hybrid} &= \sum_{i=1}^{N-3} 2^{N-i-6}\ CV_{ref}^2 \quad J \\ &\approx \left(2^{N-6}\right) CV_{ref}^2 \quad J \end{aligned} \tag{1.17}$$

Rahimi and Yavari (2014) reported a new trilevel switching method that maintains common mode voltage (V_{cm}) at differential ends. The effect of V_{cm} on accuracy of conversion is minimized, and the energy efficiency is about 93.7 %.

$$\begin{aligned} E_{New\ trilevel} &= \sum_{i=1}^{N-2} (2^i - 1) 2^{N-2i-3}\ CV_{ref}^2 \quad J \\ &\approx \left(\frac{2^{N-2}}{3}\right) CV_{ref}^2 \quad J \end{aligned} \tag{1.18}$$

Xie *et al.* (2015) proposed a new switching scheme which is same as capacitor splitting DAC structure except in the first two cycles and the last cycle. It uses V_{cm} for last switching alone so that the accuracy of SAR ADC is not affected by V_{cm}. It achieves 96.91 % energy efficiency over the conventional one but the common mode voltage varies from 0 to V_{ref}.

$$\begin{aligned} E_{Xie} &= \sum_{i=1}^{N-3} (2^i - 1) 2^{N-2i-4}\ CV_{ref}^2 \quad J \\ &\approx \left(\frac{2^{N-3}}{3}\right) CV_{ref}^2 \quad J \end{aligned} \tag{1.19}$$

Yazdani *et al.* (2015) and Yazdani *et al.* (2016) proposed two new switching schemes that achieve 97.66 % and 98.44 % energy efficiency respectively. However, the capacitor spread is reduced by 50 % only. The sampled input is divided by two because it is sampled on only half of capacitors in array. This eliminates the need for two supply

voltages and uses only V_{cm} as a supply voltage.

$$\begin{aligned} E_{Yazdani_1} &= \sum_{i=1}^{N-2} 2^{N-i-5}\, CV_{ref}^2 \quad J \\ &\approx \left(2^{N-5}\right) CV_{ref}^2 \quad J \end{aligned} \tag{1.20}$$

$$\begin{aligned} E_{Yazdani_2} &= \sum_{i=1}^{N-2} (2^i - 1) 2^{N-2i-5}\, CV_{ref}^2 \quad J \\ &\approx \left(\frac{2^{N-4}}{3}\right) CV_{ref}^2 \quad J \end{aligned} \tag{1.21}$$

Although the various switching schemes presented in literature achieve higher energy efficiency, they are not fully differential. This introduces non-linearity as well as complexity in the design of other blocks. This also increases the total power consumption of SAR ADC. This motivates us to look for energy efficient differential switching schemes for high precision SAR ADCs.

1.3.2 Noise shaping in SAR ADCs

The number of capacitors and the energy consumption are exponentially related to resolution (N-bits) of converter in binary weighted capacitor DAC. One of the most attractive architectures from energy consumption and capacitor spread perspective is the one based on charge sharing.

Initially, Suarez *et al.* (1975) proposed a serial DAC employing charge sharing technique. The design is simple, with only two capacitors and four switches as shown in figure 1.8. Initially, both capacitors C_1 and C_2 are reset to zero. Digital to analog conversion starts with LSB and then serially continues with other bits. C_1 is charged to V_{ref} or Gnd depending on whether LSB is 1 or 0 respectively. The charge is shared between C_1 and C_2 through switch S_1. In the next cycle, C_2 holds the charge and C_1 is charged to V_{ref} or Gnd. This process repeats until the conversion ends. The final voltage on capacitor C_2 is calculated as

$$V_2(N) = \sum_{i=1}^{N} \frac{2^i D_i}{2^{N+1}} V_{ref} \tag{1.22}$$

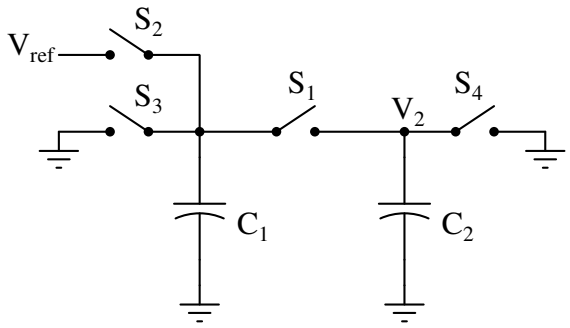


Figure 1.8: Serial DAC.

Serial DAC takes N charging cycles to convert N-bit data. In SAR ADC, MSB is determined first by setting LSB as 1. The comparator output is stored in a shift register and is subsequently used for next bit detection. The charging cycle is incremented by one for each bit detection from MSB to LSB. Thus, SAR ADC requires $\frac{N(N+1)}{2}$ clock cycles to achieve N-bit resolution. The accuracy is also affected by the parasitic capacitance of switches. This limits the use of serial DAC to moderate resolution and moderate speed applications.

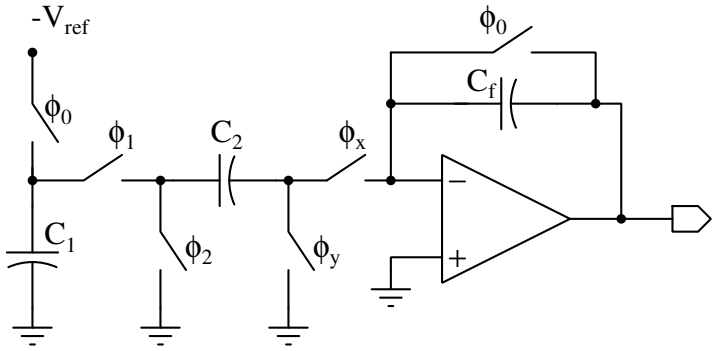


Figure 1.9: Two capacitor charge redistribution DAC.

Zheng *et al.* (1999) reported a two capacitor charge redistribution DAC based on switched capacitor integrator, as shown in figure 1.9. Initially, C_1 is charged to $-V_{ref}$, C_2 and C_f are discharged to 0. The conversion begins with MSB. In the first phase, the capacitors C_1 and C_2 involve in charge sharing through ϕ_1. If bit is 1, ϕ_x is ON such that it puts an equivalent opposite charge on C_f. If bit is 0, ϕ_y is ON instead of ϕ_x. In second phase, the capacitor C_2 is discharged through ϕ_2 while the charge on C_1 is preserved for next cycle. This DAC requires N clock cycles for N-bit conversion.

Thus, the SAR ADC requires $1.5N$ clock cycles for total conversion. Techniques for capacitance mismatch error cancellation have also been employed in DAC.

Chen *et al.* (2013) proposed noise shaping SAR ADC using three capacitors as shown in figure 1.10. In the first phase, the input is sampled on capacitor C_2 through ϕ_4 and ϕ_5 switches and C_1 is charged to V_{ref} through ϕ_1. The charge on C_2 is transferred to C_f by closing ϕ_6 and ϕ_3 in the next phase of sampling cycle. In next cycle, ϕ_3 is OFF and ϕ_2 is ON such that the charge on C_1 is shared between C_1 and C_2 while transferring equal charge to capacitor C_f. The output voltage becomes $V_{in} - \frac{V_{ref}}{2}$ and is fed to the comparator. The comparator outputs MSB based on the sign of output voltage. In the next phase, ϕ_2 is OFF and the capacitor C_2 is discharged through ϕ_3 and ϕ_5 if MSB is 1 or through ϕ_3 and ϕ_6 if MSB is 0. Thus N-bit SAR ADC needs $N + 1$ clock cycles. The voltage dependent switch parasitic capacitance introduces non-linearity in conversion.

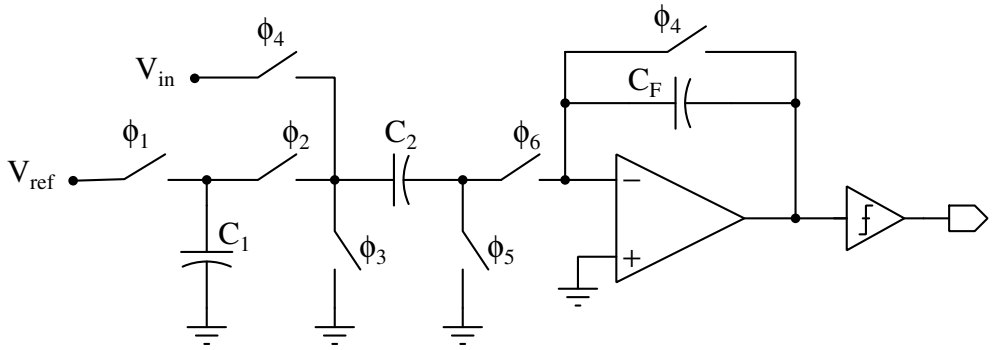


Figure 1.10: Noise shaping SAR ADC.

Alvarez-Fontecilla and Abusleme (2015) proposed a fully differential passive reference sharing SAR ADC using $(N + 1)$ capacitors and a comparator. The theoretical analysis proves that the accuracy of ADC is affected by noise and non-linearity. The parasitic capacitance and design complexity of switching logic restricts its use to low resolution and low speed applications only.

All these schemes used the charge redistribution technique to reduce the capacitor spread and switching energy. In this technique, the charge required for conversion is derived from reference voltage for every bit of the decision. This causes distortion in ADC output due to signal-dependent inaccuracies associated with the reference voltage. In an attempt to overcome this issue, Craninckx and Van der Plas (2007) proposed a charge sharing technique, in which, all the charge required for a conversion

is drawn in a single cycle from reference voltage and the conversion is performed passively.

Further, a charge sharing SAR ADC using asynchronous logic controller is proposed in Rabuske and Fernandes (2017). It uses two track and hold (TH) circuits, each with 35 unit capacitors. Also, a precision passive charge sharing DACs for SAR ADCs are reported in Chen *et al.* (2018). All these designs used explicit TH circuits which results in higher input buffer power consumption as well as large area. The second drawback is that the comparator sees different capacitances (C) at its input nodes in each comparison cycle. Consequently, the DAC voltage ($V = Q/C$) observed by the comparator decreases from cycle to cycle. This makes the ADC non-linear with comparator offset and also it becomes less noise tolerant.

Biomedical signals such as EEG, ECG, breathing quality, measures of blood parameters such as oxygenation, glucose, cholesterol, CRP, ESR, platelet count etc., have varying dynamic range and bandwidth. In addition, within a given application like ECG, to accomplish low and high resolution tasks at different intervals, a variable resolution ADC may be optimal. Hence, a power-efficient and fully programmable resolution ADC can substantially reduce the size and cost of the wireless body sensor network (WBSN). Le *et al.* (2005) proposed a variable resolution ADC with a innovative binary search algorithm. Based on the input signal and the comparator output, the proposed algorithm will select the appropriate voltage reference in every clock cycle, and thus at the end of N^{th} comparison, the equivalent N-bit output is available.

O'Driscoll *et al.* (2011) presented an adaptive resolution ADC array for neural sensor using charge redistribution SAR ADC as a base cell. Chaturvedi *et al.* (2013) proposed a 1 MS/s SAR ADC with a ping-pong input sampling scheme for multi-channel input to alleviate the bandwidth requirement of the input buffer. Also, the resolution of ADC could be varied from 8-bit to 1-bit. Yip and Chandrakasan (2013) reported a power scalable SAR ADC with a resolution reconfigurable from 5-bit to 10-bit using segmented DAC structures. In Srinivasan and Balsara (2014), Polineni and Gupta (2015), Chen *et al.* (2017), Nasserian *et al.* (2019), adaptive resolution ADC architectures are presented for implantable sensors. In all these papers, SAR ADC is designed with binary weighted capacitive DAC using different switching methods.

José (2011) presents a tutorial on design of DSMs. This explores the operating principles, design methods, circuit models and practical issues. A review on innovative

DSM architectures design and their applications has also been reported. José *et al.* (2015) discusses cutting edge DSM architectures suitable for contemporary applications along with their limitations. Moreover, this explores the evolution of strategies for future DSMs.

1.4 Thesis Contributions

The main purpose of this research is to design energy efficient ADCs for biomedical signal applications. The key contributions of this research work is listed below.

- A fully differential MSB capacitor split switching technique for binary weighted capacitive DAC based SAR ADC is proposed. To validate the performance of this proposed design, a 10-bit binary weighed capacitive DAC based SAR ADC is designed with a supply voltage of $0.5\,V$ in UMC 90 nm CMOS technology.

- A switched capacitor based SAR ADC employing a passive reference charge sharing and charge accumulation technique is proposed to reduce the number of unit capacitors required significantly in the design of DAC and hence saving the area of the circuit. This architecture is modelled in MATLAB along with practical considerations which helped to define the limitations. The proposed architecture is designed and laid out in UMC 180 nm CMOS technology for target resolution of 11-bit and validated through the post layout extracted simulation results.

- A fully differential switched capacitor integrator based programmable resolution hybrid ADC architecture for biomedical applications is proposed by integrating DSM with switched capacitor SAR ADC. The model for this architecture is developed using MATLAB and distortion analysis is carried by incorporating all non-idealities.

- The performance of programmable resolution hybrid ADC architecture is validated by designing an 8-bit to 15-bit programmable resolution ADC in UMC 180 nm CMOS technology with a supply voltage of $1.8\,V$. Also, the design is laid out and verified with the post layout extracted simulation results.

1.5 Thesis Organization

The thesis is organized as follows.

- In chapter 1, a concise discussion is provided on the motivation to choose this research topic, which is followed by the overview of ADCs and design challenges. Also, a detailed discussion on the working principles of SAR ADC, DSM ADC and their applications is presented. After that, a systematic study on state of the art designs corresponding to energy efficient switching schemes for feedback DAC in SAR ADCs, noise shaped SAR ADCs, switched capacitor ADCs and variable resolution ADCs is presented.

- In chapter 2, we propose a novel energy efficient, fully differential switching technique for feedback binary weighted capacitive DAC in SAR ADCs. The proposed technique is validated by the design and simulation of a 10-bit SAR ADC using UMC 90 nm CMOS 1P9M technology for low frequency applications.

- Chapter 3 presents a switched capacitor based SAR ADC employing a passive reference charge sharing and charge accumulation technique. Also, the practical limitations in the design and simulation of the proposed architecture are explored by modelling in MATLAB. Finally, the proposed architecture is validated by a 11-bit SAR ADC design and post-layout simulations.

- Chapter 4 presents a design and simulation of fully differential switched capacitor based hybrid ADC with variable resolution from 8-bit to 15-bit for low frequency applications. It analyzes the distortion caused by the capacitors' mismatch and operational transconductance amplifier (OTA). Also, the design and simulation of OTA with programmable slew rate and unity gain bandwidth (UGB) is presented.

- Finally, the concluding remarks of this thesis are presented in chapter 5. Also, it lists the potential methods of optimizing the proposed designs as future scope of research.

Chapter 2

Design and simulation of SAR ADC with a novel energy efficient differential switching technique for binary weighted capacitive feedback DAC

SAR ADC is well suited for moderate resolution and energy efficient applications such as biomedical signal acquisition. The comparator, feedback DAC and SAR control logic are the building blocks of SAR ADC. Among these, the feedback DAC consumes more energy as well as area compared to the dynamic comparator and the digital control logic. Therefore, in an attempt to reduce energy consumption, a novel energy efficient differential switching technique for binary weighted capacitive feedback DAC is proposed in this chapter. Initially, it is modelled and behavioural simulations are performed using MATLAB. To validate the proposed switching technique, a 10-bit SAR ADC is designed with binary weighted capacitive DAC. Specifications of SAR ADC are presented below.

- Resolution N= 10-bits.
- Input bandwidth f_{inB}=1 kHz.
- Sampling frequency f_s = 10 kS/s

- Supply voltage V_{dd}= 0.5 V.
- INL $<$ 0.5 LSB and DNL $<$ 0.5 LSB.
- UMC 90 nm CMOS 1P9M process technology.

2.1 A novel energy efficient differential switching technique.

The proposed switching scheme is based on fully differential MSB capacitor split technique. The circuit level realization of proposed 10-bit SAR ADC is shown in figure 2.1. In sampling phase, the top plates of all capacitors in DAC are connected to differential input signals. The bottom plates of MSB sub array capacitors are connected to input signals and the remaining capacitors' bottom plates are connected to *Gnd*. This allows the differential input signals to be sampled only on LSB capacitor array.

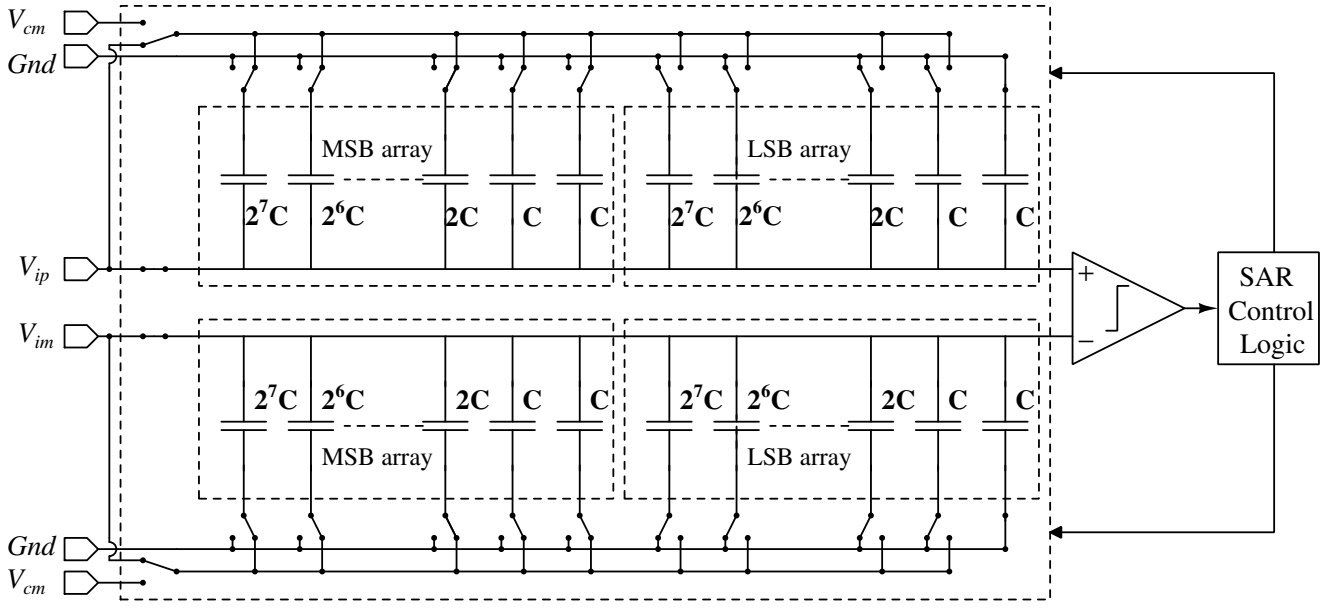


Figure 2.1: Proposed 10-bit SAR ADC architecture.

A 4-bit SAR ADC shown in figures 2.2, 2.3, 2.4 is used for describing the proposed switching technique. Here, $C_2 = 2C$ and $C_1 = C_0 = C$. After sampling phase, the bottom plates of MSB capacitor sub array are connected to V_{cm} (i.e. $0.5V_{ref}$) as shown

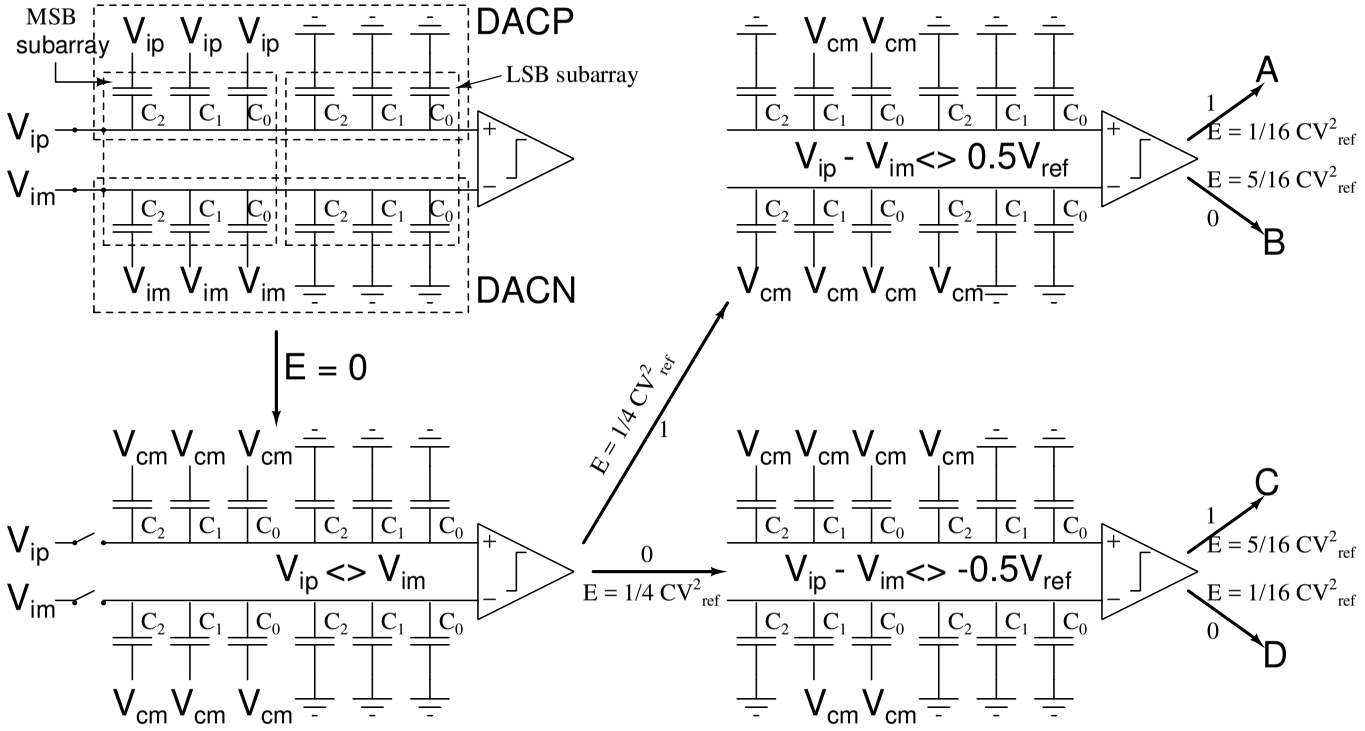


Figure 2.2: Proposed switching technique with 4-bit SAR ADC example.

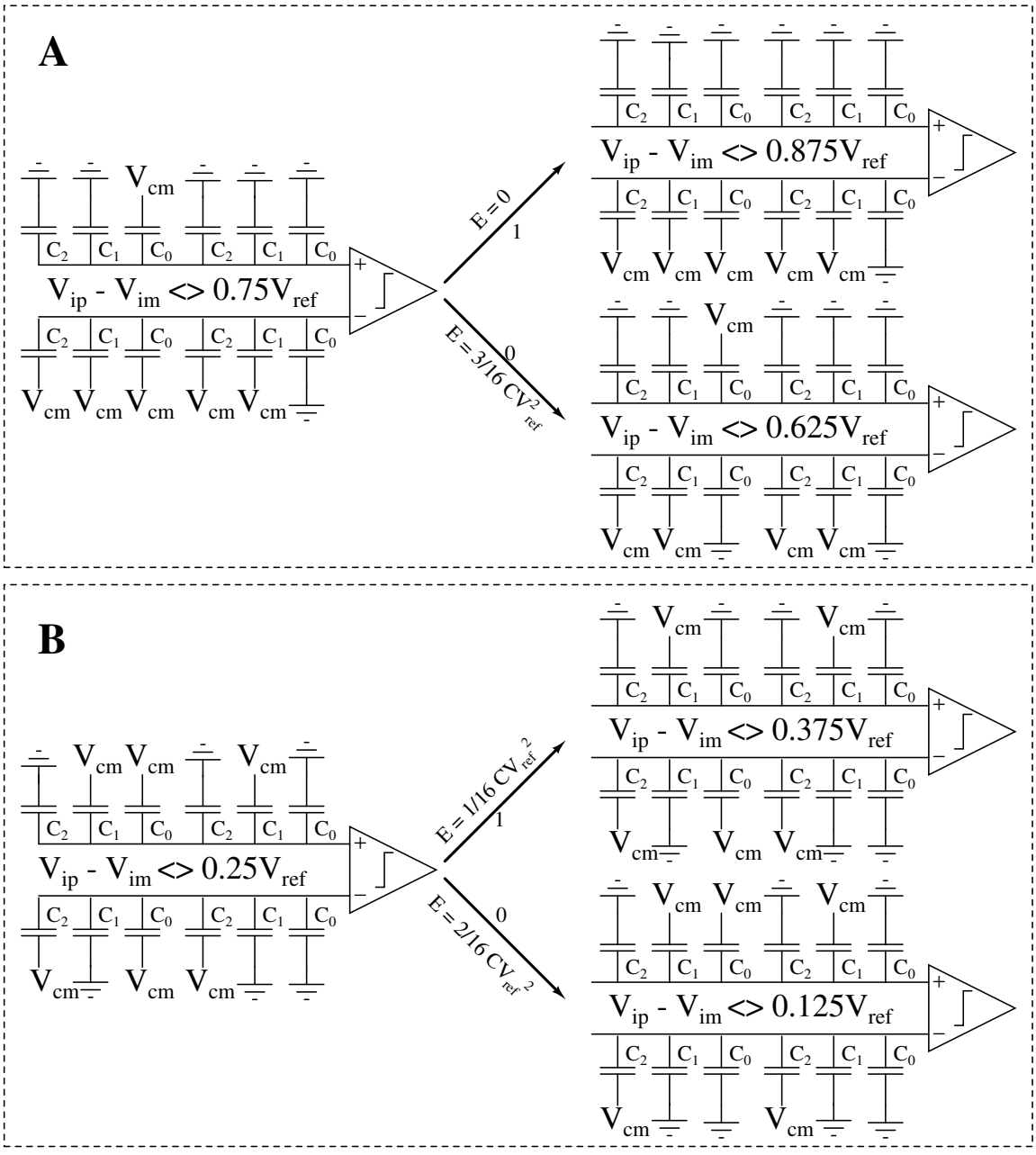


Figure 2.3: Proposed switching technique with 4-bit SAR ADC example.

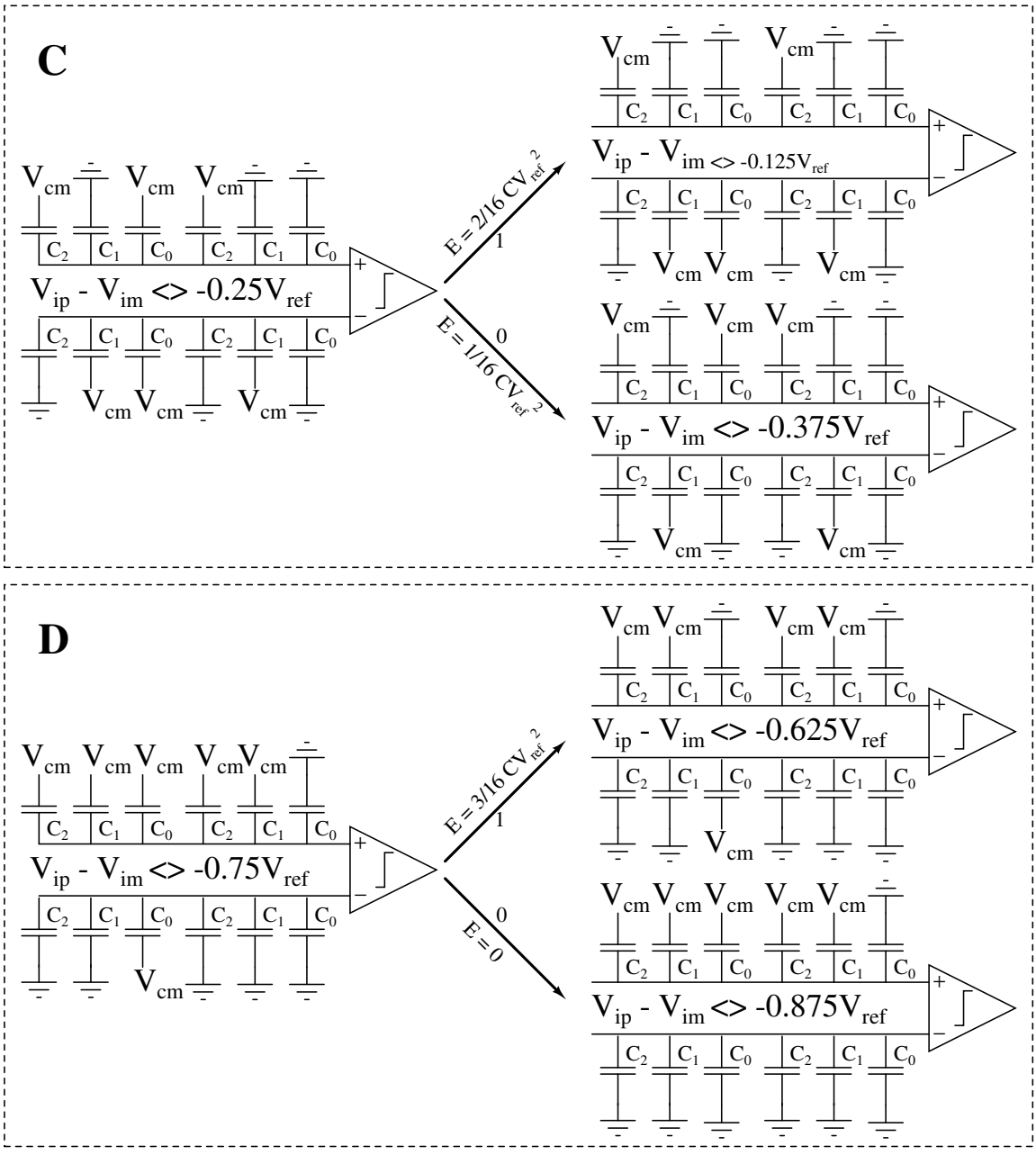


Figure 2.4: Proposed switching technique with 4-bit SAR ADC example.

in figure 2.2. By applying superposition theorem, the voltages on DACP and DACN are calculated as $\frac{V_{ip}}{2}+\frac{V_{cm}}{2}$ and $\frac{V_{im}}{2}+\frac{V_{cm}}{2}$ respectively. Here, DACP and DACN are the fully differential DACs, which are connected to the positive and negative terminals of the comparator respectively. MSB (D_3) is determined by comparing the voltages on DACP and DACN, which is equivalent to comparing V_{ip} with V_{im}. If $V_{ip} > V_{im}$ then MSB (D_3) is 1 otherwise 0.

The division of input signals by 2 along with the differential comparison used in this switching scheme makes V_{cm} ($= 0.5V_{ref}$) as supply voltage for DACs. The MSB capacitor is charged to $\frac{V_{ip}}{2}-\frac{V_{cm}}{2}$ in DACP and $\frac{V_{im}}{2}-\frac{V_{cm}}{2}$ in DACN. The net charge drawn from the supply voltage is shown in equation (2.1) and it is zero. Thus the energy consumed in the first switching step is zero.

$$\begin{aligned}\Delta q &= 2^{N-2}C\left(\frac{V_{cm}}{2}-\frac{V_{ip}}{2}\right)+2^{N-2}C\left(\frac{V_{cm}}{2}-\frac{V_{im}}{2}\right)\\ &= 2^{N-2}C\left(V_{cm}-\frac{V_{ip}+V_{im}}{2}\right)\\ &= 0 \qquad\qquad \left(\because V_{cm}=\frac{V_{ip}+V_{im}}{2}\right)\end{aligned} \tag{2.1}$$

In the second step, if D_3 is 1 (0) then the bottom plate of C_2 capacitor in MSB sub array of DACP (DACN) is connected to Gnd and the bottom plate of C_2 capacitor in LSB sub array of DACN (DACP) is connected to V_{cm}. This switching reduces the voltage on DACP (DACN) by $V_{cm}/4$ and increases the voltage on DACN (DACP) by $V_{cm}/4$. This is equivalent to comparing $V_{ip}-V_{im}$ with $0.5V_{ref}$ (-$0.5V_{ref}$). Similarly, the third switching step depends on second bit (D_2) as shown in figures 2.3, 2.4. This process repeats and calculates the remaining bits till D_1 bit. In LSB generation (D_0), only one DAC (either DACP or DACN depends on D_1) switches. If D_1 is 1 (0) then MSB sub array capacitor C_0 bottom plate in DACP (DACN) switches to Gnd. LSB (D_0) is obtained from the comparator by comparison of DACP and DACN voltages. The proposed switching scheme is built on a single reference voltage and constant common mode voltage at the comparator inputs. Thus, the linearity of ADC is improved compared to existing switching techniques. Assuming all codes are equiprobable, the average switching energy consumption for N-bit SAR ADC is

obtained as in equation (2.2).

$$E_{proposed} = \sum_{i=1}^{N-2}(2^i - 1)2^{N-2i-4}\, CV_{ref}^2 \quad J$$
$$= \left(\frac{2^{N-3}}{3} + \frac{2^{-N}}{3} - 0.25\right) CV_{ref}^2 \quad J \tag{2.2}$$

2.2 Comparison with existing switching schemes

The behavioural simulations of the proposed switching technique and the switching schemes presented in Rahimi and Yavari (2014), Yazdani *et al.* (2015, 2016) were carried out for 10-bit SAR ADC in MATLAB. The switching energy consumed by the DAC to determine all digital output codes from their equivalent analog input voltages is calculated and plotted in figure 2.5. The average switching energy of proposed fully differential 10-bit SAR ADC is $42.4\,CV_{ref}^2$ and it is 96.89 % more energy efficient than the conventional switching schemes.

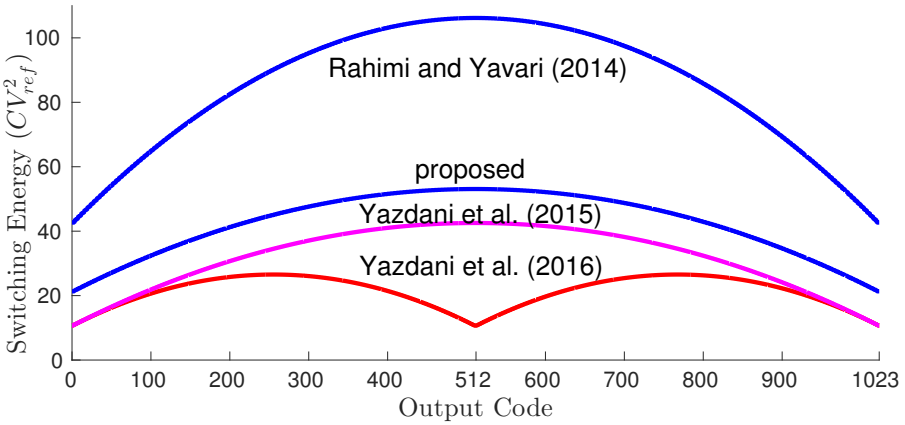


Figure 2.5: Switching energy per each code.

Figure 2.5 shows that the switching schemes presented in Yazdani *et al.* (2015),Yazdani *et al.* (2016) consume less energy than the proposed one, but this happens at the cost of comparator input common mode voltage variation. This variation in common mode voltage increases the design complexity of comparator and also changes the comparator offset. This leads to increased power consumption and non linearity in SAR

Table 2.1: Comparison of several switching schemes for 10 bit SAR ADC.

Switching Scheme	Average energy consumption (CV_{ref}^2) J	Energy efficiency (%)	Supply Voltages	Sensitivity to V_{cm} variation	Common Mode voltage variation	Number of unit capacitors (C)
Conventional (McCreary and Gray 1975)	1363.33	Reference	V_{ref}	-	No variation	2048
Capacitor-split (Ginsburg and Chandrakasan 2005)	852.33	37.48	V_{ref}	-	No variation	2048
Monotonic (Liu *et al.* 2010)	255.50	81.26	V_{ref}	-	0 to $\frac{V_{ref}}{2}$	1024
V_{cm} based (Zhu *et al.* 2010)	170.17	87.54	V_{ref}, V_{cm}	No	No variation	1024
Trilevel (Yuan and Lam 2012)	42.41	96.89	V_{ref}, V_{cm}	Yes	$\frac{V_{ref}}{2}$ to V_{ref}	512
New tri level (Rahimi and Yavari 2014)	84.9	93.7	V_{ref}, V_{cm}	Yes	No variation	512
Xie *et al.* (2015)	42.17	96.91	V_{ref}, V_{cm}	Yes	0 to V_{ref}	512
Yazdani *et al.* (2015)	31.875	97.66	V_{cm}	No	$\frac{V_{ref}}{2}$ to $\frac{5}{8}V_{ref}$	1024
Yazdani *et al.* (2016)	21.20	98.44	V_{cm}	No	$\frac{V_{ref}}{4}$ to $\frac{V_{ref}}{2}$	1024
This work	42.417	96.89	V_{cm}	No	No variation	1024

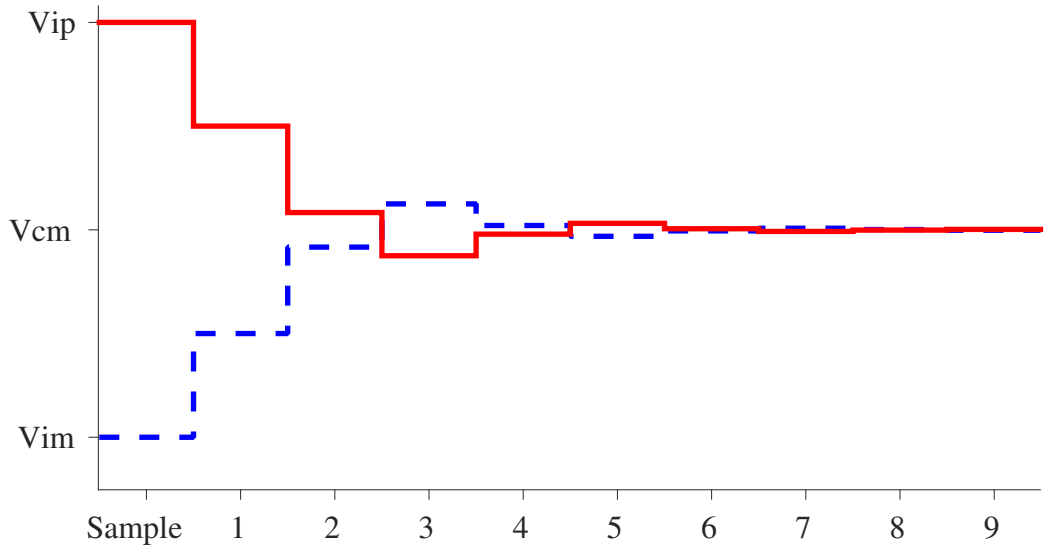


Figure 2.6: The differential voltages on DACP and DACN during conversion.

ADC. The proposed switching scheme maintains constant common mode voltage by differential change in DACP, DACN voltages as shown in figure 2.6. Table 2.1 presents a comparison of the proposed switching scheme and those reported in state of the art.

2.3 Circuit level implementation of SAR ADC

In general, a typical SAR ADC is implemented using only three main blocks, Capacitive DAC, comparator and SAR logic controller.

2.3.1 Capacitive DAC

In a SAR ADC, a capacitive DAC is commonly used to generate weighted reference voltages. Compared to a resistive DAC, the capacitor array is more easily fabricated with less mismatch errors, and it is also more power-efficient.

2.3.1.1 Choosing the capacitance value

The binary weighted capacitive DAC consists of 2^N unit capacitors for N-bit resolution. The capacitance value is determined from the thermal noise and capacitor mismatch for required accuracy.

- The unit capacitor, denoted as C , should be kept as small as possible for energy saving because the DAC energy consumption is proportional to CV_{ref}^2.
- The thermal noise of a simple RC circuit (e.g., a sampling circuit) is given by kT/C, which imposes a lower bound on the minimum required capacitance to achieve a given signal-to-noise ratio. Therefore, the thermal noise is inversely proportional to unit capacitance C.
- With respect to matching, a smaller capacitance typically has a smaller area, which results in higher mismatch as given by Pelgrom's inverse-area mismatch model (Pelgrom *et al.* 1989). Thus, the mismatch also imposes another lower bound on unit capacitance.

The lower bound on unit capacitance is determined by mismatch and noise, whichever is minimum and the higher bound is determined by the energy consumption. In binary weighted capacitive feedback DAC based SAR ADCs, the minimum capacitance is limited by the mismatch, rather than the thermal noise.

2.3.1.2 Choosing type of capacitor

Analog integrated circuits (ICs) use various types of integrated capacitors utilizing Metal-Oxide-Semiconductor (MOS), p-n junction, metal-insulator-metal (MIM), polysilicon-insulator-polysilicon (PIP), metal-oxide-metal (MOM), and other structures.

- MOS and p-n junction capacitors offer highly non-linear capacitances. Particularly, they are useful in certain applications like compensation, bypassing and delay circuits.
- A PIP capacitor have superior area density and matching properties, however, they are no longer supported by semiconductor foundries in technologies below 180 nm.
- MIM capacitors have better area efficiency, however, they are typically attributed with strict layout design rules which limit the minimum MIM capacitance to several femto farads or tens of femto farads. In addition, special dedicated metal layers, high-k dielectric and process steps required by MIM capacitors are less likely supported by all process technologies.

- The capacitive coupling between the lateral metals generated by standard metallization wiring lines, optionally, vias and normal dielectric is exploited by MOM capacitors. Lateral capacitive coupling provides better matching characteristics than vertical coupling because the lateral dimensions have better process control than the metal and dielectric layer thicknesses. Several metal layers are bound in parallel by vias, helping to create a vertical metal layer or grid, to achieve the maximum capacitance density. In general, the metal layers M1–M6 with optimum metal width and spacing are used for MOM capacitors to maximize the capacitance density particularly in deep sub micron (<100 nm) technologies.

Finally, from the state of art, the MIM capacitors are preferred because they provide larger on-chip capacitances. On the other hand, MOM capacitors are useful for small capacitors (fF/sub fF) with good enough matching and small parasitics.

Typically, MOM structures support symmetric form and asymmetric form in UMC 90 nm process technology. The two ports of symmetric capacitor are mirrored to one another and the number of fingers per layer are limited to even numbers to preserve the symmetry. In asymmetric MOM structures, one port (bottom port) is connected to metal1 (M1), which shields the other port (top port) from the substrate identical to typical planar MIM capacitor. The finger count per layer is limited to an odd number. The guard ring (ground ring) around the MOM capacitance tends to reduce the external parasitic coupling from outside environment.

2.3.1.3 Modelling capacitor mismatches in MATLAB

The capacitor mismatch introduces offset and non-linearity in ADC transfer characteristics. In general, the random variations in step sizes is measured by differential non-linearity (DNL) and the correlation between successive step sizes is measured by integral non-linearity (INL). To study the effects of capacitor mismatch on SAR ADC linearity and SNDR, a unit capacitor with a Gaussian distribution is modelled in MATLAB. The capacitive DACs are built using these models, and the non-linearities such as INL and DNL are calculated per code. The DNL and INL per code are measured by assuming 1 % standard deviation in $\Delta C/C$ since all fabrication technologies mention less than 1 % C capacitor mismatch. A 10-bit SAR ADC is implemented with proposed switching technique by incorporating capacitance mismatch in MATLAB. Using the Monte Carlo process, the effects of mismatch variations on ADC transfer

characteristics are simulated for 100 runs. The DNL and INL per code are calculated and plotted as shown in figure 2.7. It can be observed that the DNL and INL are less than ± 0.5 LSB for all codes.

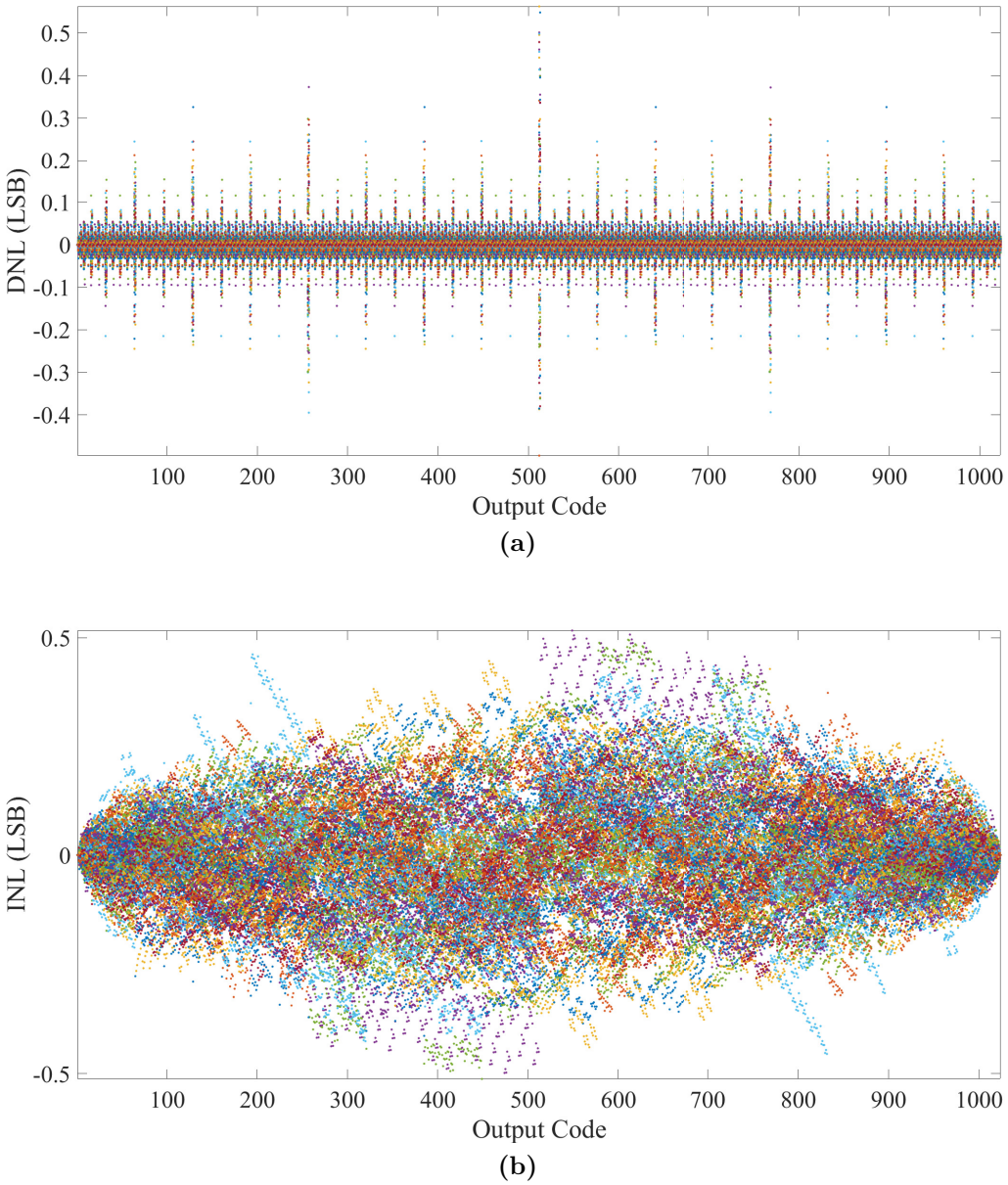


Figure 2.7: Proposed 10-bit SAR ADC Monte Carlo simulations for 100 runs: (a) DNL, (b) INL per each code.

Further, the dynamic characteristics dependence on capacitor mismatch is found through single tone testing. The mean SNDR with respect to standard deviation

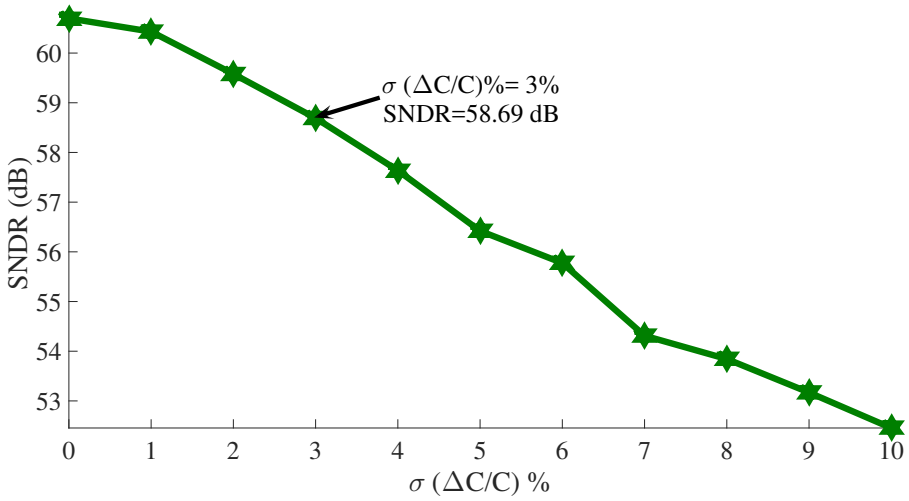


Figure 2.8: SNDR vs capacitor mismatch standard deviation.

of unit capacitor $\left(\sigma_{\Delta C/C}\right)$ is plotted in figure 2.8. One can observe that, with ideal capacitors SNDR is close to the ideal 61 dB and as the capacitor mismatch increases SNDR starts degrading.

The plot suggests that a capacitor mismatch of 3 % is acceptable up to 3 dB SNDR degradation, but since the values shown in this figure 2.8 are mean values and also depend on the random numbers used to generate the capacitor mismatch, the resulting SNDR values may vary. Monte Carlo simulations use pseudo-randomly generated

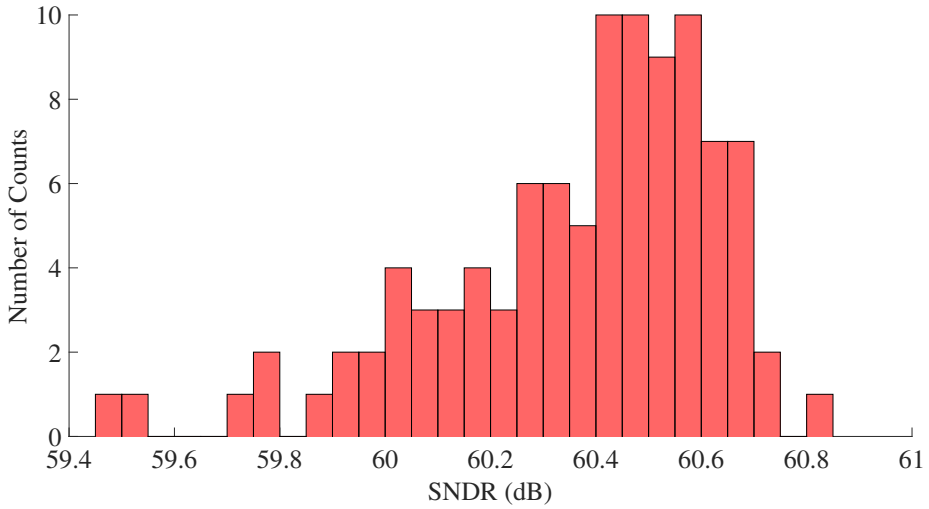


Figure 2.9: Monte Carlo simulations per 100 runs for capacitor mismatch.

numbers by repeated sampling to solve complex numerical problems. The parameters for each sample are different and unique, allowing distribution in the results. Figure 2.9 shows the SNDR distribution for a mismatch of 1 %. The SNDR distribution starts close to the ideal 61 dB, has a peak around 60.5 dB and tail towards lower values. Out of the 100 samples taken not a single one falls below 59 dB which suggests that the previously calculated capacitor matching requirement is a realistic estimate. Therefore, it can be concluded that the unit capacitance value (C) should be chosen in such a way that, it guarantees 1 % standard deviation of capacitance mismatch $\left(\sigma_{\Delta C/C}\right)$. In UMC 90 nm technology, 140 fF capacitance guarantees 1 % standard deviation of $\Delta C/C$.

2.3.2 Comparator

The comparator is crucially important block of ADC. In its simplest form, the comparator can be considered as a 1-bit ADC. The characteristics of comparator plays a significant role in ADC characterization. In general, comparators are categorized as continuous time (static) comparators and discrete time (dynamic) comparators. Static comparators are composed of operational amplifiers of high gain followed by

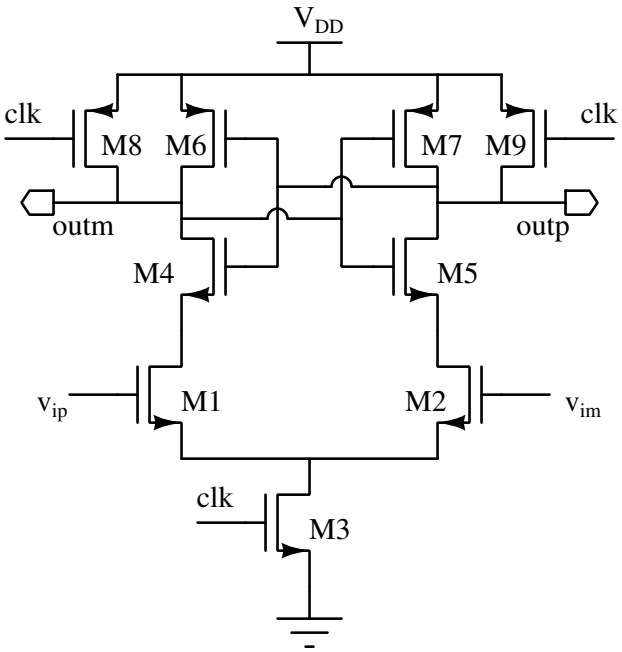


Figure 2.10: StrongARM dynamic comparator.

buffers. These comparators fail to achieve low power consumption and reduced die area at high speeds. In other words, the design of high-speed comparators requires larger bias currents, leads to higher power consumption and die area. In SAR ADC, the comparator functions only in certain time of interval after the voltage on feedback DACs settles down. Dynamic comparators that are operated by a clock are appropriate in such applications. These are also referred to as regenerative comparators or a latch, in which, the strong positive feedback used to accomplish the comparison at high speeds.

There are several architectures reported in literature for latch based comparators. Among all, strongARM latch is quite familiar for its high input impedance, rail-to-rail output swing, ideally zero static power consumption, and good robustness against noise and mismatch. The circuit diagram of strongARM comparator is shown in figure 2.10. It operates in two phases, the reset and the regeneration phase. Initially, the differential output nodes are charged to the supply voltage in reset phase. Further, in the regeneration phase, the output node voltages discharge to ground at differing rates depending on the input voltages. When these node voltages are low enough, one of the cross coupled inverters is triggered and initiates regeneration. The strong positive feedback between the cross coupled inverters pulls one of the outputs towards supply voltage, and another one is pulled to ground. The operation of comparator in two phases is depicted through figure 2.11 for a case of $v_{ip} > v_{im}$.

One of the key factors in designing a latch comparator for SAR ADC applications is the comparator's delay, which limits the maximum sampling rate that can be achieved. As shown in figure 2.11, the delay of this comparator is comprised of two time delays, t_{on} and t_{latch} (Babayan-Mashhadi and Lotfi 2014). The delay t_{on} represents the capacitive discharge of the load capacitance C_L until one of the p-channel transistors (M_6 or M_7) turns on. If the voltage at node v_{ip} is greater than v_{im} (i.e., $vip > v_{im}$), the transistor M_1 discharges 'outm' node faster compared to the 'outp' node, which is driven by the transistor M_2. Consequently, the discharge delay time (t_{on}) is given by equation (2.3).

$$t_0 = \frac{C_L|V_{thp}|}{I_2} \approxeq 2\frac{C_L|V_{thp}|}{I_{tail}} \tag{2.3}$$

The second term, t_{latch}, is the latching delay of two cross coupled inverters i.e. the time taken by the positive feedback of cross coupled inverters to reach the output

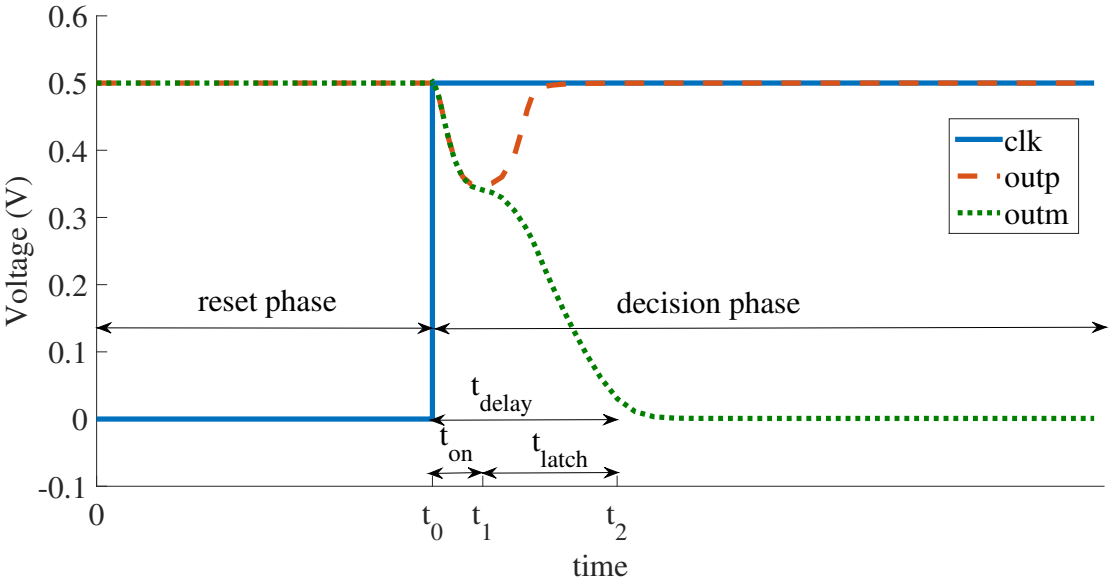


Figure 2.11: Comparator transient characteristics.

difference voltage of $V_{DD}/2$ from an initial output difference voltage ΔV_o. The output difference voltage (ΔV_o) can be calculated from t_{on} and is given by equation (2.4). Here, $g_{m,1,2}$ is transconductance of M_1, M_2 and β is current factor.

$$\begin{aligned} \Delta V_o &= |V_{outp}(t_1) - V_{outn}(t_1)| \\ &= \frac{(I_1 - I_2)t_{on}}{C_L} = |V_{thp}| \frac{\Delta I}{I_1} = |V_{thp}| \frac{g_{m1,2}\ \Delta V_{in}}{I_1} \\ &= 2\ |V_{thp}| \frac{\sqrt{\beta_{1,2}\ I_{tail}}\ \Delta V_{in}}{I_{tail}} \end{aligned} \tag{2.4}$$

The latch delay time t_{latch} is given by equation (2.5). In fact, this delay depends on the initial output voltage difference at the beginning of the regeneration (ΔV_o), in a logarithmic manner.

$$t_{latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta V_{out}}{\Delta V_o}\right) = \frac{C_L}{g_{m,eff}} \ln\left(\frac{V_{DD}/2}{\Delta V_o}\right) \tag{2.5}$$

where $g_{m,eff}$ is the effective transconductance of the cross coupled inverters. The delay expression for strongARM comparator is calculated by combining all these equations.

$$t_{delay} = \ t_{on} + t_{latch} = \frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}} \sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \tag{2.6}$$

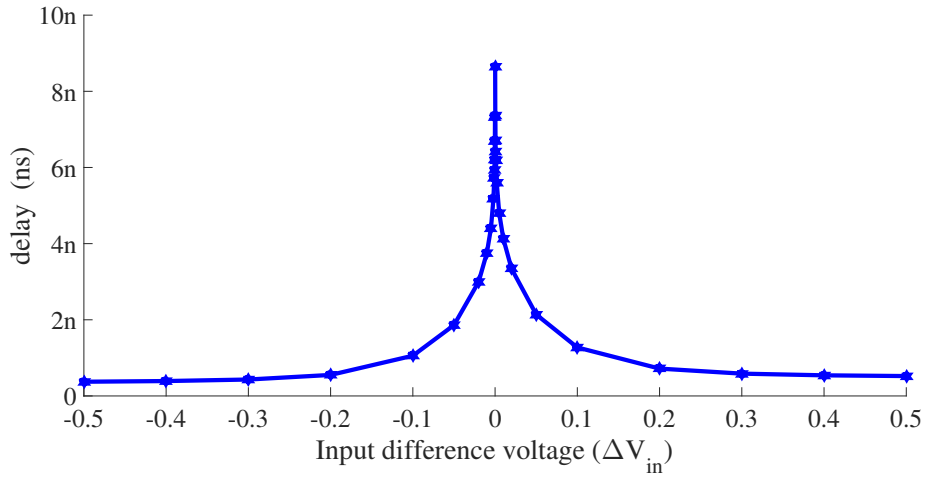


Figure 2.12: Comparator delay (t_{delay}) vs. Input voltage difference (ΔV_{in}).

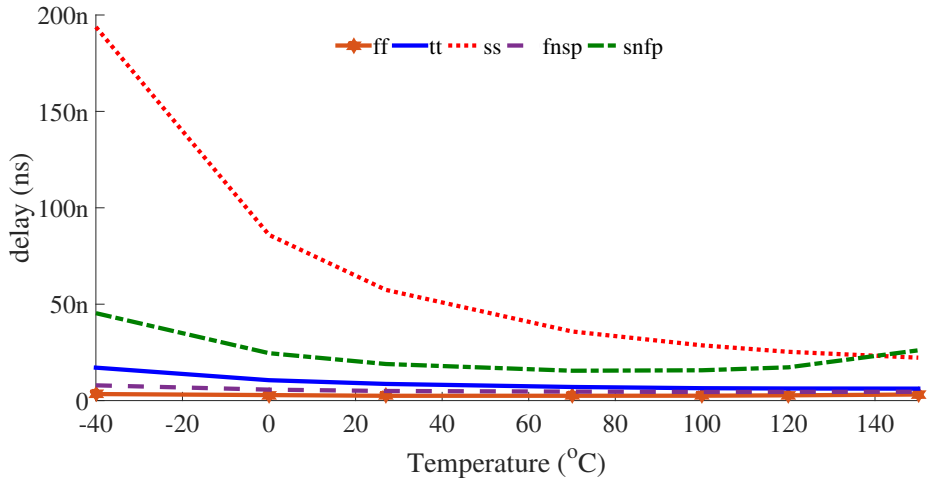


Figure 2.13: Comparator delay vs. Temperature for $\Delta V_{in} = 100\,\mu V$ across corners.

Equation (2.6) explains the impact of various parameters. The total delay is directly proportional to the comparator load capacitance C_L. In this design, there is no separate load capacitor C_L, it is a combination of parasitic capacitances at output nodes. The delay is inversely proportional to the input difference voltage (ΔV_{in}), which

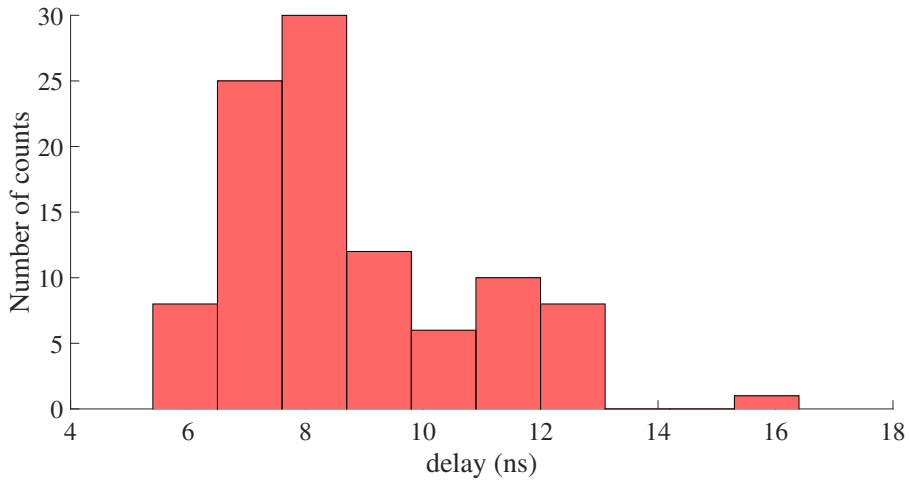


Figure 2.14: Monte Carlo simulations for 100 runs: Histogram of comparator delay for $\Delta V_{in} = 100\mu V$.

is endorsed by the simulation result as shown in figure 2.12. To find out the worst case delay, the corner analysis has been carried out at different corners with temperature variation. Figure 2.13 plots the delay as a function of temperature, at different corners for input difference voltage of 100 μV. The delay decreases with temperature in all corners because of proportional relationship between current and temperature. The worst case delay is 193.8 ns, which occurs at slow NMOS slow PMOS (ss) corner at -40 ^oC for 100 μV input voltage difference. The Monte Carlo analysis gives the effect of process and mismatch on comparator delay. Figure 2.14 plots the histogram of delay for 100 Monte Carlo runs with input difference voltage 100 μV at room temperature (27 ^oC). The histogram plot shows that the mean value of comparator delay is 8.7 ns and the standard deviation is 1.2 ns. Also, it can be observed that the maximum comparator delay is around 16 ns.

Another main characteristic of a comparator is energy consumption. Figure 2.15 plots the energy per conversion with input difference voltage (ΔV_{in}). It is observed that the energy per conversion is inversely related to absolute value of input difference voltage ($|\Delta V_{in}|$). The reason behind this relation is that the delay increases as the input difference voltage decreases, i.e. the current path exists for large time from supply voltage to ground. Further, the corner analysis has been carried out to calculate the maximum energy consumption per conversion. Figure 2.16 plots the energy as a function of temperature, at different corners for input difference voltage of 100 μV.

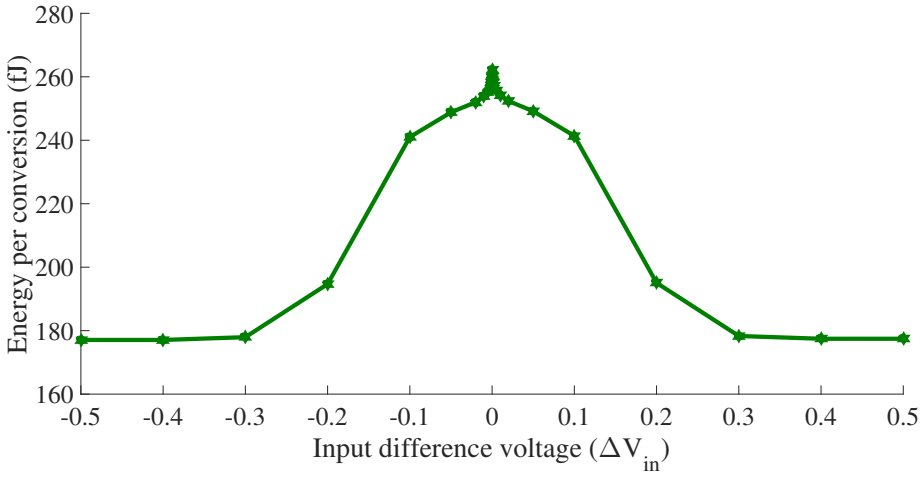


Figure 2.15: Comparator energy per conversion vs. Input voltage difference (ΔV_{in}).

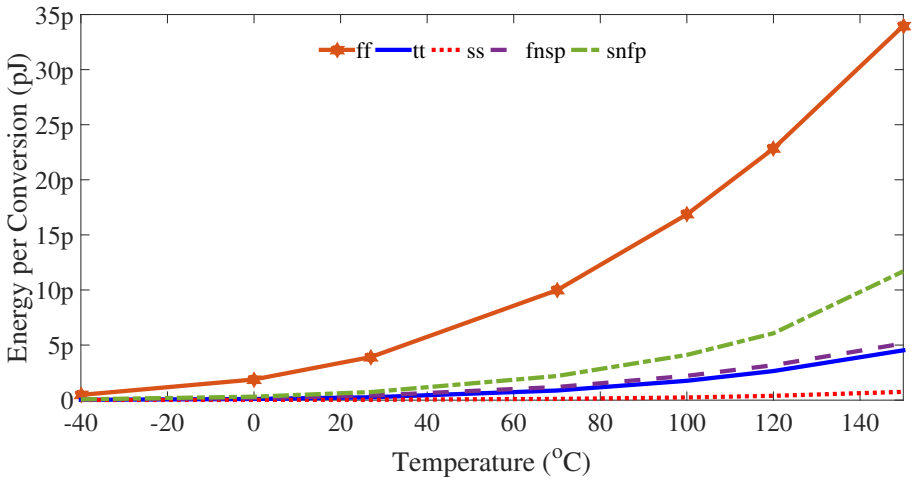


Figure 2.16: Comparator energy per conversion vs. Temperature for $\Delta V_{in} = 100\mu V$ across corners.

The energy per conversion increases with temperature because the short circuit current increases. Also, it is more in fast NMOS fast PMOS (ff) corner because of the larger short circuit current from supply voltage to ground.

Another important characteristic of comparator is its offset and hysteresis. If it is not designed properly, the comparator offset can degrade the SNDR of SAR ADC. Therefore, to estimate this effect, the comparator offset parameter is incorporated into 10-bit SAR ADC model in MATLAB and behavioural simulations are carried out. Figure 2.17 shows the SAR ADC SNDR variation with respect to comparator

offset. It guarantees 58 dB SNDR for absolute offset value, which is less than 500 μV. The comparator offset can be reduced by increasing the transconductance of input transistors pair and latch transistors. The comparator is designed and simulated in cadence using UMC 90 nm process technology. The design is optimized and the transistor dimensions are scaled to get an absolute offset less than 100 μV. Table 2.2 shows the width (W) and length (L) of each transistor used in the comparator.

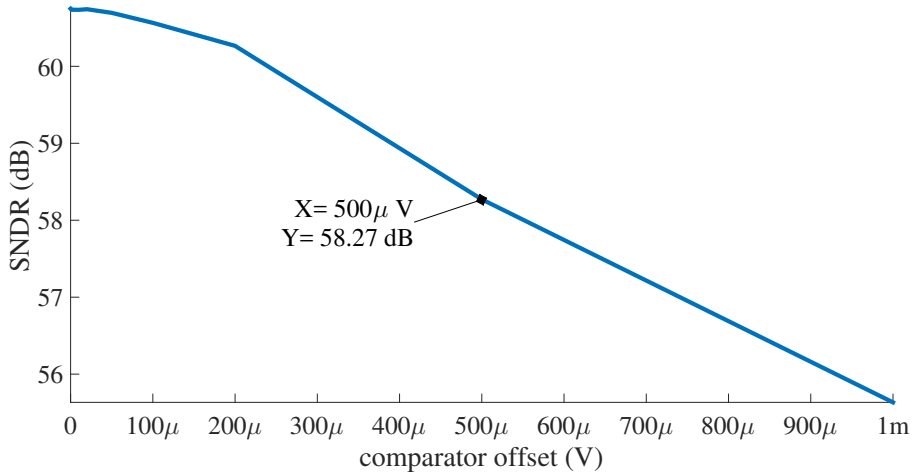


Figure 2.17: Comparator offset vs. 10-bit SAR ADC SNDR.

Table 2.2: Transistor sizes of strongARM comparator.

Transistor	W(μm)/L(μm)
M_1, M_2, M_3	0.48/0.08
M_4, M_5	2.4/0.08
M_6, M_7	7.2/0.08
M_8, M_9	0.12/0.08

Figure 2.18 shows the transfer characteristics of comparator from low to high and high to low. Here, two offsets are observed, one is when comparator output is '0' is called as offset$_0$ and the other one when comparator output is '1' is called as offset$_1$. The difference between these two offsets is known as hysteresis of comparator. From the simulation results, the offset$_0$, offset$_1$ and hysteresis values calculated at room temperature ($27\,^oC$) are -9 μV, -73 μV and 64 μV respectively. Monte Carlo analysis is used to estimate the effect of process and mismatch variations on comparator offsets and hysteresis. Figure 2.19 plots the histograms of offset$_0$, offset$_1$ and hysteresis for 100

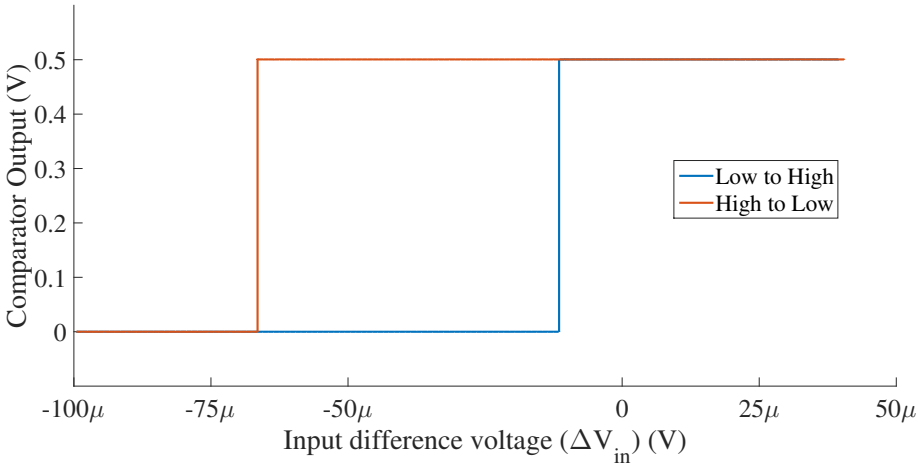


Figure 2.18: Comparator transfer characteristics.

Monte Carlo runs. The mean values and standard deviations of offsets and hysteresis are calculated as μ_{offset_0} = -9.64 μV, μ_{offset_1} = -72.36 μV, $\mu_{hysterisis}$ = 62.72 μV and σ_{offset_0} = 1.389 μV, σ_{offset_1} = 5.921 μV, $\sigma_{hysterisis}$ = 5.276 μV from the Monte Carlo analysis. These are far lower than 1 LSB and therefore they are within the acceptable limits.

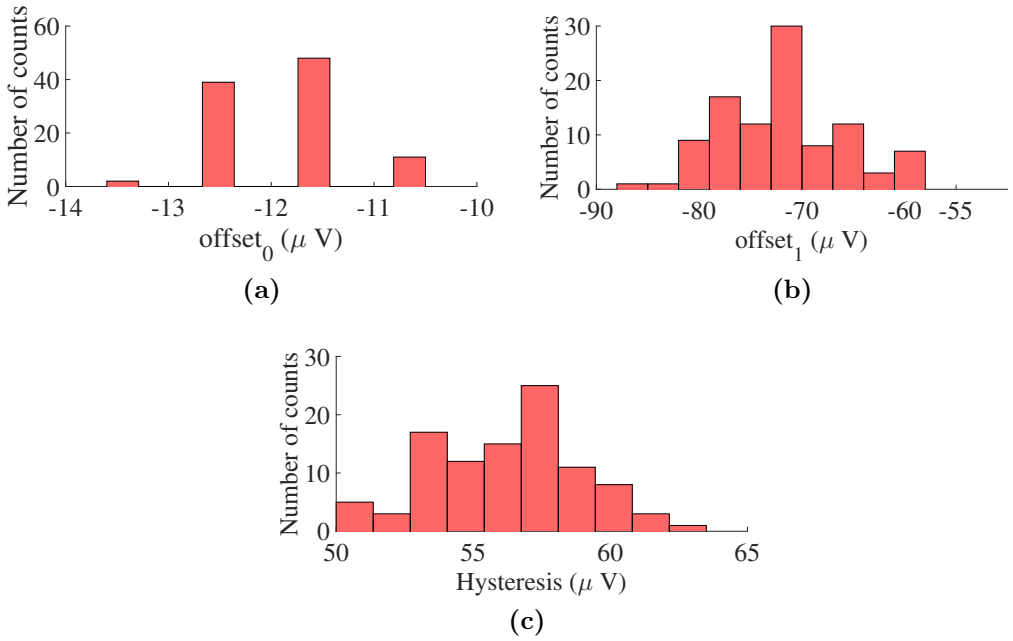


Figure 2.19: Monte Carlo simulations per 100 runs: (a) $offset_0$ histogram, (b) $offset_1$ histogram, (c) Hysteresis histogram.

2.3.3 SAR logic controller

The proposed switching technique for binary weighted capacitive feedback DAC in SAR ADC, previously described in section 2.1 is implemented using digital logic circuits. The proposed ADC utilizes a synchronous SAR logic controller, which generates the sample signal and the switch control signals for the feedback capacitive DAC. This SAR logic controller requires twelve clock cycles for each sample conversion. In those twelve clock cycles, the first two clock cycles are used for sampling the input on capacitive DAC array and the subsequent ten clock cycles used for data conversion purpose, here, each bit is determined sequentially. The detected bit determines the switch control logic for capacitive DAC in next clock cycle. At the end of 12^{th} cycle, the digital code stored in parallel in parallel out (PIPO) register and a *reset* signal is generated with a small delay. Figure 2.20 shows the timing diagram of clock signals and switch logic control signals graphically.

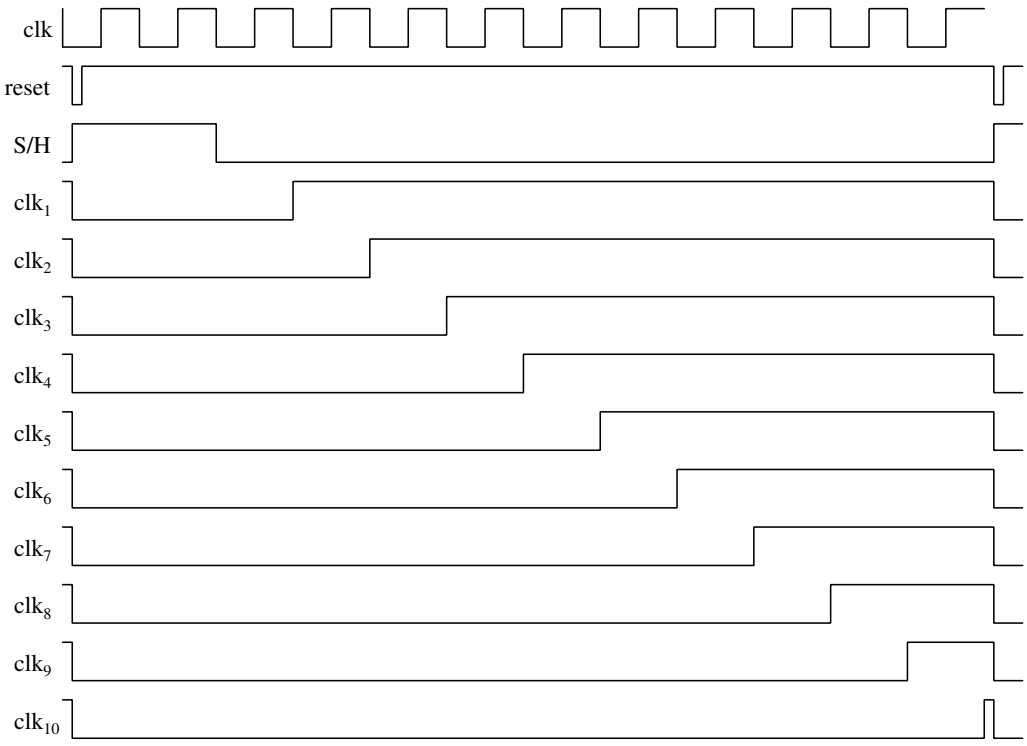


Figure 2.20: Timing diagram of clock signals for SAR control logic.

The comparator commences the comparison at the positive edge of clock cycle and generates the output. Thus, the digital output is sampled onto the serial in parallel out (SIPO) register on negative edge of clock and determines the switch control logic.

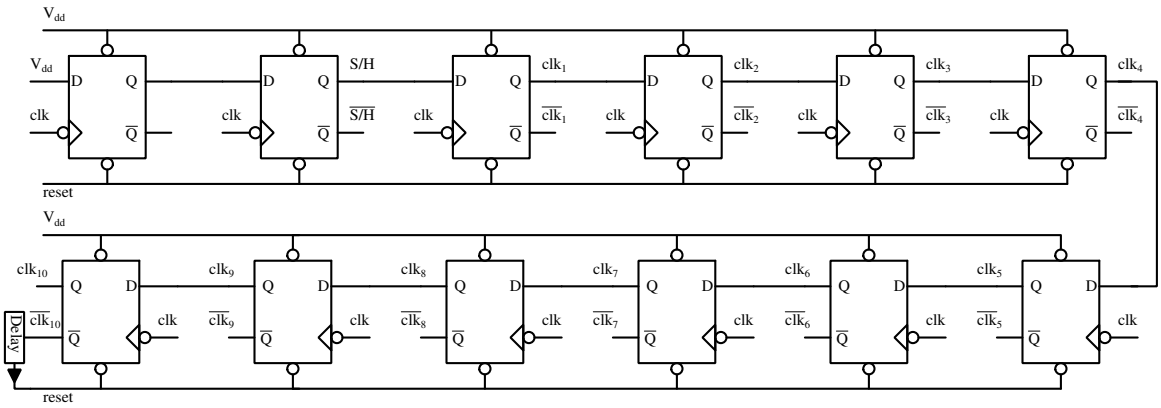


Figure 2.21: Circuit diagram of clock signals for SAR control logic.

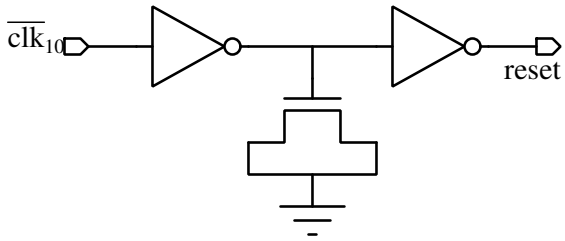


Figure 2.22: Delay circuit.

The charge redistribution takes place when clock is 'low' and ready for comparison at the positive edge of clock cycle.

As shown in figure 2.21, 12 negative edge asynchronous active low set-reset D–FFs (Flip Flops) are used to produce sample signal and 10 clock cycles (clk_1 to clk_{10}). Initially, all D–FFs are set 'low' by active low *reset* signal. The input of first D–FF is connected to V_{dd} and the output is connected to next D–FF input so that it produces clk_n in n^{th} clock cycle. From delayed $\overline{clk_{10}}$, *reset* signal is generated. The circuit diagram for delay cell is shown in figure 2.22. Here, the pulse width of *reset* signal can be controlled by the dimensions of mos transistor used in delay circuit. Also, the schematic circuit diagram for D–FF is shown in figure 2.23. All transistors are with minimum dimensions. The generated sample and hold signals are complementary to each other. These two signals should not overlap with each other to ensure the proper operation. The non-overlapped sample and hold signals are produced from sample signal using a circuit as shown in figure 2.24.

The switches in feedback capacitive DAC implemented with PMOS and NMOS transistors accordingly, i.e. when the control signal is '0', the capacitor is connected

Table 2.3: Switch logic.

clock cycle	sample	DACP	DACN	D_{out}
1	1	000000000 11111111	000000000 11111111	-
2	1	000000000 11111111	000000000 11111111	-
3	0	000000000 11111111	000000000 11111111	D_9
4	0	$D_9$00000000 $D_9$1111111	$\overline{D_9}$00000000 $\overline{D_9}$1111111	D_8
5	0	$D_9D_8$0000000 $D_9D_8$111111	$\overline{D_9}$ $\overline{D_8}$0000000 $\overline{D_9}$ $\overline{D_8}$111111	D_7
6	0	$D_9D_8D_7$000000 $D_9D_8D_7$11111	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$000000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$11111	D_6
7	0	$D_9D_8D_7D_6$00000 $D_9D_8D_7D_6$1111	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$00000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$1111	D_5
8	0	$D_9D_8D_7D_6D_5$0000 $D_9D_8D_7D_6D_5$111	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$0000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$111	D_4
9	0	$D_9D_8D_7D_6D_5D_4$000 $D_9D_8D_7D_6D_5D_4$11	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$11	D_3
10	0	$D_9D_8D_7D_6D_5D_4D_3$00 $D_9D_8D_7D_6D_5D_4D_3$1	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$00 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$1	D_2
11	0	$D_9D_8D_7D_6D_5D_4D_3D_2$0 $D_9D_8D_7D_6D_5D_4D_3D_2$	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$0 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$	D_1
12	0	$D_9D_8D_7D_6D_5D_4D_3D_2D_1$ $D_9D_8D_7D_6D_5D_4D_3D_2$	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$ $\overline{D_1}$ $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$	D_0

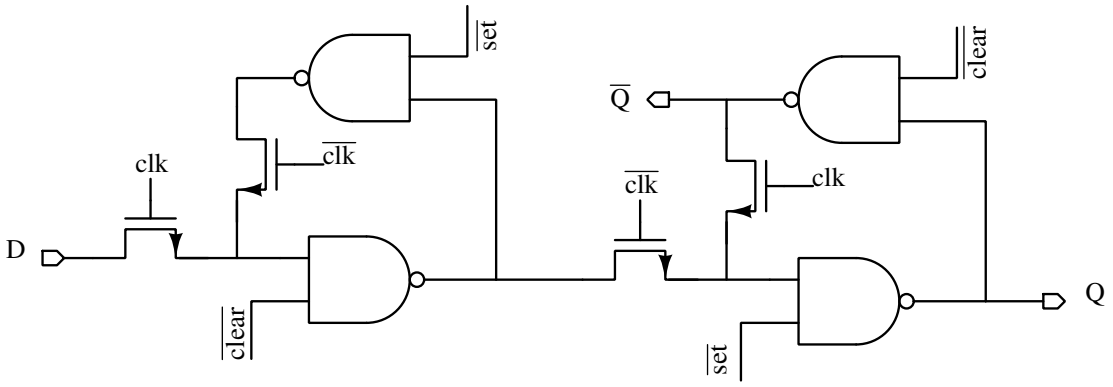


Figure 2.23: Circuit diagram of D Flip-flop.

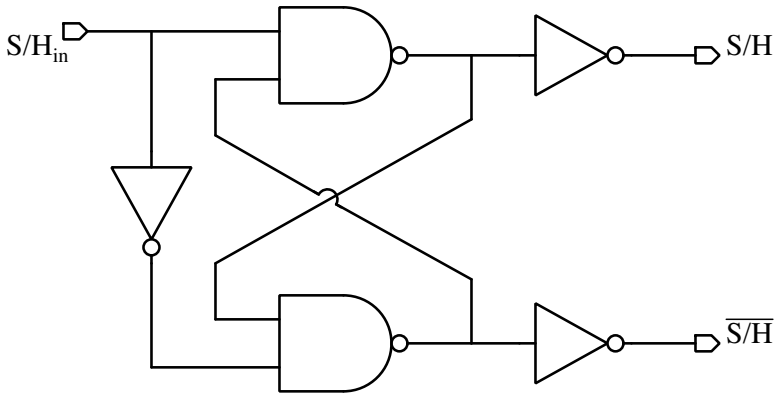


Figure 2.24: Non overlapping signals generation circuit.

to V_{dd} through PMOS transistor and if it is '1', the capacitor is connected to *Gnd* through NMOS transistor. Table 2.3 shows the control signals for both DACP and DACN in each and every clock cycle. The control logic is implemented by utilizing total 18 D–FFs as shown in figure 2.25. Initially, the *reset* signal set 9 D–FFs to 'high' and other 9 D–FFs to 'low'. The comparator output is connected to the input of all D–FFs. Thus, the output bit is stored on corresponding D–FF on arrival of positive edges of clock cycles from clk_1 to clk_{10}. Finally, when positive edge of clk_{10} arrives, the 10-bit digital code transferred and stored into PIPO register till the next sample output comes out. The schematic circuit diagram of PIPO register is shown in figure 2.26.

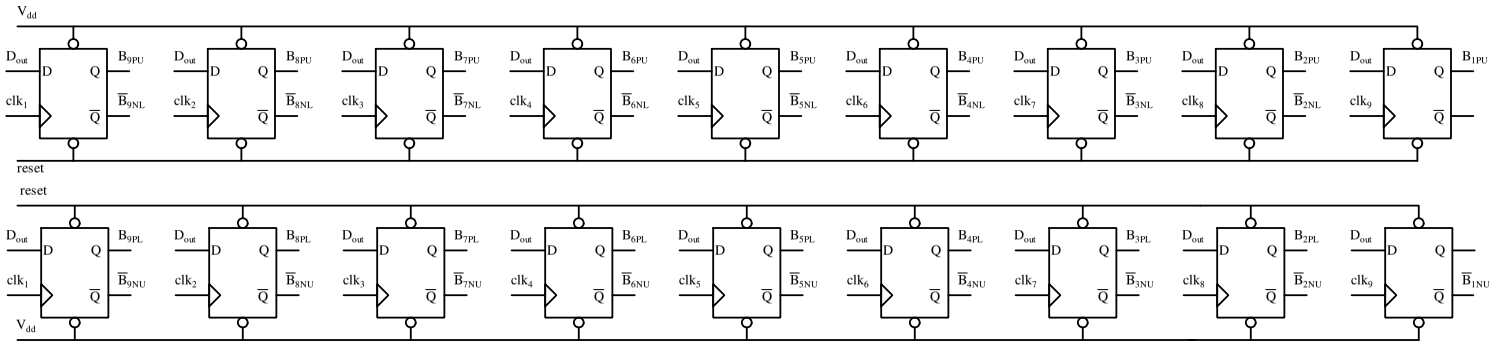


Figure 2.25: SAR ADC switch logic circuit diagram.

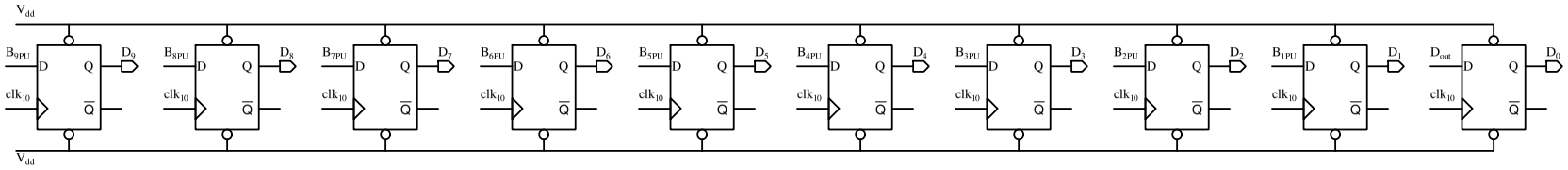


Figure 2.26: PIPO register circuit diagram.

2.4 Results

2.4.1 Proposed SAR ADC simulation results with an example of 10-bit resolution

A 10-bit proposed SAR ADC is designed and simulated in cadence using UMC 90 nm CMOS 1P9M process technology with supply voltage of 0.5 V. A 1 V peak to peak sinusoidal signal of frequency 615 Hz is applied as an input to SAR ADC for testing its dynamic characteristics. The sampling frequency is 10 kS/s, therefore, the clock frequency (f_{clk}) is 120 kHz. Here, first two clock cycles used to sample the input signal onto DAC capacitors. After that, the SAR ADC needs 10 cycles for conversion. At the end of 12^{th} clock cycle, the 10-bit data is transferred to PIPO register and *reset* signal is generated. The spectrum of SAR ADC output signal is calculated using fast Fourier transform (FFT) and plotted as shown in figure 2.27. It can be observed that, the noise floor is roughly -100 dB and it includes both noise as well as harmonics. The total harmonic distortion is found to be around -75.53 dB. The proposed SAR ADC has achieved 55.93 dB SNDR and it is equivalent to ENoB of 9 bits. The spurious free dynamic range (SFDR) of SAR ADC is calculated and it is 77.17 dB.

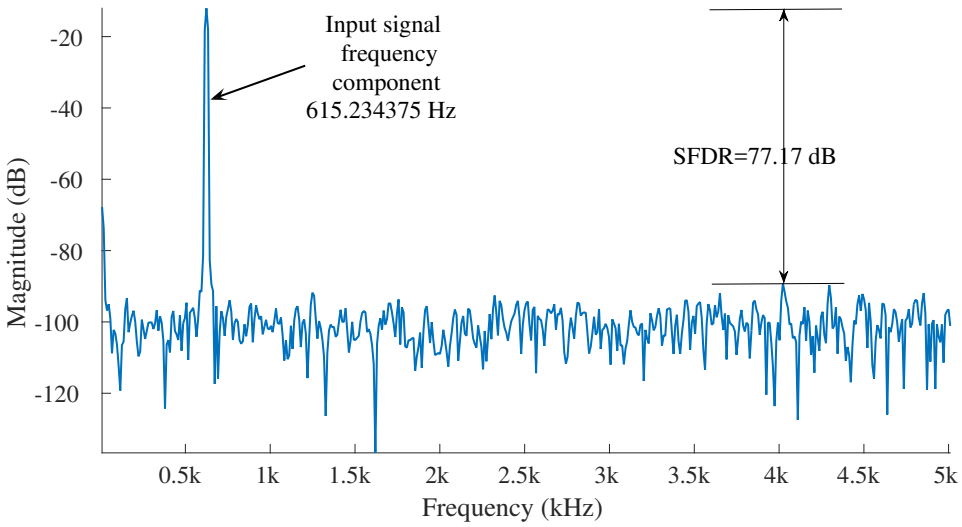


Figure 2.27: Spectrum of SAR ADC output signal.

The power consumption of SAR ADC and its sub blocks is calculated individually. The energy per conversion for each digital output sequence is calculated and plotted in

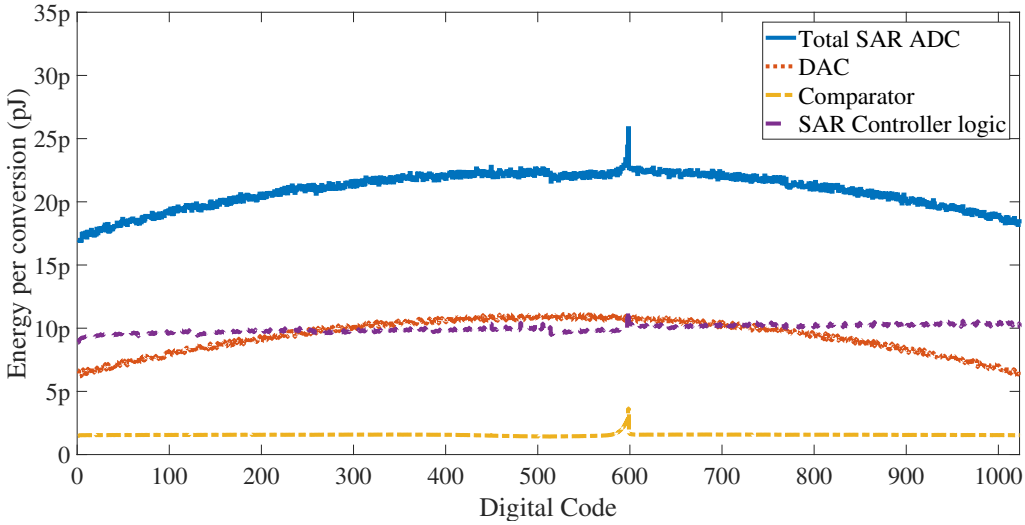


Figure 2.28: Energy Consumption per code of SAR ADC.

figure 2.28. It is observed that, the average energy per conversion for integrated SAR ADC is 19.8 pJ. This energy is distributed among SAR ADC sub blocks as 8.79 pJ, 1.56 pJ, 9.46 pJ for capacitive DAC, comparator, SAR controller block respectively. The SAR ADC is operated at 10 kS/s so that the average power consumption is calculated as 198.4 nW. The sub blocks - capacitive DAC, comparator, SAR controller block consume 87.9 nW, 15.6 nW and 94.6 nW respectively.

Figure 2.29 shows that, the percentage of power distribution among SAR ADC sub blocks. One can observe that, the feedback capacitive DAC power consumption is around 44 % and rest of the blocks - comparator, SAR controller logic blocks consumes around 8 % and 48 % of total SAR ADC power consumption respectively. The Walden figure of merit (FoMW) (Walden 1999) is calculated using equation (A.15) and it is 38.67 fJ/conv. The performance metrics of the proposed SAR ADC are tabulated in Table 2.4.

2.4.2 Summary

A novel, energy-efficient differential switching scheme for feedback DAC used in SAR ADC is proposed to reduce the power consumption as well as area. The proposed switching scheme utilizes single reference voltage V_{cm} (i.e. $0.5V_{ref}$) and improves the switching energy efficiency. The proposed switching scheme is 96.88 % energy efficient and 50 % capacitor area efficient than conventional switching scheme. A 10-bit SAR

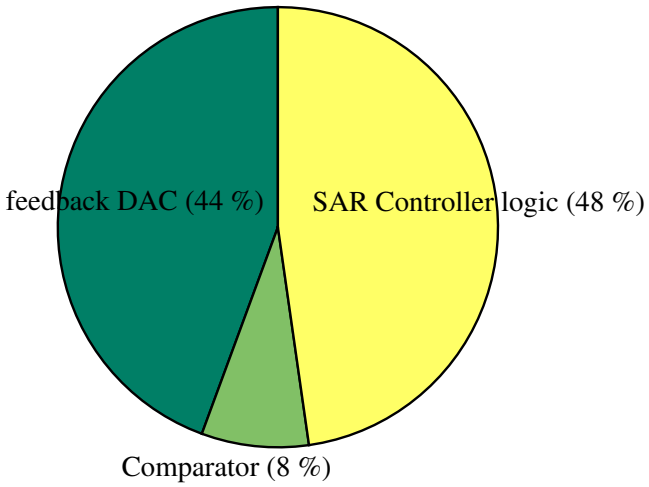


Figure 2.29: Distribution of the proposed 10-bit SAR ADC Power consumption.

Table 2.4: Proposed 10-bit SAR ADC performance metrics.

Performance metrics	Value
Process Technology	UMC 90 nm
Resolution	10-bits
Supply Voltage	0.5 V
Input signal bandwidth	1 kHz
Sampling frequency (f_s)	10 kS/s
SFDR	77.17 dB
THD	-75.5322 dB
SNDR	55.93 dB
Average power consumption	198.4 nW
FoMW	38.67 fJ/conv

ADC is designed and simulated in UMC 90 nm CMOS 1P9M process technology with supply voltage of 0.5 V. The proposed SAR ADC achieves 55.93 dB SNDR, which is equivalent to ENoB of 9 bits. The obtained SFDR for SAR ADC is 77.17 dB. The FoMW is found to be 38.67 fJ/conv.

Chapter 3

A switched capacitor based SAR ADC employing a passive reference charge sharing and charge accumulation technique

A SAR ADC comprises of feedback DAC, comparator and successive approximation logic. Typically, the feedback DAC is implemented with binary weighted capacitors for high accuracy in a conventional SAR ADC. However, one important point worth mentioning is that the number of capacitors and energy consumption are exponentially related to ADC resolution (N-bits) in binary weighted capacitor DAC. Capacitor mismatch is a critical issue in high resolution ADCs employing large number of capacitors, leading to distortion. Also, it uses charge redistribution technique, in which the charge required for conversion is derived from reference voltage for every bit of the decision. This causes distortion in ADC output due to signal-dependent inaccuracies associated with the reference voltage.

A switched capacitor based SAR ADC employing a passive reference charge sharing and accumulation technique is proposed in this chapter. Here, the feedback DAC is implemented with a switched capacitor integrator and an extra capacitor for sampling the reference voltage at the start of conversion. All the charge required for a conversion is drawn in a single cycle from reference voltage and the conversion is performed passively. By drawing all the charge at the beginning of conversion, this charge sharing technique is less prone to any signal-dependent inaccuracies associated

with the reference voltage. Also, the proposed SAR ADC consumes equal energy for all the codes, unlike most other SAR architectures, where the DAC switching energy is dependent on the code, which causes non-linearity due to reference instability. A 11-bit SAR ADC is designed and laid out in UMC 180 nm CMOS technology with a supply voltage of 1.8 V.

3.1 Charge sharing and accumulation based SAR ADC

The conventional SAR ADC is implemented using a sample and hold (S/H), comparator, SIPO register and N-bit feed back DAC blocks as shown in figure 3.1a. Here, f_s is sampling frequency and N is resolution of ADC. In the proposed work, the N-bit feedback DAC is implemented with a 1-bit DAC and discrete time integrator as shown in figure 3.1b. The discrete time integrator accumulates the scaled reference voltage after every comparison cycle from 1-bit DAC and refreshes in each sampling phase. Thus, it fulfills the functionality of an equivalent N-bit DAC.

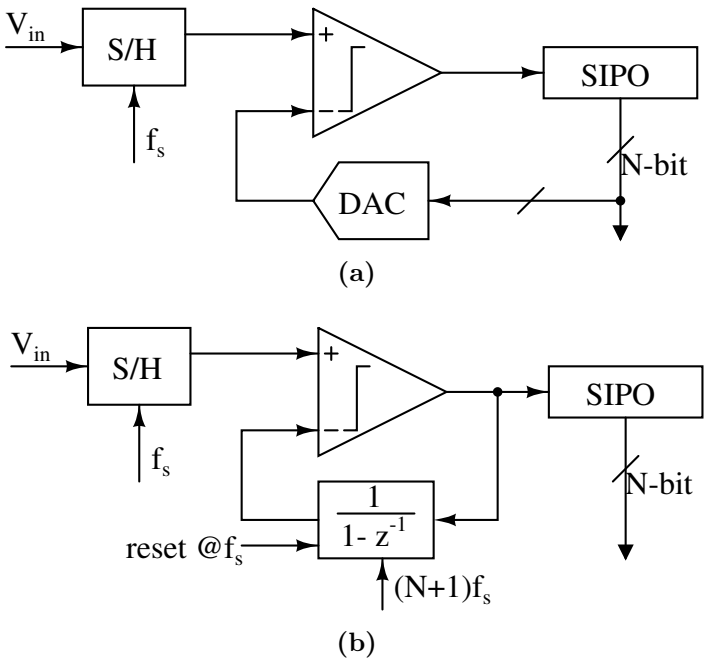


Figure 3.1: (a) SAR ADC block diagram, (b) SAR ADC with feedback integrator DAC.

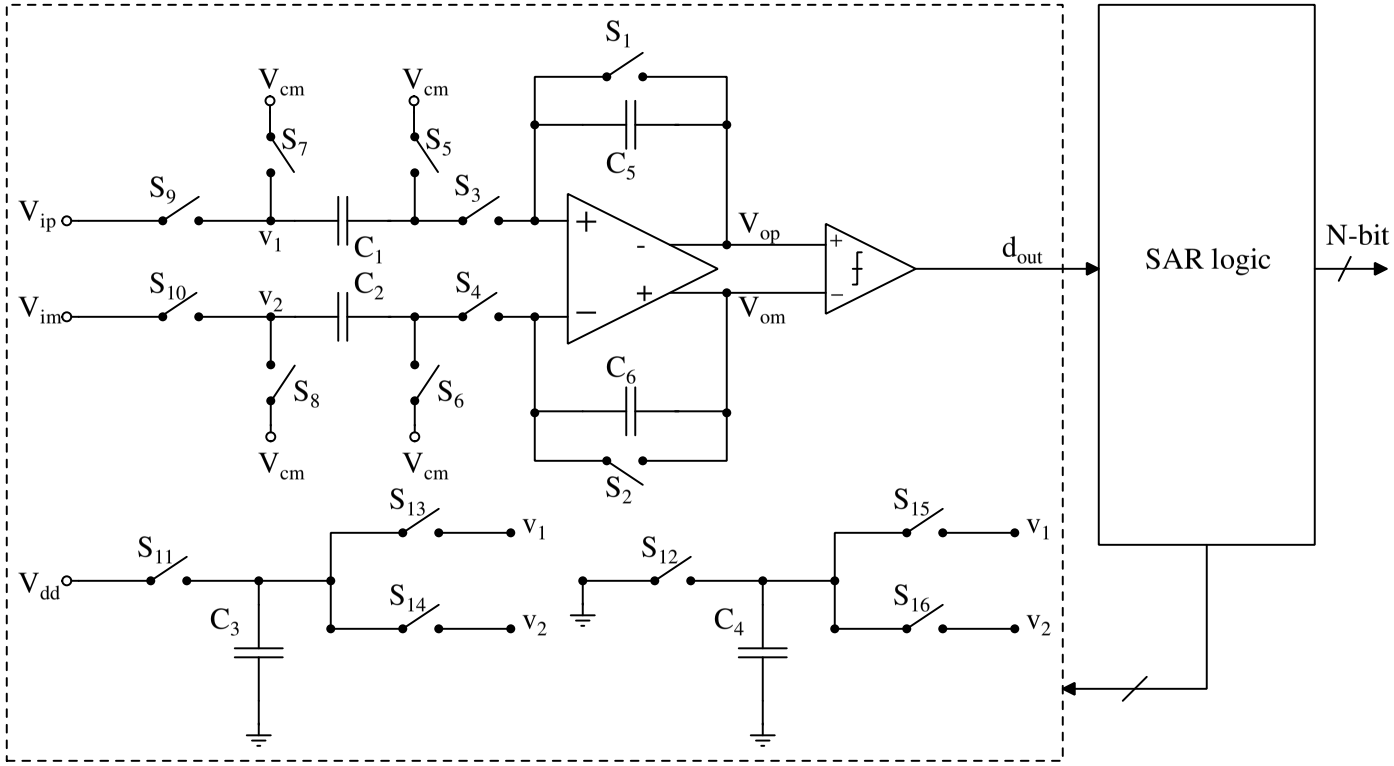


Figure 3.2: Charge sharing and accumulation based SAR ADC architecture.

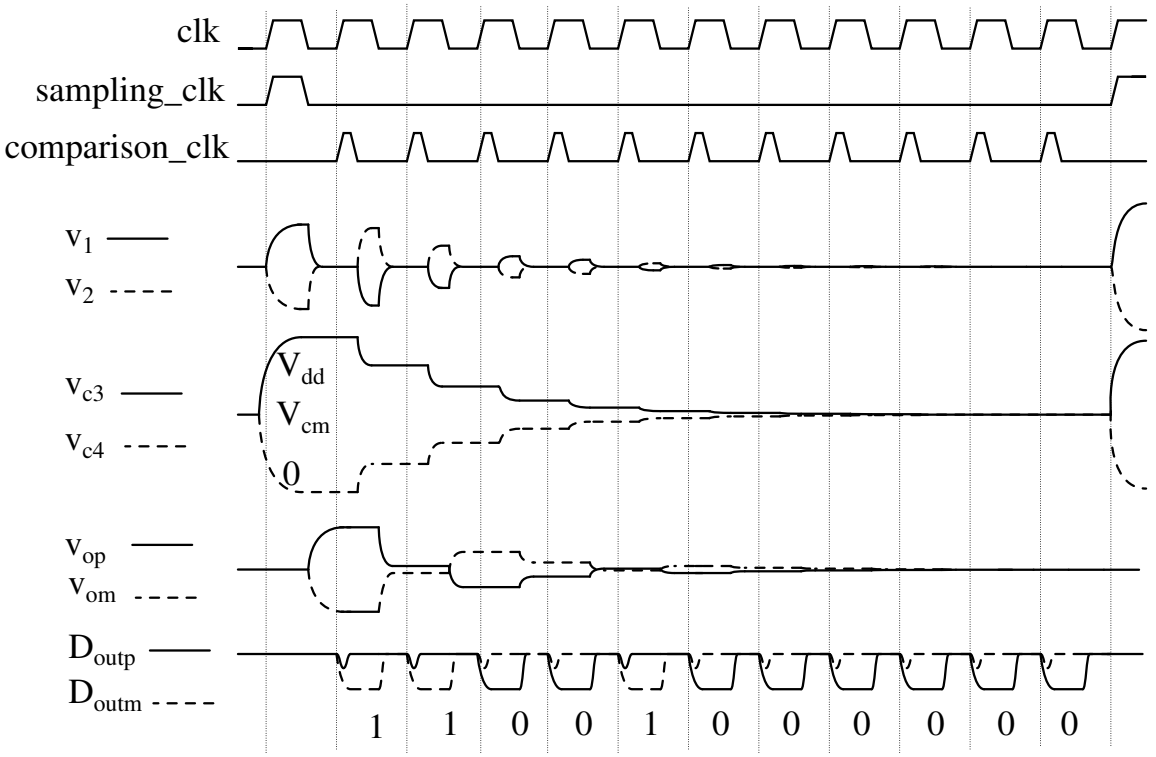


Figure 3.3: Timing waveform of the proposed SAR ADC operation.

The architecture of charge sharing and accumulation based SAR ADC is shown in figure 3.2. This architecture is implemented by using a fully differential OTA, comparator, 6 capacitors and 16 switches. Figure 3.3 shows timing diagram of the proposed SAR ADC operation. Algorithm 1 briefly explains the proposed SAR conversion procedure. This architecture takes N+1 clock cycles for one sample conversion. An active low *reset* signal is used to reset the circuit and the conversion starts when *reset* is high. In the sampling phase, when the sampling clock is high, switches S_1, S_2, S_5, S_6, S_9, S_{10}, S_{11} and S_{12} are 'ON' enabling the capacitors C_1 and C_2 to sample the differential input signals V_{ip} and V_{im} respectively, while capacitor C_3 charges to V_{dd} and C_4 discharges to *Gnd*. Also, the switches across the capacitors C_5 and C_6 are 'ON' and thereby neutralizing the positive and the negative charge between them.

In the next phase, also known as accumulation phase, switches S_3, S_4, S_7 and S_8 are 'ON' and the rest of the switches are 'OFF'. Because of the virtual short between the two OTA inputs, the charge on C_1 and C_2 shifts to capacitors C_5 and C_6 respectively. The OTA output voltages are given by, V_{op} $(= V_{ip} + V_{cm})$ and V_{om} $(= V_{im} + V_{cm})$, where $V_{cm} = V_{dd}/2$ is the common mode voltage. They are then compared using a

strongARM dynamic comparator and the decision is stored in a SIPO register of the SAR logic.

In the next cycle, based on the comparator output, capacitors C_1, C_2, C_3 and C_4 share the charge. If the comparator output is '0', capacitors C_1, C_3 share the charge through switch S_{13}. Initially, the capacitor C_3 is charged to V_{dd} and the charge on C_1 is '0'. Therefore, by applying charge conservation principle on node v_1 (left of the capacitor C_1),

$$\begin{aligned} C_3 V_{dd} &= C_3 v_1 + C_1 (v_1 - V_{dd}/2) \\ v_1 &= \frac{C_3 + C_1/2}{C_3 + C_1} V_{dd} \end{aligned} \tag{3.1}$$

Similarly, capacitors C_2 and C_4 share the charge through S_{16}. Initially, the charge on both the capacitors C_2 and C_4 is '0'. By applying charge conservation principle at node v_2 (left of the capacitor C_2),

$$\begin{aligned} 0 &= C_4 v_2 + C_2 (v_2 - V_{dd}/2) \\ v_2 &= \frac{C_2/2}{C_4 + C_2} V_{dd} \end{aligned} \tag{3.2}$$

Algorithm 1 Proposed SAR conversion procedure

1: **set** *ADC Resolution* (N);
2: **while** (reset=1) **do**
3: **start** conversion;
4: **sampling**: $C_1 \leftarrow V_{ip}$, $C_2 \leftarrow V_{im}$, $C_3 \leftarrow V_{dd}$, $C_4 \leftarrow 0$;
5: **while** $N \geq 0$ **do**
6: shift charge: $C_5 \leftarrow C_1$, $C_6 \leftarrow C_2$;
7: compare $V_{op} <> V_{om}$;
8: **return** d_{out};
9: **if** ($d_{out} = 0$) **then**
10: charge sharing: C_1&C_3 and C_2&C_4;
11: **else**
12: charge sharing: C_1&C_4 and C_2&C_3;
13: **end if**
14: N ← N-1;
15: **end while**
16: **return** *digital output*;
17: **end** conversion;
18: **end while**

Since, C_1=C_2=C_3=C_4, equations (3.1) and (3.2) can be written as,

$$v_1 = \frac{3V_{dd}}{4} \quad \text{and} \quad v_2 = \frac{V_{dd}}{4}$$

Thus, in this phase, the capacitors are sharing charge between them and consequently, this phase is referred to as charge sharing phase.

Next, in the accumulation phase, the charge in capacitors C_1, C_2 will accumulate on capacitors C_5, C_6 respectively. Outputs of OTA after these two phases can be written as shown in equations (3.3) and (3.4).

$$V_{op} = \left(\frac{C_1}{C_5}\right)\left(V_{ip} + \frac{V_{dd}}{4}\right). \tag{3.3}$$

$$V_{om} = \left(\frac{C_2}{C_6}\right)\left(V_{im} - \frac{V_{dd}}{4}\right). \tag{3.4}$$

The comparator triggers at the negative edge of accumulation phase and compares V_{op} with V_{om}. The comparator gives out '0' or '1' depending upon $V_{op} < V_{om}$ or $V_{op} > V_{om}$ respectively. This comparison of V_{op} and V_{om} can be interpreted as $V_{ip} - V_{im} <> -V_{dd}/2$, if the output bit in previous cycle is '0'. Here, the symbol <> represents comparison (i.e. lesser or greater). On the other hand, if the comparator bit is '1' in the previous cycle, capacitors C_1 and C_4 share charge through switch S_{14} while capacitors C_2 and C_3 share charge through switch S_{15} and the comparison of V_{op} with V_{om} can be interpreted as $V_{ip} - V_{im} <> V_{dd}/2$. Here, $-V_{dd}/2$ and $V_{dd}/2$ are the reference voltage levels in second cycle. As shown in figure 3.3, this process repeats for N cycles and an N-bit digital output is generated at the end of conversion.

Since the proposed architecture uses fewer capacitors compared to the conventional binary weighted capacitive DAC, the non-linearity due to mismatch between the capacitors will be much less. Also, in this architecture, the absolute values of capacitors are determined by the noise considerations, which certainly gives an area advantage compared to conventional binary weighted capacitive DAC where the unit capacitance values are lower bounded by capacitors' mismatch. Secondly, the energy consumption per conversion is same for all codes unlike the existing switching schemes in the case of conventional SAR ADC. The power consumption of this SAR ADC can be derived as shown in equation (3.5).

$$P_{diss} = \underbrace{C_3 V_{dd}^2 f_s}_{\text{DAC}} + \underbrace{I_{bias} V_{dd}}_{\text{OTA}} + \underbrace{(N+1) C_p V_{dd}^2 f_s}_{\text{Comparator}} \tag{3.5}$$

where, f_s is the sampling frequency and C_p is the total parasitic capacitance at the comparator output node.

3.2 Practical considerations

Generally, switched capacitor circuits built using OTAs, switches and capacitors exhibit inherent non-idealities. In the previous section, it is assumed that the OTA has infinite gain, bandwidth and in the accumulation phase entire charge is instantly transferred from one capacitor to the other. However, usually, some charge is left behind in capacitor (e.g., in C_1) which amounts to error voltage known as static error voltage, due to the finite amplifier gain. Also, finite UGB and slew rate limit the speed of charge transfer between the capacitors and cause an error voltage which is known as dynamic error. All these non-idealities are considered and the proposed ADC is modeled using MATLAB. This modeling is explained in this section.

3.2.1 Finite OTA gain

By recollecting the virtual short concept, the inverting terminal of OTA is charged to -v_o/A, which is not exactly zero in an inverting amplifier configuration. This left over charge changes the transfer function of switched capacitor integrator by a small term (Pavan *et al.* 2017). Assume that, the capacitor C_1 is charged to v_{in} in the first phase. During the charge accumulation phase, since the capacitor C_1 is connected to virtual ground, bulk of the charge flows to capacitor C_5 while a residual charge of $-v_o/A$ remains on C_1. Under this condition, the output voltage is given by equation (3.6).

$$v_o = \frac{\frac{C_1}{C_5} v_{in}}{1 + \frac{1}{A}\left(1 + \frac{C_1}{C_5}\right)} \tag{3.6}$$

The term $\frac{1}{A}\left(1 + \frac{C_1}{C_5}\right)$ in the denominator of equation (3.6) causes an integrator gain coefficient error but has negligible effect on linearity of ADC characteristics with large OTA gain(A). However, the residual charge (v_o/A) on C_1 alters the ADC reference levels and causes non-linearity while sharing charge with capacitor C_3 or C_4. To

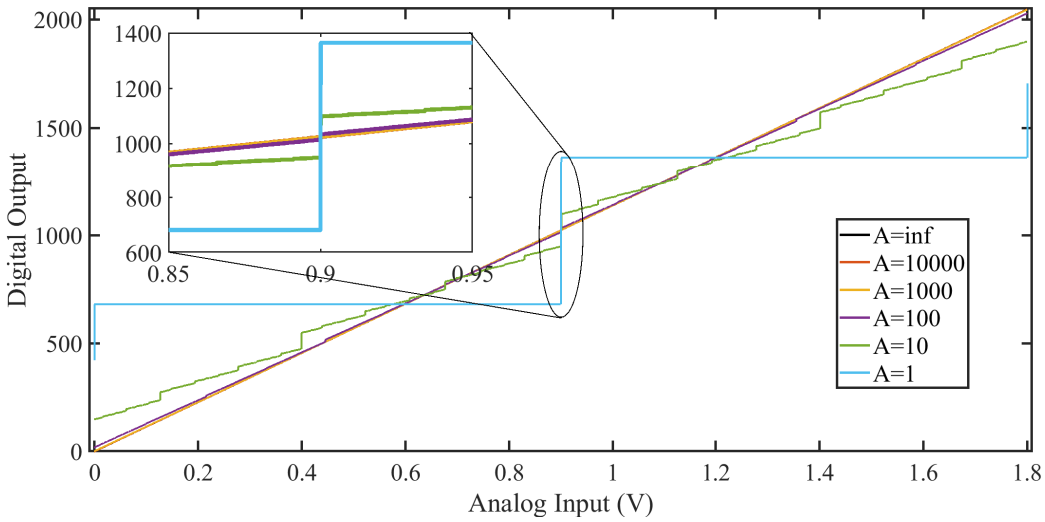


Figure 3.4: ADC transfer characteristics vs. OTA gain.

observe this effect on ADC characteristics, the proposed ADC is modeled in MATLAB and the transfer characteristic is plotted as shown in figure 3.4, for different OTA gains.

The OTA gain has great bearing on ADC linearity and a lower gain results in degraded linearity. The non-linearity in ADC characteristics produces harmonics in the output. To observe this, a sinusoidal signal is fed to the MATLAB model and the total harmonic distortion (THD) is calculated from the output spectrum. Figure 3.5 shows a linear variation of THD with OTA gain. Using curve fitting, the relation between the OTA gain and THD can be approximated as in equation (3.7).

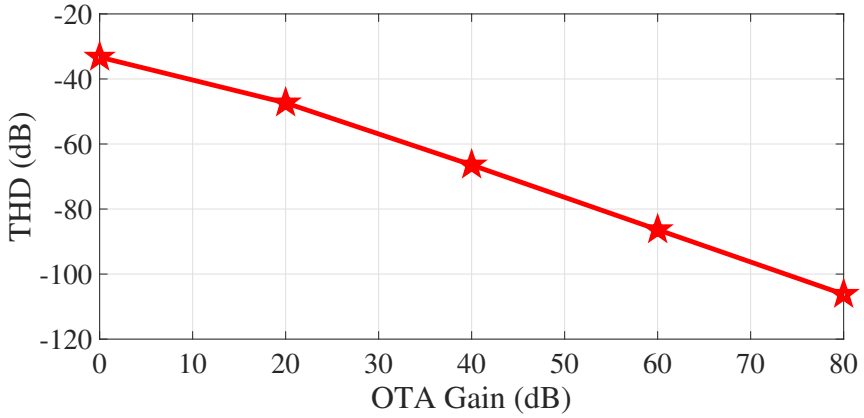


Figure 3.5: THD in ADC characteristics vs. OTA gain.

$$THD = -A_{dB} - 27\ dB \tag{3.7}$$

In all the above discussions, the OTA gain is assumed to be constant for all input voltages but practically the gain reduces for larger input voltages. This variation of gain demands even higher OTA gain to keep the harmonics down.

3.2.2 Finite Settling time considerations

In charge accumulation phase, the integrator with practical OTA takes some settling time to transfer the charge due to finite slew rate and UGB (Quinn and Van Roermund 2007). It is to be noted that the settling time needs to be less than half the clock period for the ADC to operate correctly. Typically, at large inputs, the OTA saturates and the current flows fully in one branch of the differential pair. Clearly, this current (I) should be sufficient to shift the charge from input capacitor(s) to accumulating capacitor(s) within the specified period. This phenomenon is known as slewing and the rate at which the charge transfer happens is called slew rate. Once the OTA input voltage falls under the input range of OTA, the transconductance (g_m) decides the minimum time needed to settle within the required accuracy. This is known as linear settling phase. It is assumed here that, slewing phase exists for x part of $T_{clk}/2$ and rest of $T_{clk}/2$ is taken by the linear settling phase. The boundary conditions for bias current and the transconductance can be derived as follows. The maximum charge that needs to be transferred from capacitor C_1 to C_5 is $C_1 v_{in,max}$ in $xT_{clk}/2$ time and therefore, the bias current should follow the relation as shown in equation (3.8).

$$I > \frac{C_1 v_{in,max}}{xT_{clk}/2} \tag{3.8}$$

In linear settling phase, the OTA gain in $s-$domain follows as in equation (3.9), where τ is considered to be time constant of an integrator small signal model in charge integration phase. Figure 3.6 shows the equivalent circuit of small signal model of an integrator in charge integration phase and τ can be calculated as shown in equation (3.10).

$$A(s) = \frac{A}{1 + s\tau} \tag{3.9}$$

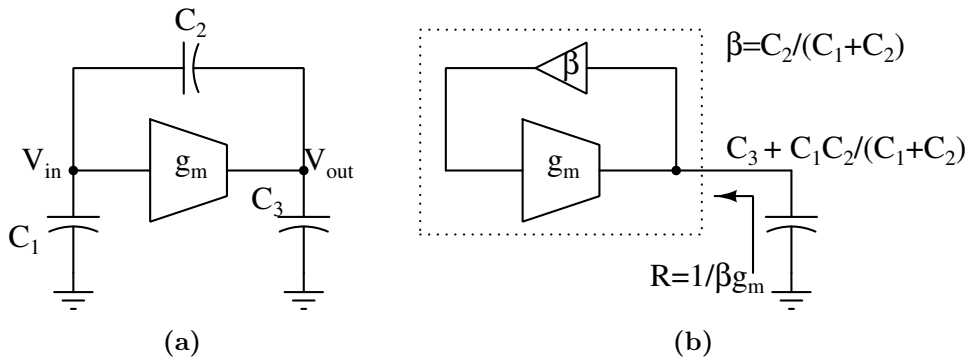


Figure 3.6: Linear settling phase (a) Circuit configuration, (b) Equivalent circuit.

$$\tau = \frac{C_1 + C_L + C_1 C_L / C_5}{g_m} \approx \frac{C_1}{g_m} \tag{3.10}$$

The settling time required to keep normalized error voltage below -100 dB is

$$(1 - x)\frac{T_{clk}}{2} \quad = \quad \tau \ln(10^5) \approx 12\tau \tag{3.11}$$

Therefore, the required OTA transconductance (g_m) can be computed using equation (3.12).

$$g_m = \frac{C_1}{(1 - x)T_{clk}/24} \tag{3.12}$$

From equations (3.8) and (3.12), the relation between g_m/I and x can be derived as in equation (3.13). The MOSFET characterization in UMC 180 nm technology shows that the g_m/I ratio greater than $18\,V^{-1}$ can be achieved in weak inversion region. This allows extra slewing time especially in comparison with linear settling and thereby optimizing the current.

$$\frac{g_m}{I} = \frac{12}{v_{in,max}} \frac{x}{1 - x} \tag{3.13}$$

3.2.3 Parasitic capacitances

The switched capacitor integrator circuit used in this work is often known as parasitic-insensitive (Pavan *et al.* 2017), because the transfer function is not significantly im-

pacted by parasitic capacitances from the switch terminals to *Gnd*. To strengthen this argument, consider a parasitic capacitance on the left terminal of capacitor C_1. This parasitic capacitance charges to input sample in the first half of clock cycle and again charges to V_{cm} in the second half of clock cycle. Similarly, the parasitic capacitance on the right side of capacitor C_1 is connected to either V_{cm} in the first half of clock cycle or inverting terminal of OTA (virtual common mode) in the second half of clock cycle. Since, any of the charge in these two parasitic capacitors is not accumulating on to integrating capacitor C_5 , the transfer function remains the same irrespective of parasitic capacitances. Nevertheless, the OTA output node parasitic capacitances add to the load capacitance and change UGB and slew rate to some extent. The parasitics of capacitors C_1, C_2, C_3 and C_4 play a significant role in conversion accuracy since these are involved in charge sharing and reference voltage generation. However, these parasitic effects can be minimized by matching the capacitors $C_1 - C_4$ with proper layout.

3.2.4 Noise Analysis

In an analog circuit, every transistor contributes noise. Switches and OTA circuit are the primary noise sources in the proposed ADC circuit. The power spectral density (PSD) of thermal noise due to a switch is shown by equation (3.14).

$$S_{n,sw}(f) = 4kTR_{on}\ V^2/Hz \tag{3.14}$$

where, k is Boltzmann constant, k = 1.38 x $10^{-23}\,J/K$, R_{on} is the switch 'ON' resistance and T is absolute temperature in Kelvin (^{o}K).

The input-referred noise spectral density of folded cascode (FC) OTA shown in figure 3.8 is given by equation (3.15).

$$S_{n,OTA}(f) = \frac{16kT}{3g_{m1}}\left(1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m10}}{g_{m1}}\right) \tag{3.15}$$

Figure 3.7 shows the noise models for single ended circuit of SC integrator. In sampling mode, thermal noise of switches S_1 and S_2 accumulates on the capacitor C_1 and the mean square noise is given by equation (3.16).

$$\overline{v_{c1}^2} = \frac{kT}{C_1} \tag{3.16}$$

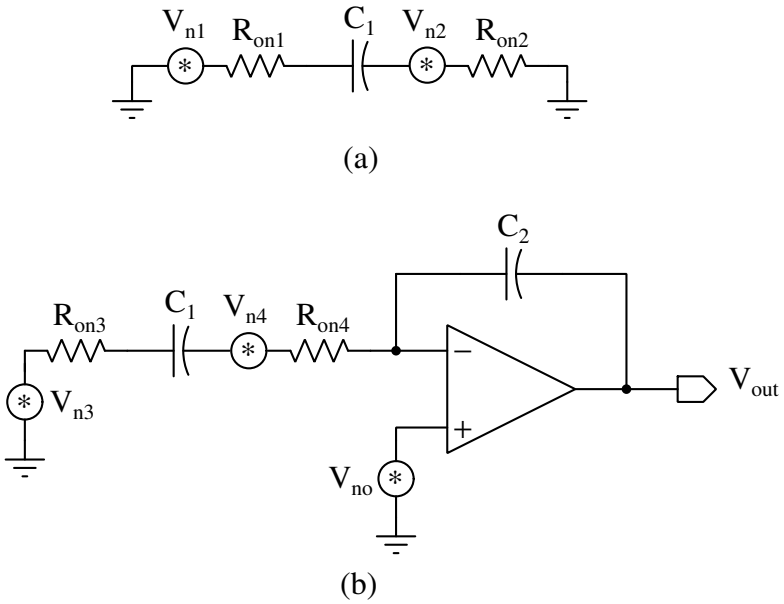


Figure 3.7: Noise analysis (a) Sampling mode, (b) Accumulation mode (Schreier *et al.* 2005).

In the accumulation mode, the mean square noise on capacitor C_1 due to switches S_3, S_4 and the OTA input-referred noise through the capacitive feedback (Schreier *et al.* 2005) are as follows:

$$\overline{v_{c1,sw}^2} = \frac{S_{n,sw3} + S_{n,sw4}}{4\tau} = \frac{8kTR_{on}}{4(2R_{on} + 1/g_{m1})C_1} \tag{3.17}$$

$$\overline{v_{c1,OTA}^2} = \frac{4kT}{3(2R_{on}g_{m1} + 1)C_1}\left(1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m10}}{g_{m1}}\right) \tag{3.18}$$

The noise accumulated on capacitor C_1 at the end of sampling mode is v_{c1} while in accumulation mode, the noise is contributed by both OTA and switches. Since the three components of the noise power are uncorrelated, the total noise power is sum of all noise powers, given by equation (3.19).

$$\overline{v_{c1}^2} = \frac{kT}{C_1}\left(1 + \frac{x}{x+1} + \frac{4/3}{1+x}\left(1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m10}}{g_{m1}}\right)\right) \tag{3.19}$$

where, $x = 2R_{on}g_{m1}$. If $x \gg 1$ (i.e., $g_{m1} \gg 1/R_{on}$), then the resulting noise can be approximated to be equal to $2kT/C_1$. OTA's noise term is negligible, as it is inversely proportional to g_{m1}. Due to the sampling process the noise will be aliased. This noise folding due to aliasing increases the power spectral density (PSD) of noise but the

mean square value of sampled noise remains the same.

3.3 Building blocks

The major building blocks of proposed SAR ADC are OTA, comparator, boot strapped switch and SAR logic. The design of each of these blocks is discussed in this section.

3.3.1 Operational Transconductance Amplifier (OTA)

OTA is an important building block often used in the design of analog and mixed signal processing systems like ADC, switched capacitor filters, front-end amplifiers and more. The intrinsic gain of transistor tends to reduce rapidly due to a gradual decrease of feature size in deep sub-micron technology and results in a significant reduction in an amplifier's DC gain. To achieve a high DC gain with low bias current, operating a transistor in weak inversion region is a feasible option. Among the numerous OTA architectures (Allen *et al.* 1987), FC OTA is most suitable for high gain applications because, the folding connection at the middle of input differential pair and the complementary cascode transistor source allows a large input common-mode range, while the cascoded current source in the output branch offers a high impedance at the output node, which results in large OTA gain.

Figure 3.8 shows the complete schematic circuit of FC OTA. It includes differential-in differential-out FC OTA, common mode feedback circuit, bias generation circuit as well as a beta multiplier circuit. The capacitance ratio (C_1/C_5) is chosen to be 0.3 so that the required peak-to-peak output swing of the OTA becomes $0.54\,V$ for a $1.8\,V$ peak-to-peak input signal. This allows approximately $0.6\,V$ to operate each one of the PMOS and NMOS cascode current sources in saturation. Since, the cascode transistors (M6, M7, M8, M9) would not contribute any noise to the output, a large portion of the voltage ($0.4\,V$) is allocated to the current sources (M4, M5, M10, M11) to reduce noise contribution by them. Further, for UMC 180 nm technology, it is found that g_m/I_D in sub threshold region is around $23\,V^{-1}$ for V_{dd}=$1.8\,V$ and therefore, the value of x in equation (3.19) is determined as 0.775. Further, the required slew rate and UGB are calculated as $0.12\,V/\mu$s and 0.43 MHz using equations (3.8) and (3.12) respectively. With these specifications, the FC OTA is designed using g_m/I_D technique (Jespers 2009) and the transistor sizes are computed and listed in table 3.1.

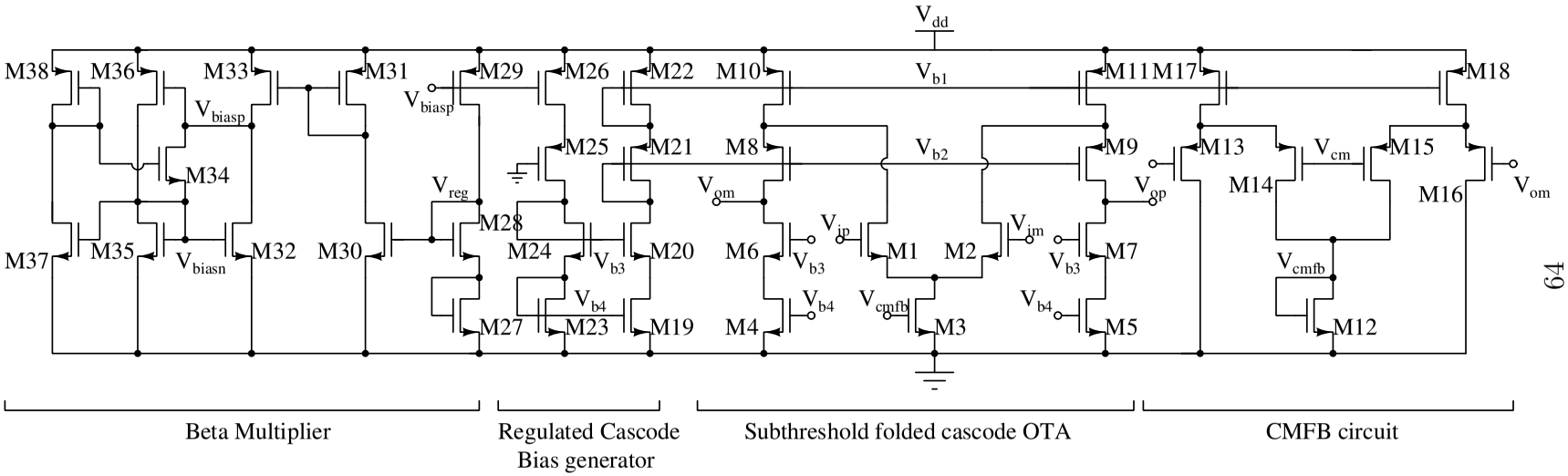


Figure 3.8: Complete schematic circuit of FC OTA.

Table 3.1: Transistor sizes of FC OTA of figure 3.8.

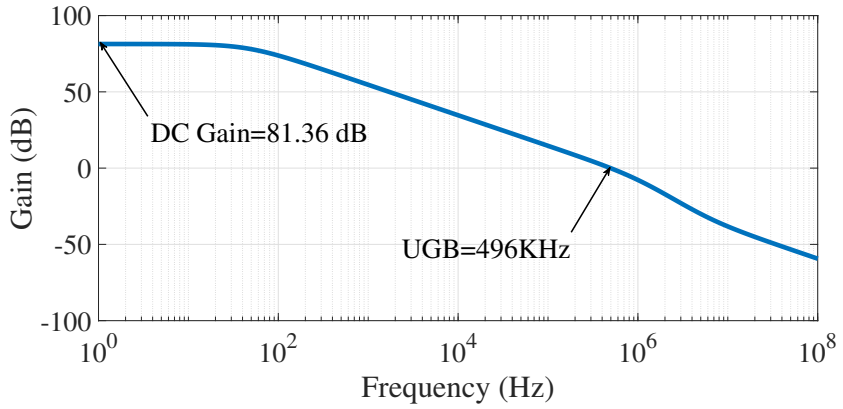
Transistor	Fingers	W(μm)/L(μm)
M_1, M_2	10	25/5
M_3	20	25/5
M_4, M_5, M_6, M_7	12	25/5
M_8, M_9	12	8/0.5
M_{10}, M_{11}	22	18/1
M_{12}	2	25/5
M_{13}, M_{14}, M_{15}, M_{16}	1	8/0.5
M_{17}, M_{18}	2	18/1
M_{19}, M_{20}, M_{23}, M_{24}	10	25/5
M_{21}, M_{25},	10	8/0.5
M_{22}, M_{26}	10	18/1
M_{27}, M_{28}	14	0.5/0.5
M_{29}, M_{31}, M_{33}, M_{36}	2	0.5/0.5
M_{30}, M_{32}, M_{35}, M_{37}	2	0.5/0.5
M_{34}	2	1.6/0.5
M_{38}	2	0.24/0.5

The transistors used in the design have large sizes to reduce flicker noise and transistor mismatch.

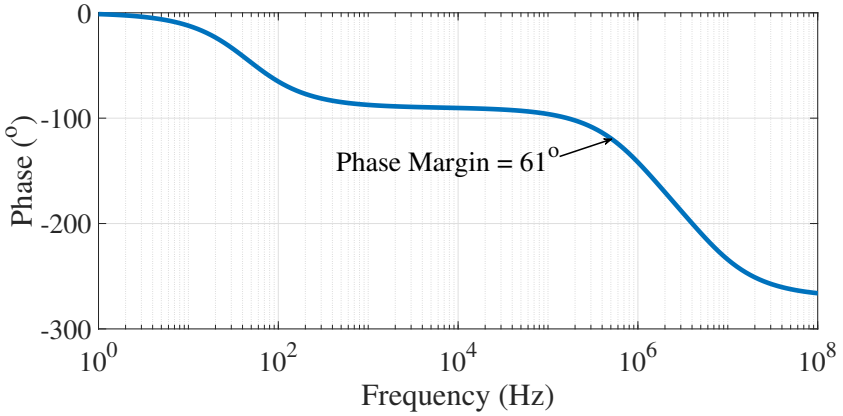
The FC OTA is laid out carefully and post–layout simulations are performed. Figure 3.9 shows the frequency response of the extracted design. OTA exhibits a DC gain of 81.36 dB and UGB of 0.5 MHz while offering a phase margin of 61^o. Further, the variation of DC gain over an output swing is plotted in figure 3.10 and it shows that the DC gain varies less than 0.5 dB over $\pm 0.5\,V$ output swing. Also, it is observed that the OTA gain is above 81 dB for all process corners except for slow-slow (ss) corner in which it is 79.7 dB. Figure 3.11 shows the plot of power spectral density of input refereed noise of FC OTA.

3.3.2 Switches

The proposed programmable resolution ADC consists of a total of 16 switches. It is required to consider the effects like charge injection, clock feed-through and gate voltage dependent resistance while implementing switches, to reduce harmonic dis-



(a)



(b)

Figure 3.9: AC analysis of FC OTA, (a) Magnitude response, (b) Phase response.

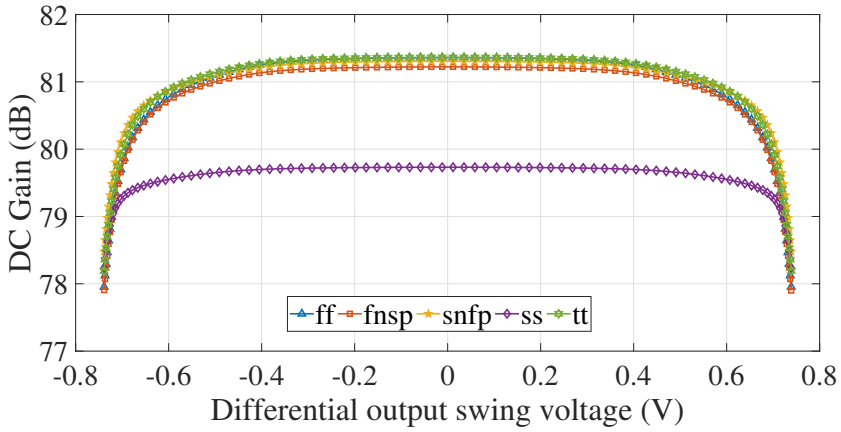


Figure 3.10: DC gain vs. output swing of FC OTA.

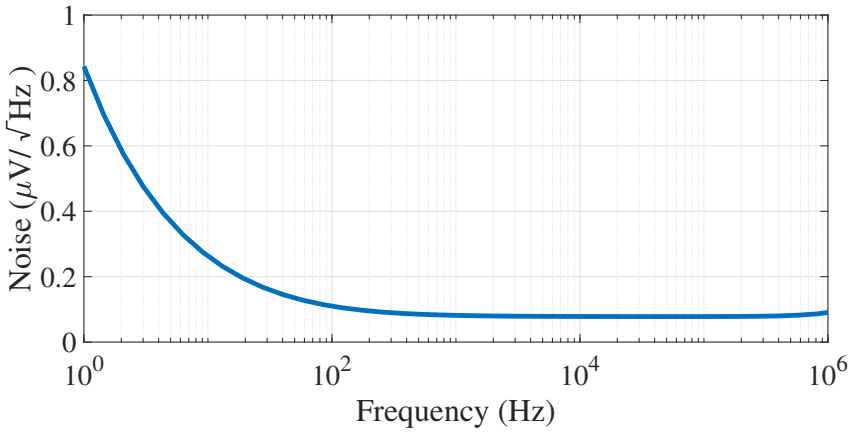


Figure 3.11: FC OTA input referred noise.

tortion. The NMOS transistor can switch 'ON' for voltages below V_{dd} - V_{thn} and the PMOS transistor can switch 'ON' for voltages above $|V_{thp}|$ without distortion. In other cases, transmission gate is used as a switch when node voltages swing between 0 and V_{dd}. Sampling switches S_9, S_{10} and S_3, S_4 are implemented using bootstrapped switch (Razavi 2015) to reduce the input dependent non-linearity. The circuit diagram of boot strapped switch is shown in figure 3.12. Switches S_1, S_2, S_5, S_6, S_7, S_8, S_{12}, S_{15} and S_{16} are implemented with NMOS transistors and S_{11}, S_{13} and S_{14} are implemented using PMOS transistors. Further, to reduce the effects of clock feed through and charge injection on conversion, the techniques like dummy transistors,

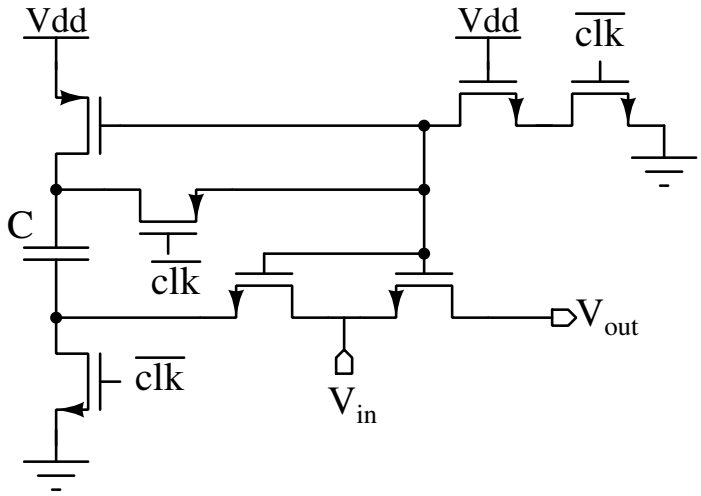


Figure 3.12: Bootstrapped switch circuit diagram.

non overlapping clocks and bottom plate sampling are used. Figure 3.13 shows the output spectrum of bootstrapped circuit, which ensures that all harmonics are less than -100 dBc.

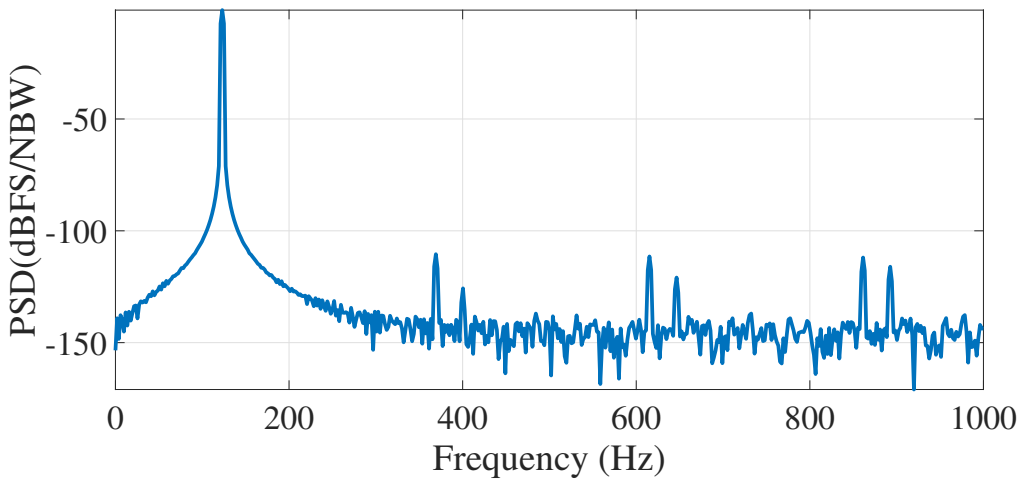


Figure 3.13: Bootstrapped switch output spectrum.

3.3.3 Comparator

The comparator plays a crucial role in ADC designs. Numerous architectures for latch based comparators are reported in the literature. The schematic diagram of a strongARM comparator (Babayan-Mashhadi and Lotfi 2014) is shown in figure 3.14, which is generally used in ADCs because of its positive feedback, high input impedance, rail-to-rail output swing and negligible static power consumption. In reset phase, the *clk* signal is low, thus, the transistor M3 is in 'cut-off' region and the output nodes *outp*, *outm* charge to V_{dd} through the transistors M8 and M9 respectively. When *clk* signal goes *high*, the decision phase starts and output nodes start discharging at different rates depending upon the input voltages V_{ip} and V_{im}. Meanwhile, when one of the output nodes reaches $V_{dd} - |V_{thp}|$, corresponding transistor M6 or M7 switches 'ON' and the positive feedback between back-to-back connected inverters (M4, M6 and M5, M7), also known as latch, enables and pulls one of the output nodes to V_{dd} and other to *gnd*.

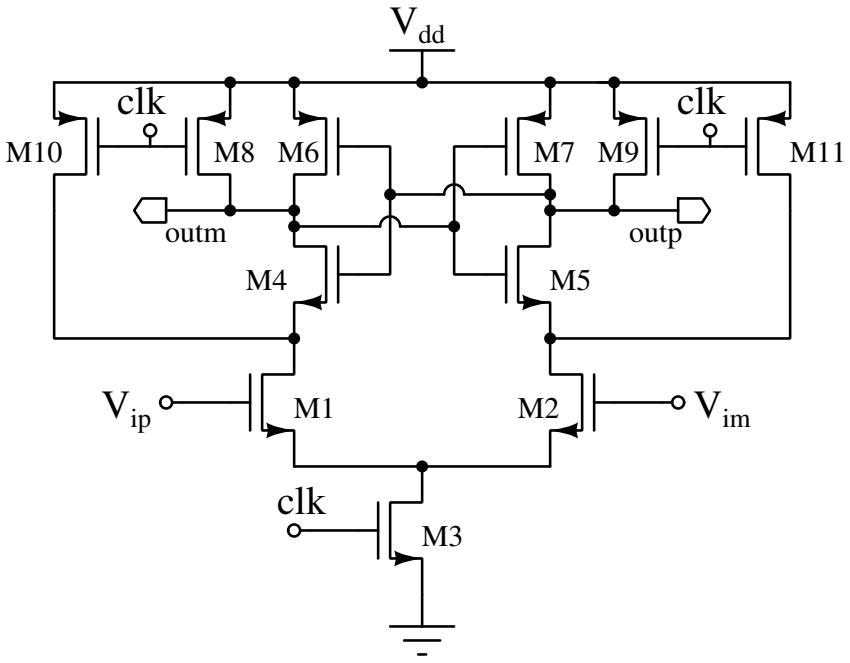


Figure 3.14: StrongARM comparator circuit diagram.

3.3.4 SAR logic

The SAR logic shown in figure 3.2 consists of two blocks, SIPO and switch control logic. This takes the digital output of the comparator and decides which all switches need to be turned 'ON' in the next phase. It also stores the comparator output in SIPO register. At the end of $(N+1)^{th}$ clock cycle, it generates end of conversion (EoC) signal and gives out the N-bit digital output. This logic is coded in verilog-A and synthesized.

3.4 Results and discussion

The proposed SAR ADC design is laid out in UMC 180 nm 1P6M CMOS technology and it occupies an active area of 568 μm x 298 μm as shown in figure 3.15. The layout is made as compact and symmetric as possible using common centroid layout matching technique to reduce the mismatch effects. The total power consumption of the design is 0.28 μW at a supply voltage of 1.8 V. Further, static and dynamic performance of the proposed ADC are examined by carrying out the post–layout simulations.

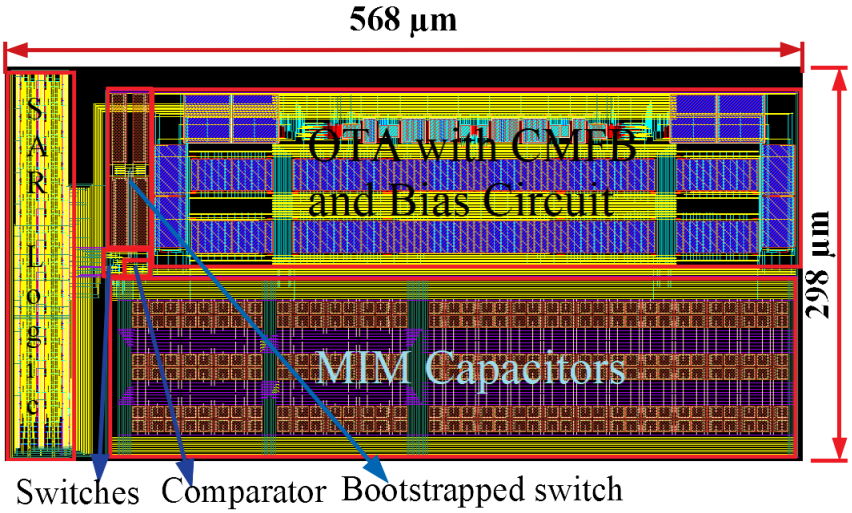


Figure 3.15: Layout of proposed 11-bit ADC.

3.4.1 Static Performance

To verify the linearity of ADC, the transfer characteristics of ADC is calculated using histogram method (Ting *et al.* 2008). The ADC is tested with a ramp signal by allowing 20 samples per code. The INL and DNL per each code is calculated and plotted in figures 3.16 and 3.17 respectively. It can be observed that, both INL and DNL are less than 1 LSB which ensures good linearity of ADC.

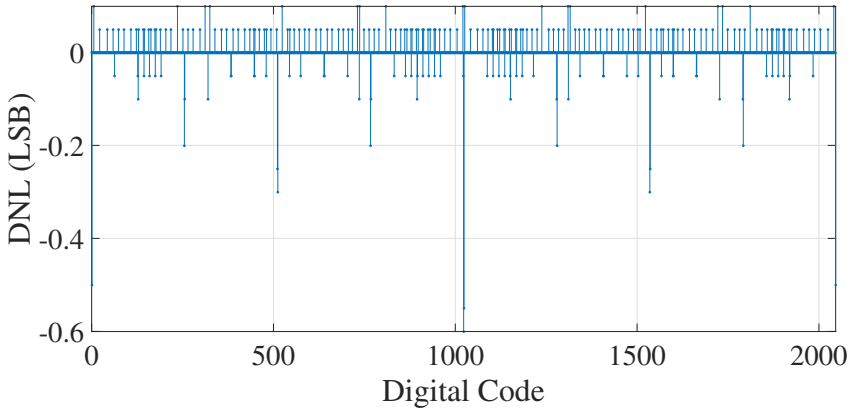


Figure 3.16: DNL plot of ADC static performance test.

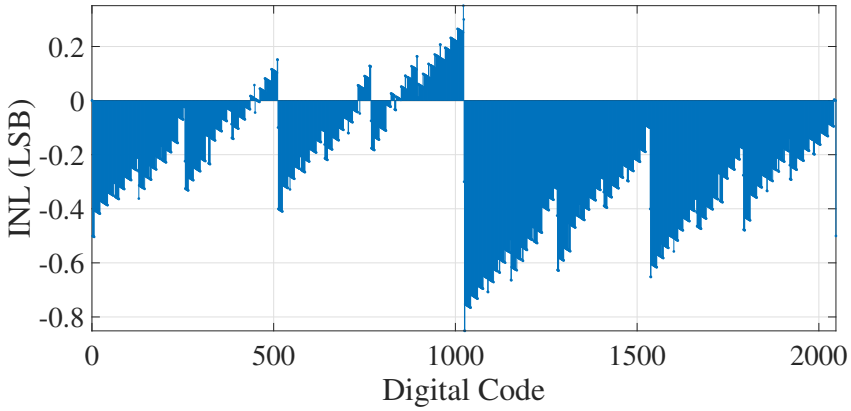


Figure 3.17: INL plot of ADC static performance test.

3.4.2 Dynamic performance

Single-tone testing with a sampling frequency of 2 kS/s is performed for the proposed ADC to evaluate its dynamic performance. FFT of the ADC output is calculated using Hann window function. Figure 3.18 shows the output spectrum of 11-bit SAR ADC for an input signal of 111 Hz. The SNDR is determined as 62.8 dB, which is equivalent to an ENoB of 10.14 bits.

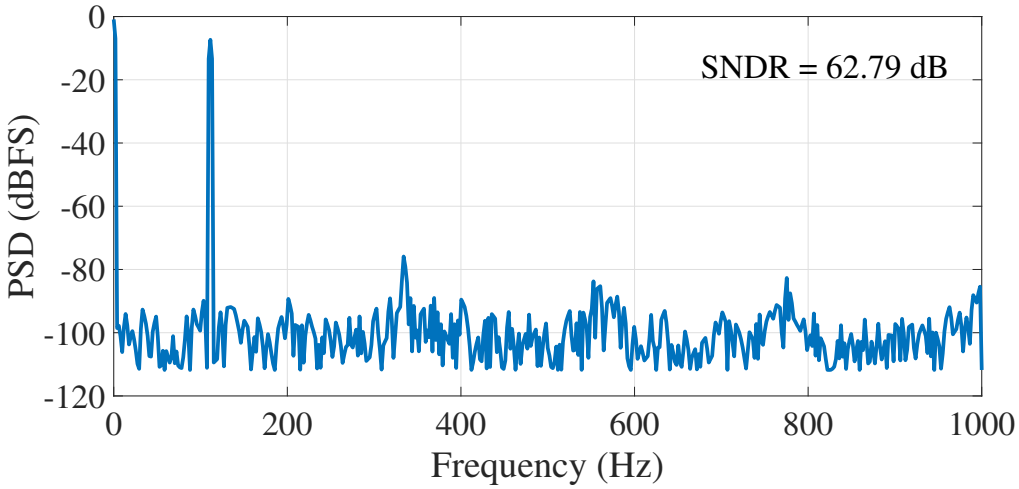


Figure 3.18: FFT spectrum of ADC output @ 111 Hz Input signal.

Figure 3.19 plots the calculated SNDR as a function of input signal amplitude with respect to full signal swing (FS) from both behavioral and post–layout simulations. Figure 3.20 shows the variation of SNDR with input signal frequency for behavioral

Table 3.2: A summary of performance and comparison.

	Das *et al.* (2014) †	Mahmoud *et al.* (2015) ⋆	Fazel *et al.* (2016) ⋆	Asghar *et al.* (2018) ††	Aminzadeh (2019) ⋆	Mekkattillam *et al.* (2019) ⋆	**This Work**⋆
Technology (nm)	180	250	180	130	180	180	180
Supply voltage (V)	1.8	1	1.2	1.2	1.2	1.8	1.8
Resolution (bits)	8	8	7	12	5	14	11
Sampling rate	40 kS/s	10 kS/s	83 MS/s	2 MS/s	20 MS/s	10 kS/s	2 kS/s
Area (mm^2)	-	1.297	0.023	0.237	0.19	6.25	0.17
INL (LSB)	-	-	+0.72/-0.83	+2.3/-2.2	+0.8/-1	+0.42/-0.38	+0.35/-0.84
DNL (LSB)	-	-	+0.44/-0.46	+1.2/-1.0	+1/-1	+0.5/-0.6	+0.1/-0.6
SNDR (dB)	46.5	40.5	37.8	62.3	30.3	84.5	62.8
SFDR (dB)	61.6	41	47.16	79	-	89.75	74.4
Power (μW)	44.7	1.87	4560	820	77	11.5	0.28
FoMW (pJ/conv-step)	13	6.85	0.433	0.19	0.144	0.14	0.12

†Schematic simulation results ⋆Post–layout results ††Fabricated results

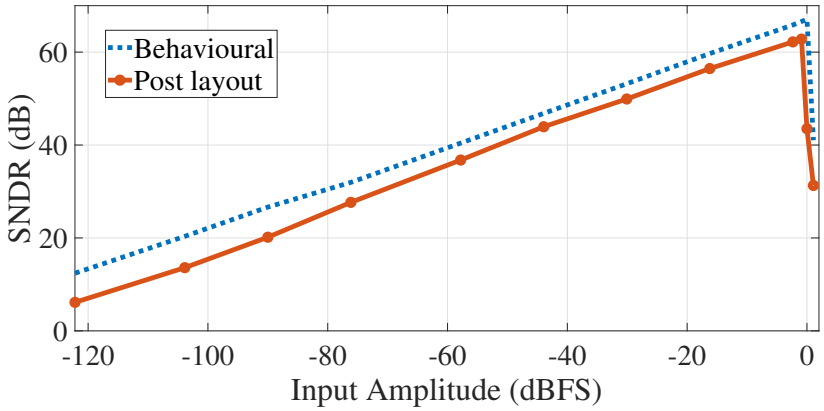


Figure 3.19: SNDR variation with input amplitude.

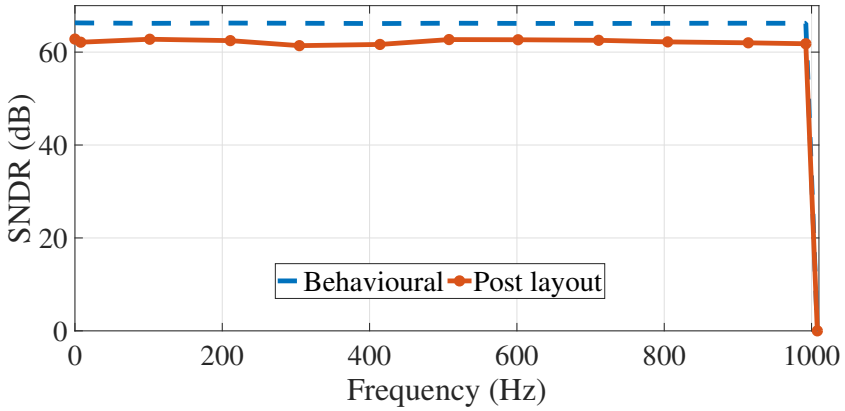


Figure 3.20: SNDR variation over an input signal bandwidth.

and post–layout simulated ADC. The SNDR is almost constant over the input signal bandwidth. The deviation in the results between the post–layout simulation and behavioral simulation can be attributed to non-idealities of practical circuit blocks such as OTA, switches and capacitors as mentioned in section 3.2. The FoMW (Walden 1999) for proposed design is calculated as 0.12 pJ/conv-step which is least among the listed references. Table 3.2 summarizes the post–layout results of proposed SAR ADC and compares with some of the recent ADCs of similar type. It is found that the proposed design is power efficient and exhibits good FoMW compared with many state-of-the-art designs found in the literature.

3.4.3 Summary

A switched capacitor based SAR ADC is proposed based on passive reference charge sharing and charge accumulation technique which uses less number of capacitors compared to conventional SAR ADC. The passive charge sharing technique is used to generate the necessary reference voltages for SAR ADC. To validate the functionality of the proposed SAR ADC design, a model has been developed in MATLAB and the behavioral simulations are carried out. Later, the non-idealities of practical amplifier and their effects on the proposed ADC are discussed. These non-idealities are incorporated into MATLAB model and their effects on the ADC characteristics are evaluated. The proposed ADC is designed using UMC 180 nm 1P6M CMOS technology for a target resolution of 11-bits. The post–layout simulations prove that the ADC achieved 10.14 bits of ENoB, FoMW of 0.12 pJ/conv-step by consuming 0.28 μW power and occupying an area of 0.17 mm^2. Also, the histogram testing shows that both INL and DNL are less than $\pm$ 1 LSB.

Chapter 4

A Fully Differential Switched Capacitor based ADC with Programmable Resolution 8-to-15-bit for Low frequency Applications

Basically, ADCs are classified as Nyquist rate and over sampled ADCs. Nyquist rate ADCs are suitable for lower data resolutions and high speed applications whereas DSMs are suitable for high resolution and lower speed applications. This idea motivates us for designing a general purpose ADC architecture for all applications. A choice to vary the resolution based on the speed and power consumption in a given application would be of great utility. Thus, a hybrid ADC with variable resolution for low frequency applications is proposed in this chapter, which uses switched capacitor integrator based architecture. The proposed ADC operates in two modes of operation, one, SAR ADC mode for lower resolution of 8-11 bits and two, DSM with multi-bit quantizer for higher resolution of 12-15 bits.

4.1 Operating principle of Proposed hybrid ADC

Figure 4.1a shows the block diagram of first order multi-bit DSM ADC which can achieve high resolutions with oversampling and noise shaping technique. The multi-bit ADC in the loop can be realized with a SAR quantizer which is shown in figure 3.1b. In the block diagram shown in figure 4.1b, there are two DACs, one operates at frequency Nf_s used for SAR operation and another is a N-bit DAC which operates at a frequency of f_s and used for noise shaping purpose. This N-bit DAC can be implemented with a discrete time integrator and 1-bit DAC as shown in figure 3.1b. Since both the paths are using the same DAC structure, they can be reduced to one path. Further, by shifting the summing point towards the comparator, the integrator block operated at frequency f_s added into both forward and feedback paths. The series connection of the integrator block and reset@f_s blocks cancel with each other in the feedback path. Therefore, the reduced block diagram of first order DSM with SAR quantizer can be redrawn as shown in figure 4.1c. Hence the only difference between SAR quantizer of figure 3.1b and the first order DSM with SAR quantizer of figure 4.1c is the reset@f_s block. Therefore it is possible to switch between SAR quantizer and first order multi-bit DSM by controlling this reset@f_s block. Further, the resolution of SAR quantizer is programmable by controlling N value and the DSM resolution is controlled with a OSR.

Figure 4.2 shows circuit level implementation of the proposed 8-15 bit programmable resolution hybrid ADC which is controlled by a 3-bit input bus $res[2:0]$. The discrete time integrator is implemented with a switched capacitor integrator with fully differential OTA, capacitors C_1, C_2, C_5, C_6 and switches $S_{3:8}$. The reset@f_s block is implemented with two switches S_1 and S_2. The feedback 1-bit DAC is implemented using capacitors C_1, C_2, C_3, C_4 and switches $S_{11:16}$. Figure 4.3 shows the timing waveform of proposed hybrid ADC in first order DSM with SAR quantizer mode. When sampling clock is high, the voltage nodes v_1 and v_2 are connected to the differential input signals V_{ip} and V_{im} through the switches S_9 and S_{10}. The capacitors C_1 and C_2 sample the input signal. This charge transferred to the capacitors C_5 and C_6 when clock is low, develops voltages V_{op} and V_{om}. The comparison clock goes high at the start of next clock cycle, thus, the comparator compares V_{op} and V_{om} and gives digital output. Once the comparison clock goes low, the capacitors C_3, C_4 connect to capacitors C_1, C_2 based on the comparator output and share the charge until the clock is

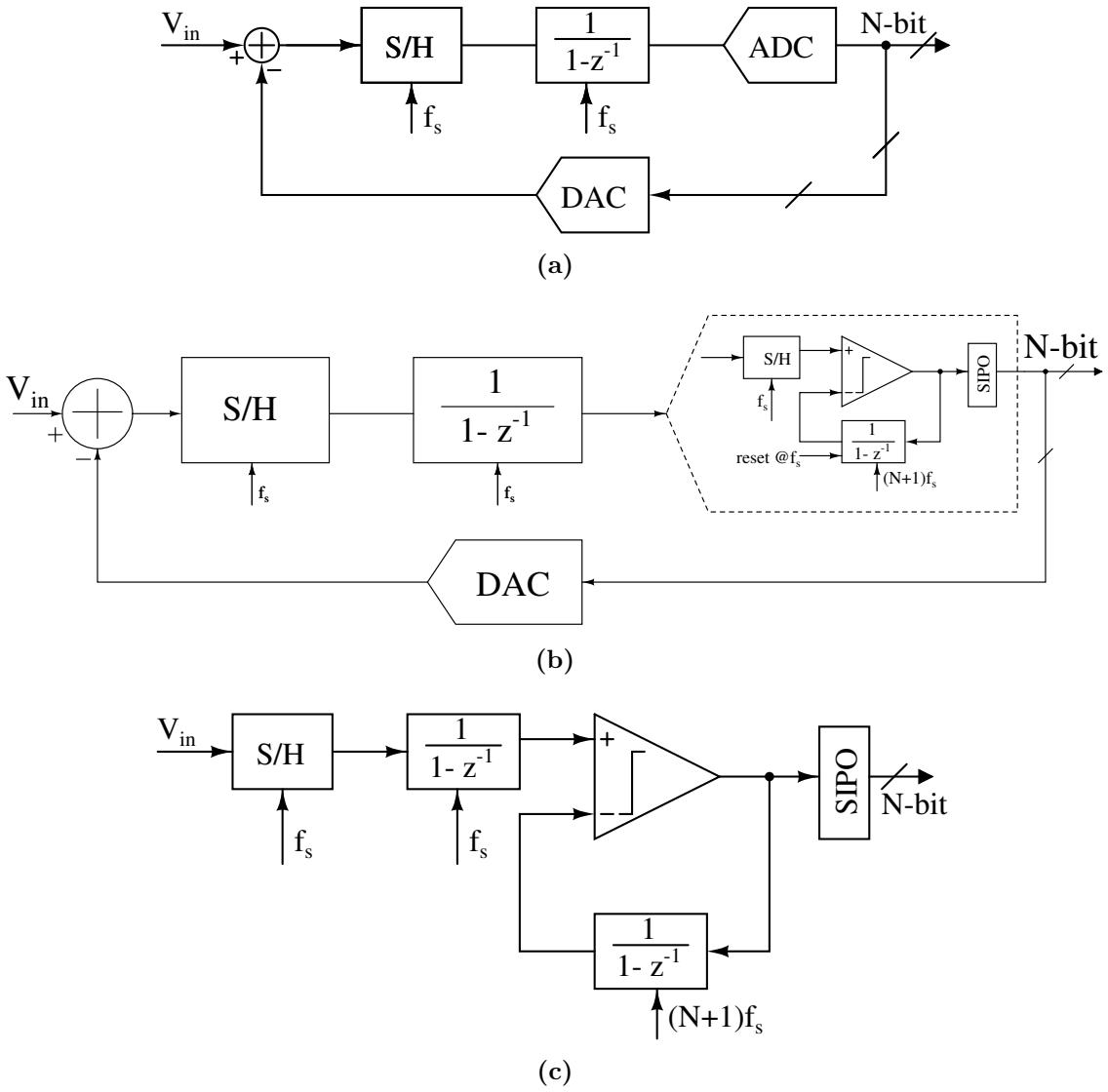


Figure 4.1: (a) First order multi-bit DSM block diagram, (b) First order DSM with SAR quantizer, (c) Reduced block of first order DSM with SAR qauntizer.

high. When clock goes low, the capacitors C_1, C_2 disconnect from C_3, C_4 and connect to C_5, C_6. The charge transfer takes place and the voltages V_{op}, V_{om} are developed. This conversion procedure is depicted with a flow chart as shown in figure 4.4. The proposed hybrid ADC configured as a switched-capacitor integrator based SAR ADC from 8-bit to 11-bit resolution and a first-order multi-bit DSM from 12-bit to 15-bit resolution. The control bus $res[2:0]$ is used to select the resolution of ADC. The

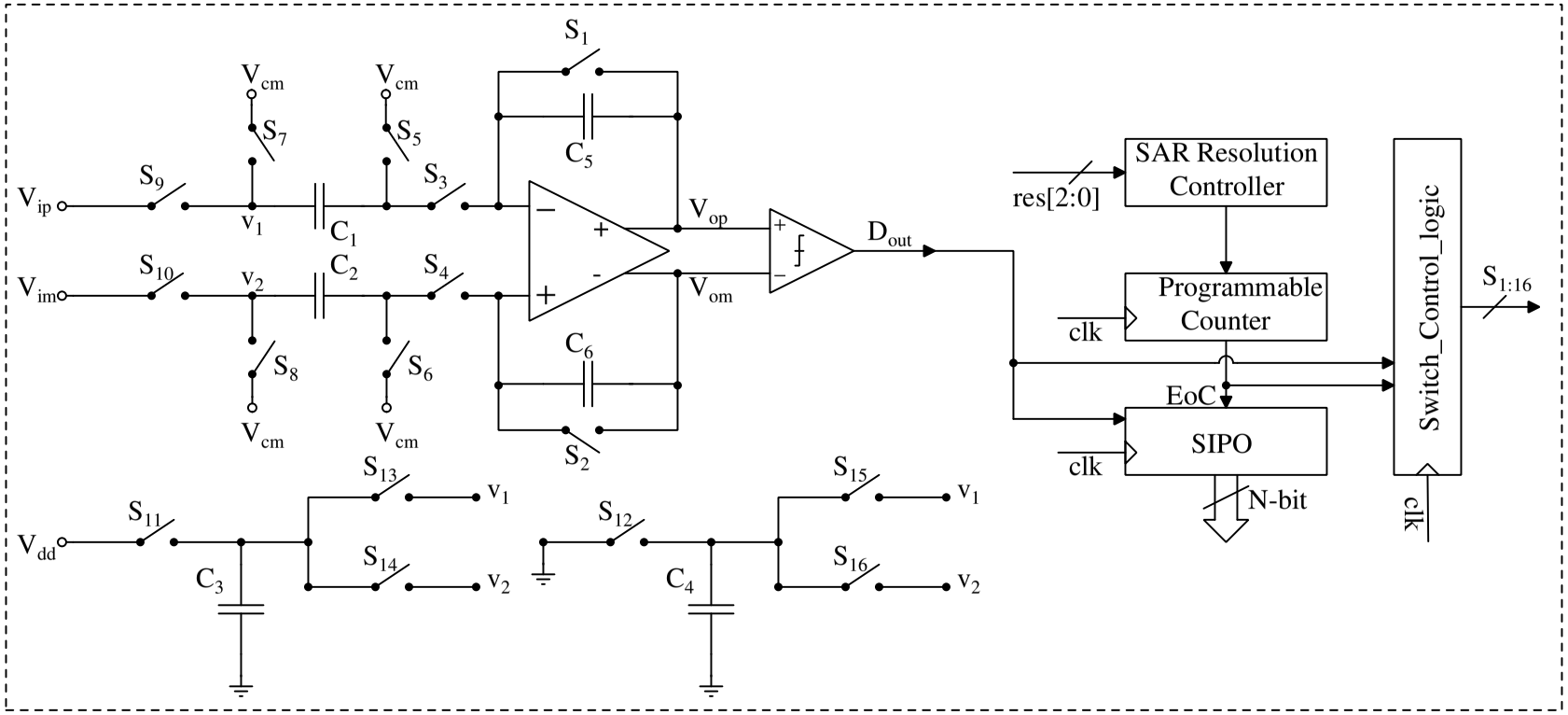


Figure 4.2: Circuit diagram of the proposed programmable resolution ADC architecture.

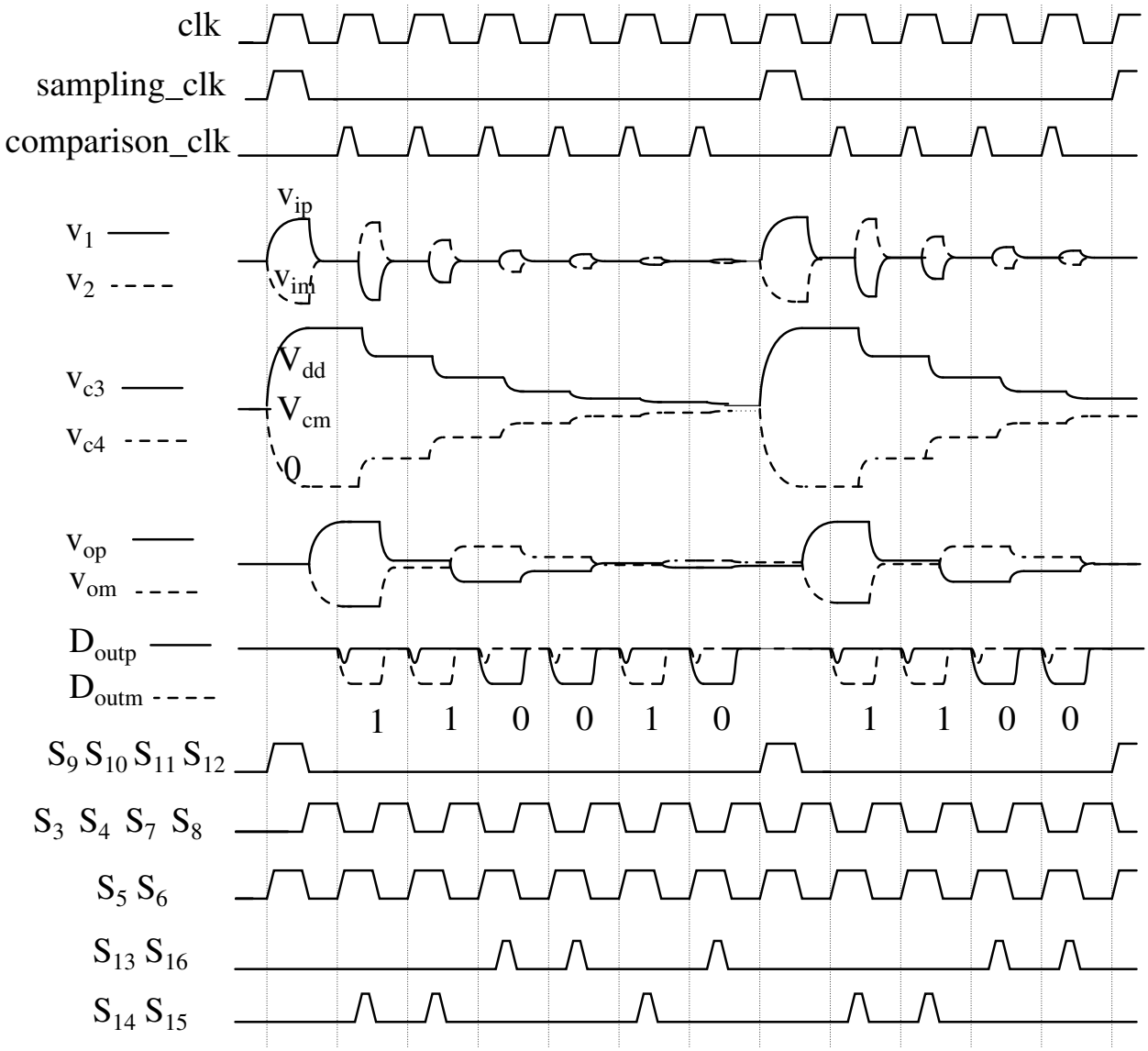


Figure 4.3: Timing diagram of the proposed programmable resolution ADC architecture.

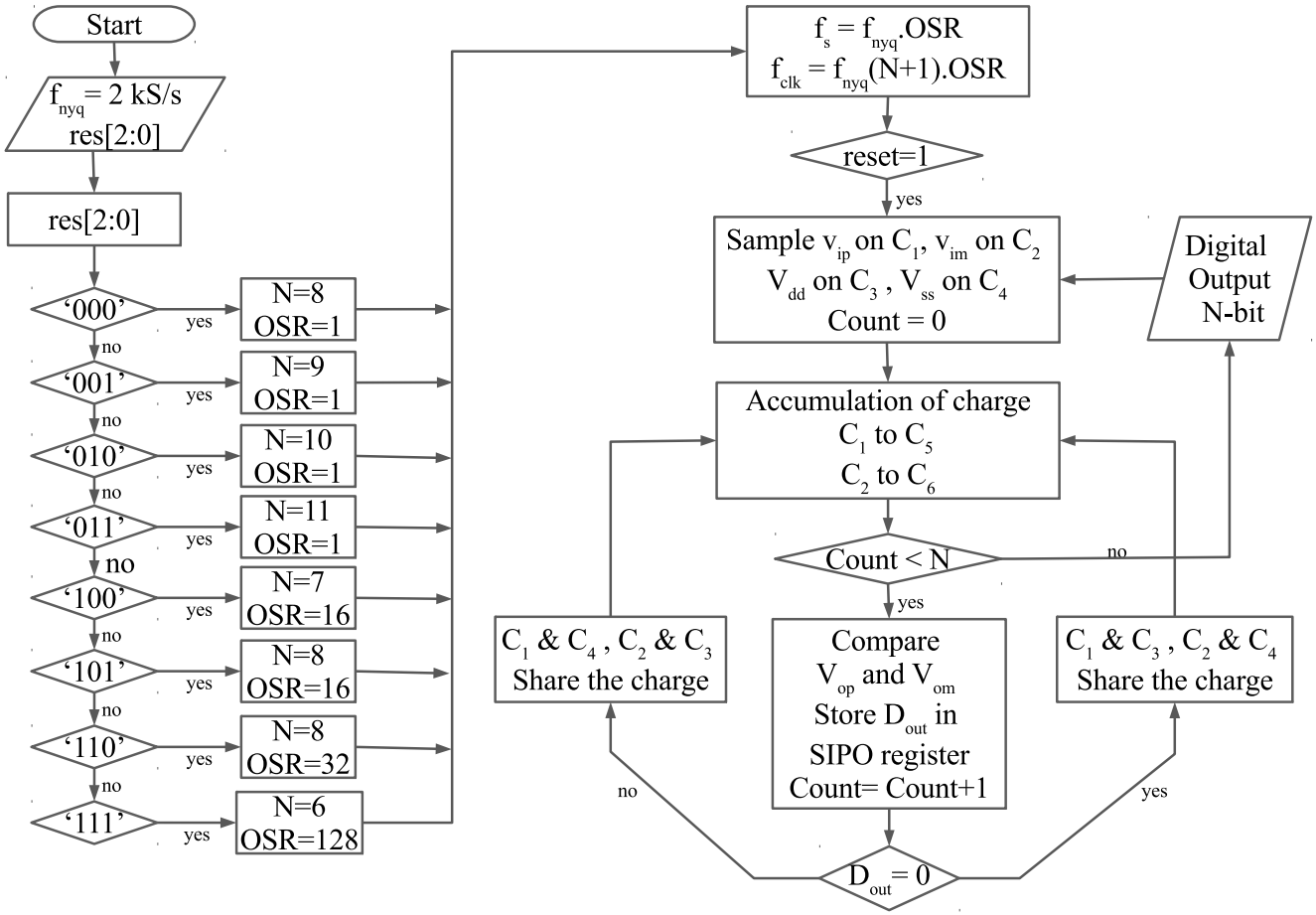


Figure 4.4: Flow chart of programmable resolution ADC.

SNR for the first order DSM with multi-bit quantizer is given by equation (4.1).

$$SNR_{dB} \;=\; 6.02N \;+\; 1.76 \;+ 30\log_{10}(OSR) - 10\log_{10}\left(\frac{\pi^2}{3}\right) \tag{4.1}$$

The resolution (N) for multi-bit DSM and oversampling ratio (OSR) are chosen to target corresponding SNR for each resolution from 12-bit to 15-bit. For example, $res[2:0]$='100' configures the proposed ADC as the first order DSM with 7-bit SAR quantizer and an OSR of 16 which targets 75 dB SNR. The sampling and clock frequency, targeted SNR, SAR quantizer resolution and OSR for all modes are calculated according to the resolution mode chosen by $res[2:0]$.

The conversion process starts when *reset* is 'high'. The total conversion can be divided into four phases as follows.

Sampling Phase In this phase, switches S_5, S_6, S_9, S_{10}, S_{11} and S_{12} are 'ON'. Capacitors C_1 and C_2 sample the differential input signals V_{ip} and V_{im} through S_9, S_5 and S_{10}, S_6 switches respectively. Also, capacitor C_3 samples the supply voltage V_{dd} through switch S_{11} and capacitor C_4 discharges to ground through switch S_{12}. In 8-11 bit resolution modes, switches S_1 and S_2 are 'ON' thereby resetting the capacitors C_5 and C_6. This phase exists for a positive half cycle of the clock after the EoC. Further, to avoid the distortion due to charge injection, bootstrapped switches with bottom plate sampling are used.

Charge Accumulation Phase This phase comes up during every negative half of clock cycle. In this phase, S_3, S_4, S_7, S_8 switches are 'ON' and the remaining switches are 'OFF'. Therefore, the capacitors C_1, C_2 are connected between V_{cm} and virtual short node. This forces the charge on capacitors C_1 and C_2 to transfer and accumulate on capacitors C_5 and C_6 respectively.

Comparison Phase This phase exists for a small interval which starts at the positive edge if EoC is low. In this phase, the differential outputs of OTA are compared and the decision bit is stored in SIPO register.

Passive Charge Sharing Phase This phase starts after the comparison phase in positive half cycle, in which the capacitors C_1, C_2, C_3, C_4 involve in passive charge

sharing through switches S_5, S_6, S_{13}, S_{14},S_{15},S_{16} based upon the comparator output. As shown in figure 4.4, if the comparator output is high, capacitors C_1, C_4 and C_2, C_3 share the charge otherwise capacitors C_1, C_3 and C_2, C_4 share the charge, respectively. This allows to decide the comparison level for next cycle.

The conversion starts with sampling phase and then followed by accumulation, comparison and passive charge sharing phases for N cycles. At the end of conversion, the capacitors C_5 and C_6 are discharged by closing switches S_1 and S_2, when the proposed ADC is configured in SAR mode. In first order DSM mode, at the end of conversion of SAR quantizer, the capacitors C_5 and C_6 are left with the quantization error. Hence, the integration property allows noise shaping with OSR. This characteristic allowed to obtain high resolutions.

4.1.1 Modeling in MATLAB

To verify the functionality of the proposed programmable resolution ADC design, a model has been designed in MATLAB. The behavioral simulations are carried out for various resolutions. The architecture operates in SAR mode for 8-bit to 11-bit and multi-bit quantizer DSM mode for 12-bit to 15-bit. Here, the integrator based SAR ADC acts as a multi- bit quantizer.

Figure 4.5 shows the output spectrum for resolutions from 8-bit to 11-bit with a full scale sine wave input signal of frequency 117 Hz. The sampling frequency (f_s) is 2 kHz. Similarly, figure 4.6 shows the output spectrum for resolutions from 12-bit to 15-bit. In this range of resolution, the ADC is implemented using first order DSM with multi- bit quantizer. These figures clearly show a noise-shaped characteristics and the 20 dB/decade slope of the noise is consistent with first-order noise shaping. Table 4.1 lists the parameters such as target resolution, SAR ADC resolution, OSR, SNR, THD, SNDR and ENoB achieved by the programmable resolution ADC.

4.2 Distortion analysis

The ADC characteristics deviate from ideal due to non-idealities of OTA, capacitors' mismatch and switches. This non-linearity reflects as a distortion in the output and degrades the ENoB. The estimation of distortion shows the effect of each sub circuit and the specifications needed to achieve the required resolution.

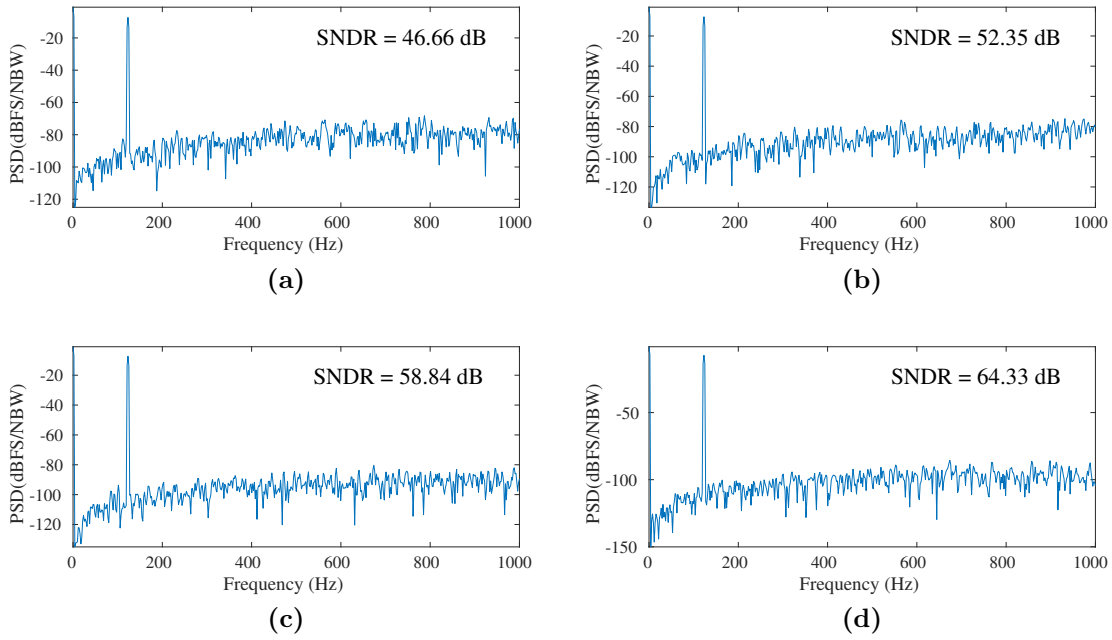


Figure 4.5: Ideal PADC output spectrum (a) 8- bit, (b) 9- bit, (c)10- bit, (d) 11- bit SAR ADC.

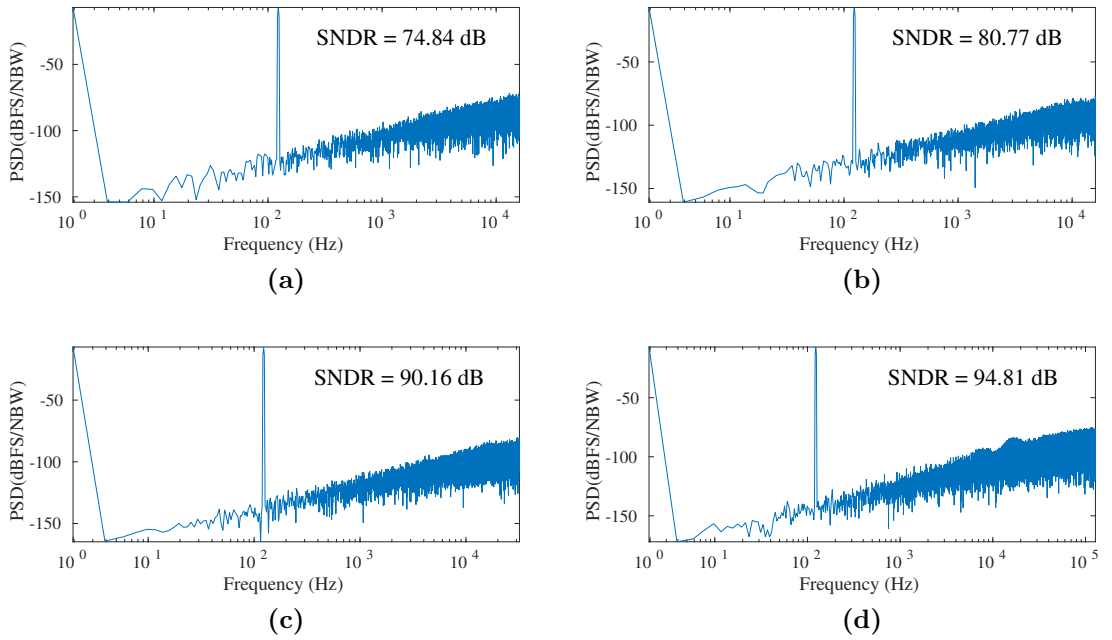


Figure 4.6: Ideal PADC output spectrum (a) 12- bit, (b) 13- bit, (c)14- bit, (d) 15- bit.

Table 4.1: Ideal PADC performance.

Target resolution	SAR quantizer resolution	OSR	SNR (dB)	THD (dB)	SNDR (dB)	ENoB
8	8	1	46.89	-59.47	46.66	7.46
9	9	1	52.62	-64.6	52.35	8.4
10	10	1	59.1	-71.38	58.84	9.48
11	11	1	64.67	-75.55	64.33	10.4
12	7	16	75.04	-88.3	74.84	12.14
13	8	16	81	-93.35	80.77	13.1
14	8	32	90.4	-102.7	90.16	14.7
15	6	128	95.3	-104.45	94.8	15.46

4.2.1 Capacitor Mismatch

The accuracy of SAR ADC depends on the matching of feedback capacitors. The physical design and manufacturing process control the variation of mismatch between capacitors. This kind of mismatch can not be removed entirely but this can be viewed as a random statistical process and the variation in system characteristics can be estimated (Chang 2013). In fully differential circuits and charge sharing circuits, the relative values of capacitors are more important than absolute values. Therefore, the deviation or mismatch between the components is calculated as the normalized deviation from their mean value.

It is assumed that the capacitors C_1-C_4 are matched well and α_1, α_2, α_3 and α_4 are the normalized deviations of capacitors C_1-C_4 from their mean value, respectively.

$$\begin{aligned} \alpha_i &= \frac{\Delta C_i}{C_m 1} = \frac{C_i - C_{m1}}{C_{m1}} \\ C_{m1} &= \frac{C_1 + C_2 + C_3 + C_4}{4} \\ \sum_{i=1}^{4} \alpha_i &= \alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 \\ &= \frac{C_1 + C_2 + C_3 + C_4 - 4C_{m1}}{C_{m1}} = 0 \end{aligned} \tag{4.2}$$

Similarly, α_5 and α_6 are the normal deviations of C_5 and C_6 respectively.

$$
\begin{aligned}
C_{m2} &= \frac{C_5 + C_6}{2} \\
\alpha_5 &= \frac{C_5 - C_{m2}}{C_{m2}} \\
\alpha_6 &= \frac{C_6 - C_{m2}}{C_{m2}} \\
\therefore \quad \alpha_5 + \alpha_6 &= \frac{C_5 + C_6 - 2C_{m2}}{C_{m2}} = 0
\end{aligned}
$$

Therefore, from a statistical point of view, it can be assumed that the sum of normalized deviations is zero. Accordingly,

$$\sum_{i=1}^{4} \alpha_i = \alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 = 0 \tag{4.3}$$

$$\alpha_5 + \alpha_6 = 0 \tag{4.4}$$

The charge sharing between capacitors C_1-C_4 determines the voltage reference levels whereas capacitors C_5 and C_6 are involved in accumulation and comparison. Therefore, the group of capacitors C_1-C_4 and C_5-C_6 need to be matched well. The mismatch between them induces an error voltage in each comparison and causes non-linearity in ADC transfer characteristics. In SAR ADC operation mode, the deviation of reference voltages in each cycle due to the capacitors' mismatch is derived and tabulated in table 4.2. The INL_{max} can be derived as shown in equation (4.5) and it occurs when the comparator output is '1' in all cycles. The standard deviation (σ) of this INL_{max} relates to the standard deviation of capacitor ($\sigma_{\Delta C}$) as shown in equation (4.6).

$$
\begin{aligned}
|\text{INL}|_{max} &= (\alpha_1 + \alpha_2)\, 2^{N-2} \sum_{k=1}^{N-1} \frac{k}{2^k} \\
&= (\alpha_1 + \alpha_2)\, 2^{N-2} \left(2 - \frac{N+1}{2^{N-1}}\right) \\
&= (\alpha_1 + \alpha_2) \left(2^{N-1} - \frac{N+1}{2}\right) \qquad (4.5) \\
\sigma_{|INL|_{max}} &= \left(2^N - N - 1\right) \frac{\sigma_{\Delta C}}{\sqrt{2}C} \qquad (4.6)
\end{aligned}
$$

Table 4.2: SAR ADC voltage reference levels due to capacitors' mismatch.

Cycle	Voltage reference level	Error in voltage reference level (V_e)
1	0	0
2	$(-1)^{\overline{b_{N-1}}}\left(1-\frac{\alpha_1+\alpha_2}{2}\right)\frac{V_{dd}}{2^2}$	$(-1)^{b_{N-1}}(\alpha_1+\alpha_2)\frac{V_{dd}}{2^3}$
3	$(-1)^{\overline{b_{N-1}}}\left(1-\frac{\alpha_1+\alpha_2}{2}\right)\frac{V_{dd}}{2^2}+(-1)^{\overline{b_{N-2}}}\left(1-\frac{2(\alpha_1+\alpha_2)}{2}\right)\frac{V_{dd}}{2^3}$	$(-1)^{b_{N-1}}(\alpha_1+\alpha_2)\frac{V_{dd}}{2^3}+2(-1)^{b_{N-2}}(\alpha_1+\alpha_2)\frac{V_{dd}}{2^4}$
4	$(-1)^{\overline{b_{N-1}}}\left(1-\frac{\alpha_1+\alpha_2}{2}\right)\frac{V_{dd}}{2^2}+(-1)^{\overline{b_{N-2}}}\left(1-\frac{2(\alpha_1+\alpha_2)}{2}\right)\frac{V_{dd}}{2^3}$ $+(-1)^{\overline{b_{N-3}}}\left(1-\frac{3(\alpha_1+\alpha_2)}{2}\right)\frac{V_{dd}}{2^4}$	$(-1)^{b_{N-1}}(\alpha_1+\alpha_2)\frac{V_{dd}}{2^3}+2(-1)^{b_{N-2}}(\alpha_1+\alpha_2)\frac{V_{dd}}{2^4}$ $+3(-1)^{b_{N-3}}(\alpha_1+\alpha_2)\frac{V_{dd}}{2^5}$
.	.	.
.	.	.
.	.	.
N	$\sum_{k=1}^{N-1}(-1)^{\overline{b_{N-k}}}\left(1-\frac{k(\alpha_1+\alpha_2)}{2}\right)\frac{V_{dd}}{2^{(k+1)}}$	$\sum_{k=1}^{N-1}k(-1)^{b_{N-k}}(\alpha_1+\alpha_2)\frac{V_{dd}}{2^{(k+2)}}$

4.2.2 OTA non-idealities

In section 4.1, operation of the proposed ADC is demonstrated by assuming infinite gain, bandwidth for OTA and also instant charge transfer between capacitors. In reality, due to the finite gain of OTA, during charge sharing, some charge will be left behind in capacitors C_1 and C_2, which is known as static error voltage. Similarly, the finite UGB and slew rate of amplifier causes settling time error, which is known as dynamic error. These errors depend on the input signal, which causes harmonics at the output.

4.2.2.1 Finite gain of OTA

The switched-capacitor integrator transfer function is derived as follows (Pavan *et al.* 2017) by analyzing the finite gain effect of OTA. During sampling phase (ϕ_1), C_1 charges to the input voltage ($v_{ip}[n]$), while C_5 holds the charge ($q_5[n-1]$) held in previous cycle. Due to finite gain (A) of OTA, the voltage on the left side of C_5 is $-v_{op}[n-1]/A$. Thus, the charge on C_5 ($q_5[n-1]$) can be written as

$$q_5[n-1] = C_5\left(1+\frac{1}{A}\right)v_{op}[n-1] \tag{4.7}$$

In charge integration phase, it is assumed that, the charge q flows out from C_1 to C_5 and the charge on C_1 becomes

$$q_1[n] - q = C_1\left(\frac{v_{op}[n]}{A}\right) \tag{4.8}$$

From equation (4.8), the transferred charge q can be written as

$$q = q_1[n] - C_1\left(\frac{v_{op}[n]}{A}\right) \tag{4.9}$$

After, charge (q) transfer takes place, the charge on capacitor C_5 becomes

$$\begin{aligned} q_5[n] &= q_5[n-1] + q \\ q_5[n] &= q_5[n-1] + q_1[n] - C_1\left(\frac{v_{op}[n]}{A}\right) \\ v_{op}[n] &= \frac{q_5[n-1] + q_1[n]}{C_5\left(1 + \frac{1}{A} + \frac{C_1}{C_5 A}\right)} \qquad (4.10) \\ v_{om}[n] &= \frac{q_6[n-1] + q_2[n]}{C_6\left(1 + \frac{1}{A} + \frac{C_2}{C_6 A}\right)} \qquad (4.11) \end{aligned}$$

Voltage reference levels deviate from the ideal voltage references because of this repetitive gain error which results in non-linearity in ADC transfer characteristics. Equation (4.12) shows the voltage reference error due to the finite gain of OTA in n^{th} cycle of SAR ADC operation.

$$V_e = -\frac{C_1 V_{dd}}{C_5 A}\sum_{k=1}^{N-1}(-1)^{b_{N-k}}\frac{k}{2^{(k+1)}} \qquad (4.12)$$

The maximum integrated non-linearity can be calculated as

$$|\text{INL}|_{max} = \frac{C_1}{C_5 A}\left(2^N - N - 1\right) \qquad (4.13)$$

From equation (4.13), the OTA gain needs to satisfy the following relation to achieve INL less than 0.5 LSB.

$$A > \frac{C_1}{C_5}\left(2^{N+1} - 2N - 2\right) \qquad (4.14)$$

In DSM operation, the variation in integrator transfer function alters the STF and NTF. By substituting equation (4.7) and $q_1[n] = C_1 v_{ip}[n]$ in equation (4.10) and applying z transform results in

$$V_{op}(z) = \frac{C_1/C_5}{\left(1 + \frac{1}{A}\right)(1+\epsilon)}\frac{V_{ip}(z)}{\left(1 - \frac{z^{-1}}{1+\epsilon}\right)} \qquad (4.15)$$

Similarly,

$$V_{om}(z) = \frac{C_2/C_6}{\left(1+\frac{1}{A}\right)(1+\epsilon)} \frac{V_{im}(z)}{\left(1-\frac{z^{-1}}{1+\epsilon}\right)} \tag{4.16}$$

where

$$\epsilon = \frac{C_1}{C_5(A+1)} = \frac{C_2}{C_6(A+1)} \tag{4.17}$$

Since, $C_1 = C_2$ and $C_5 = C_6$, the loop filter transfer function of DSM can be written as

$$L(z) = \frac{V_{op}(z) - V_{om}(z)}{V_{ip}(z) - V_{im}(z)} = \frac{g.p}{1 - pz^{-1}} \tag{4.18}$$

where $g = \frac{C_1}{C_5}\frac{A}{A+1}$ and $p = \frac{1}{1+\epsilon}$ are integrator gain and pole respectively.

Therefore, the STF and NTF become

$$STF(z) = \frac{L(z)}{1+L(z)} = \frac{g.p}{1 - p(1-g)z^{-1}} \tag{4.19}$$

$$NTF(z) = \frac{1}{1+L(z)} = \frac{1 - pz^{-1}}{1 - p(1-g)z^{-1}} \tag{4.20}$$

From equation (4.18), it can be observed that the finite amplifier gain has two effects: a small reduction in the integrator's gain constant and an inward shift of the integrator's pole (z-1). The change in integrator's gain constant is equivalent to a coefficient error (ϵ) and also causes the extra poles of both STF and NTF move away from the origin. Thus, this change in integrator gain has a negligible impact on the in-band SNR degradation. In contrast to this, the second effect, the shift in pole location of loop filter is more problematic because the loop filter pole becomes an NTF zero. This movement of an NTF zero affects the attenuation of noise in pass band.

This phenomenon is modelled in MATLAB for an integrator gain (C_1/C_5) of 0.3. The pole-zero movement in STF and NTF with OTA gain (A) is observed and plotted in figure 4.7. One can observe that the pole of STF is moving away from z =0.7 as OTA gain (A) decreases and zero stays at the origin. This results in the gain reduction in the signal path, as shown in frequency response of STF in figure 4.8a. In the pole-

zero plot of NTF, shown in figure 4.7b, as OTA gain (A) decreases, the NTF zero moves from z =1 towards z=0 and pole moves away from z =0.7 which is similar to STF pole movement. The movement of NTF zero causes reduction of attenuation as can be observed in figure 4.8b. From all of the discussions above, it can be concluded that the finite dc gain of OTA is one of the limiting factors for modulator to achieve maximum SNR.

Further, a low-order modulator is susceptible to the non-linear phenomenon of dead bands. A dead band is a range of inputs that yields the same periodic output sequence and hence the same post-decimation output. Therefore, in dead band, a dc input with a small magnitude appears as a zero input. The reason behind this is the shift in NTF's zero from z=1 to z=p, which limits the NTF's dc gain to $(1-p)/(1-p+gp) = 1/(1+A)$ instead of zero. Thus, the modulator loses its ability to achieve infinite precision with dc signals. To register small dc input values (u), the following expression (Pavan *et al.* 2017) should satisfy

$$A > \frac{1}{2|u|} \tag{4.21}$$

It is assumed that the OTA gain is constant over output swing in all the above

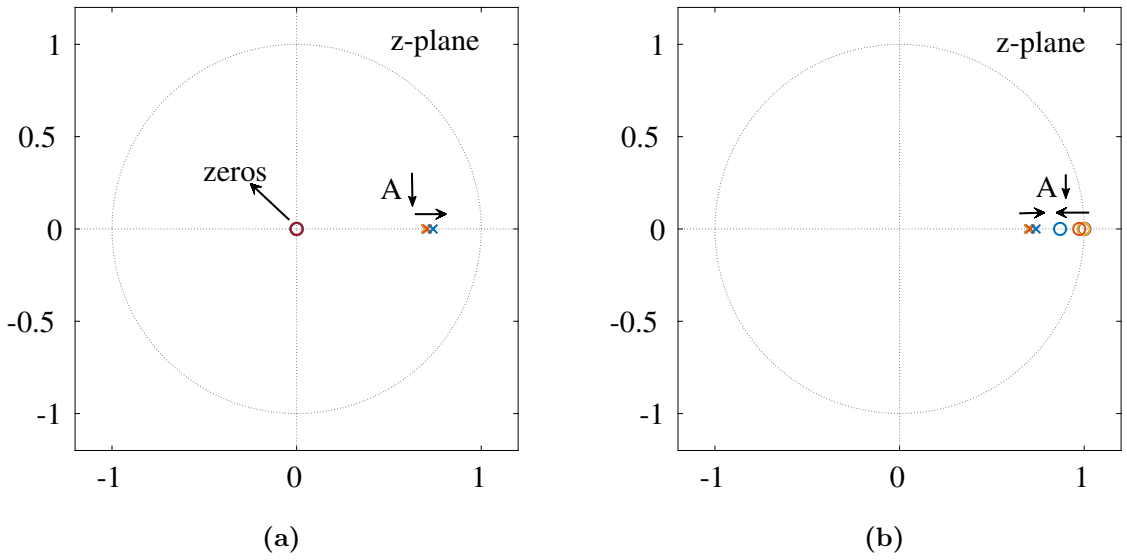


Figure 4.7: Pole-Zero mapping (a) STF, (b) NTF for different OTA gains.

discussions. In practice, OTA gain is a function of input voltage, which causes harmonic distortion. Since the magnitude of the associated input-referred error signal is no more than v_{outmax}/A, The maximum output of OTA (v_{outmax}) is $(C_1/C_5)\cdot v_{inmax}$. Therefore, upper limit on the distortion of the signal is

$$THD = \frac{C_1}{C_5}\frac{1}{A} \tag{4.22}$$

Even if there is no explicit distortion limit for the ADC, it is needed to ensure that the loop filter is sufficiently linear so that the distorted out-of-band quantization

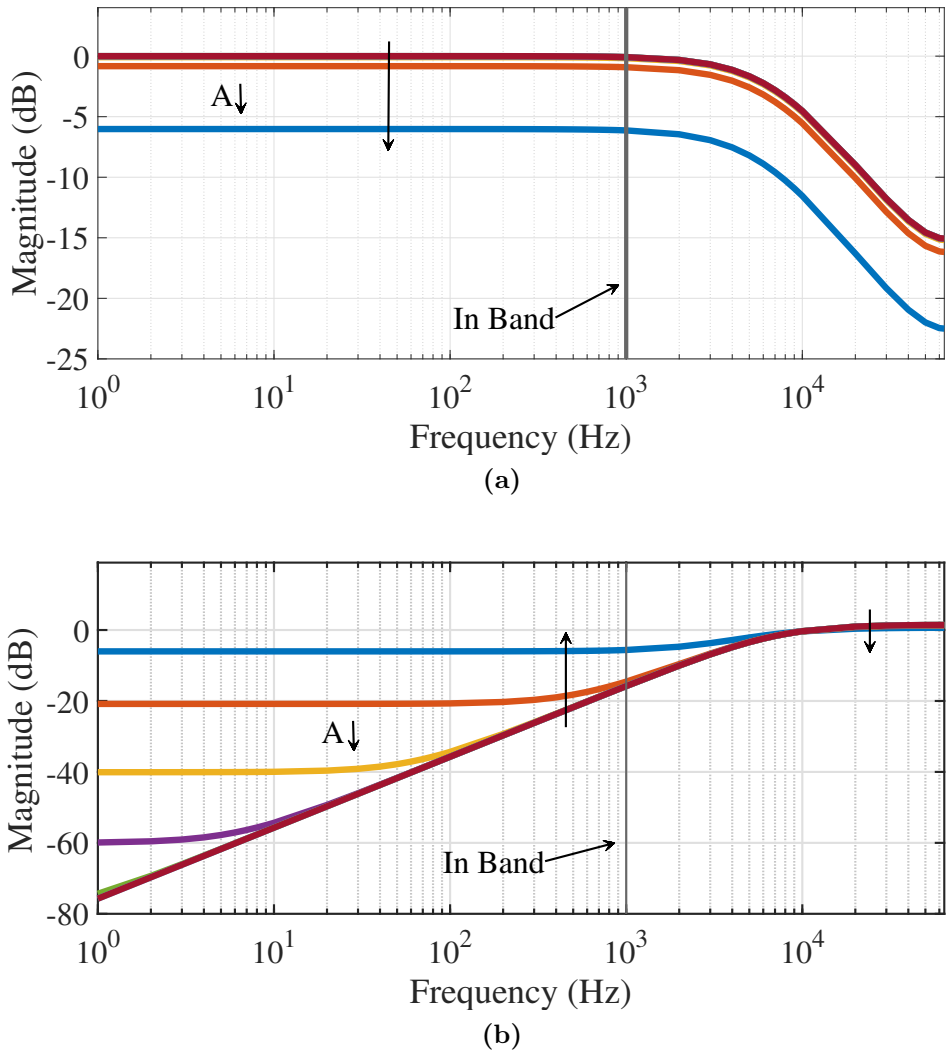
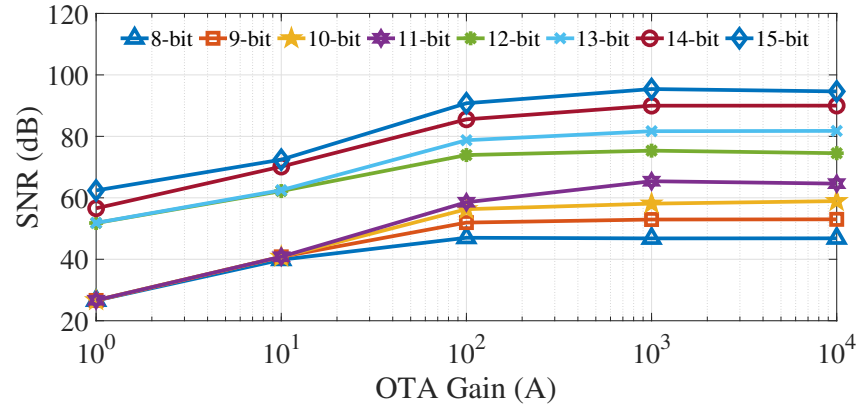
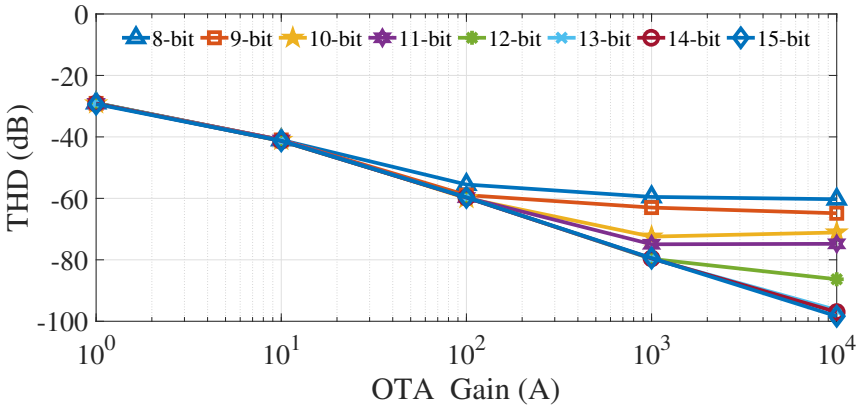


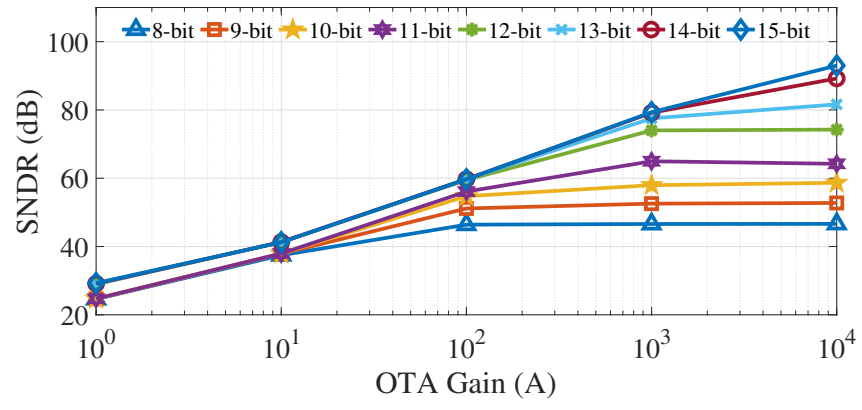
Figure 4.8: Bode plot (a) STF, (b) NTF for different OTA gains.



(a)



(b)



(c)

Figure 4.9: ADC characteristics vs. Gain (a) SNR, (b) THD, (c) SNDR.

noise does not fall in the noise notch. Based on these considerations, the amplifier is designed for a particular gain, followed by modulator simulations to verify that the amplifier's linearity is adequate.

Further, the programmable resolution ADC with finite OTA gain is modelled in MATLAB. The ADC is simulated with a sinusoidal signal of frequency 123 Hz for resolutions from 8-15 bit. As the OTA gain is varied from 0 dB to 80 dB, SNR, THD and SNDR are observed as shown in figure 4.9. It can be seen that, the SNR improves with the OTA gain. It is observed that, the gain around 80 dB ensures the THD below -90 dBc, which is needed in case of 15- bit resolution. From this result it is concluded that, OTA with 80 dB gain serves our purpose of designing an ADC that is programmable from 8-bit to 15-bit.

4.3 Realization of Programmable resolution ADC

The ADC works as SAR ADC for 8-11 bit resolution and a multi-bit quantizer DSM for 12-15 bits. Here, the SAR ADC works as a multi-bit quantizer. The proposed programmable resolution ADC is built with OTA, comparator, digital control logic, bootstrapped switch, capacitors and switches. This section discusses the design of each of these blocks. The total input referred noise power for a switched-capacitor integrator (Schreier *et al.* 2005) is given by equation (4.23).

$$\overline{v_{n,diff}^2} \approx 4 \cdot \frac{2kT}{C_1} \tag{4.23}$$

By considering the in-band mean-square noise, the value of capacitor C_1 is calculated and tabulated as shown in table 4.3 using equation (4.24) for a required SNR. Therefore, the capacitor C_1 is determined as 1 pF subject to the noise for 15- bit resolution. The value of capacitor C_5 is determined as 3.3 pF from the integrator gain which is 0.3.

$$C_1 \geq \frac{64kT}{V_{dd}^2\, OSR} 10^{SNR/10} \tag{4.24}$$

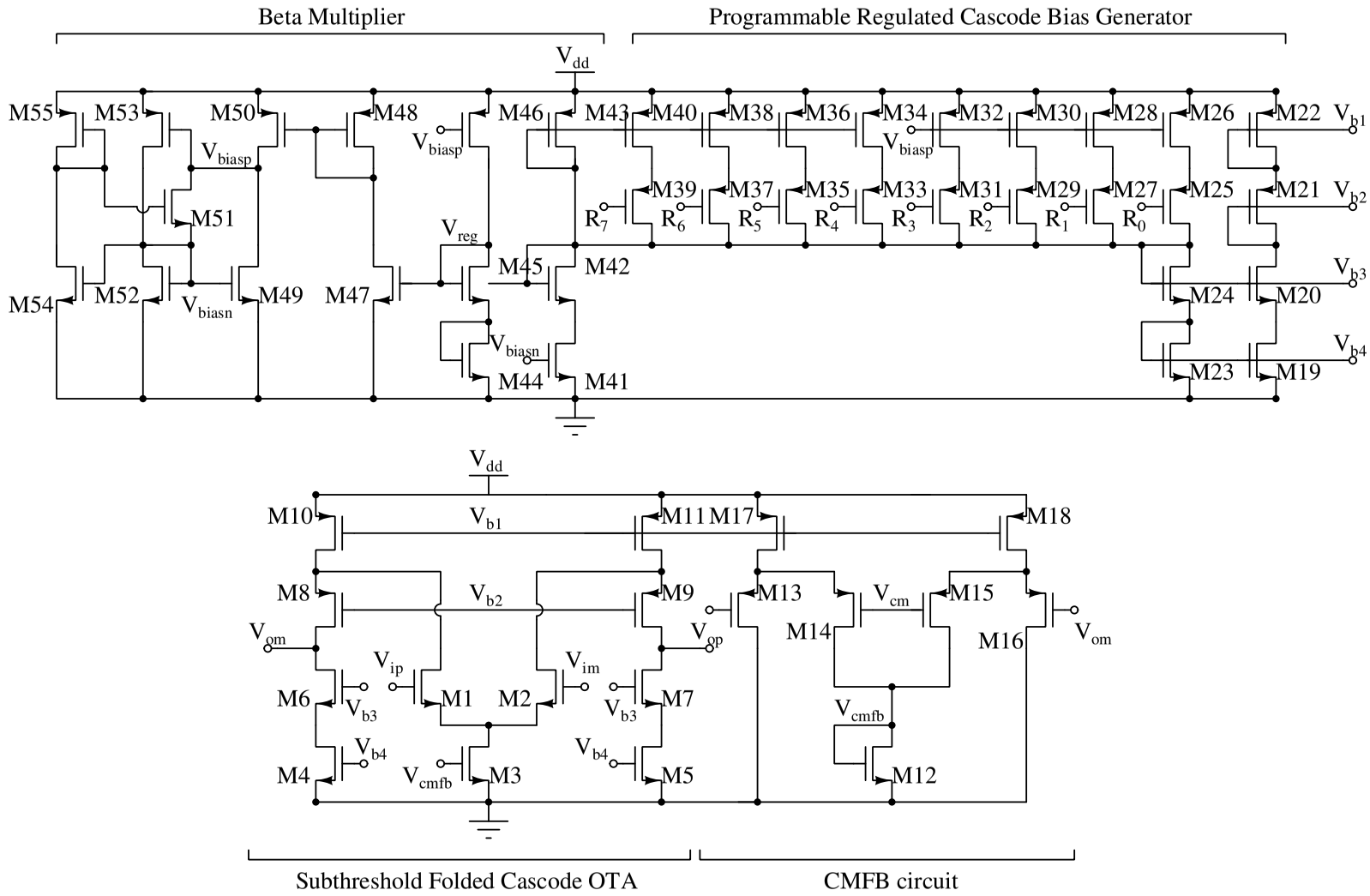


Figure 4.10: FC OTA with programmable bias circuit.

Table 4.3: The capacitor size C_1, slew rate and UGB requirements of OTA for all resolutions.

Target resolution	OSR	SNR (dB)	$\overline{v_{n,diff}^2}$	$C_1(fF) \geq$	SAR	f_{clk} (kHz)	Slew rate $(V/\mu s)$	UGB (MHz)	$I_b\,(\mu A)$
8	1	50	4.05 $(\mu V)^2$	8.2	8	18	0.08	0.43	0.1
9	1	56	1.02 $(\mu V)^2$	32.6	9	20	0.09	0.47	0.12
10	1	62	0.26 $(\mu V)^2$	129.7	10	22	0.1	0.51	0.14
11	1	68	64.2 $(nV)^2$	516.2	11	24	0.11	0.55	0.15
12	16	75	12.8 $(nV)^2$	161.8	7	256	1.2	4.9	1.5
13	16	81	3.2 $(nV)^2$	643.8	8	288	1.3	5.4	1.8
14	32	86	1.02 $(nV)^2$	1018	8	576	2.7	10	4
15	128	92	0.26 $(nV)^2$	1013	6	1792	9	27	12

4.3.1 OTA

The folded cascode OTA (Allen *et al.* 1987) is used to implement the switched-capacitor integrator as shown in figure 4.10. In previous section it is discussed that a DC gain of 80 dB is sufficient to keep the third harmonic distortion below -90 dBc. The slew rate and UGB requirements of OTA depend on the clock frequency used for a particular resolution from 8-bit to 15-bit. The designed ADC operates as SAR ADC for 8-11 bits and first-order multi- bit SAR quantizer DSM for 12-15 bits. Therefore, a first-order N- bit quantizer DSM requires $(N+1)\cdot OSR$ clock cycles for conversion. The Nyquist sampling frequency is 2 kHz. Table 4.3 lists the quantizer resolution, OSR and frequency (f_{clk}) of the clock. The required slew rate and UGB of OTA are determined from clock frequency using equations (3.8), (3.10) and are tabulated. The bias current of folded cascode OTA and clock frequency are chosen according to ADC resolution.

The FC OTA is designed such that it operates in weak inversion region for all bias currents. The transistors are sized in such a way that, the flicker noise as well as the effect of transistor mismatch (Pelgrom *et al.* 1989) are less. Figure 4.11 shows AC response of FC OTA for all bias currents. It is observed that, the DC gain of OTA is greater than 80 dB in all these cases and also the required slew rate and UGB have been achieved. Also, the phase margin is above 60^o for all cases which can be seen from figure 4.11b. Further, the DC analysis is carried out by varying the input voltage. Figure 4.12 shows the DC gain variation over output swing. It confirms the variation in DC gain is less than 1 dB over $\pm 0.54\,V$ output swing, which helps to reduce the harmonics.

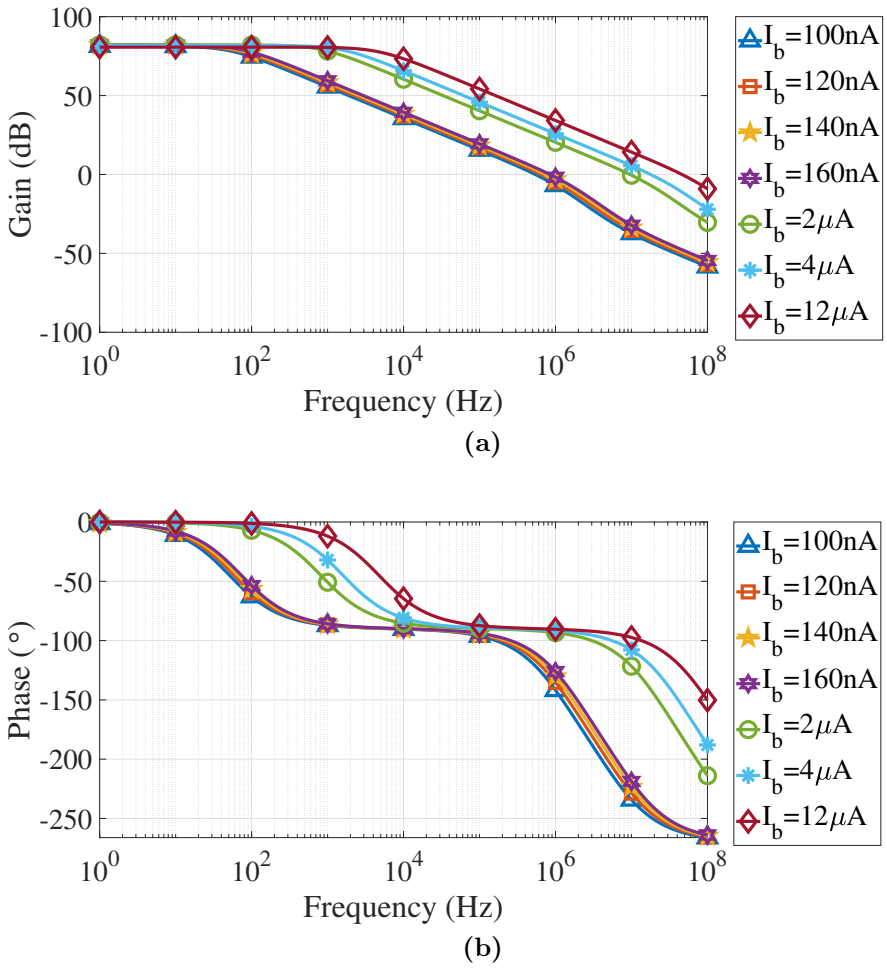


Figure 4.11: FC OTA AC analysis (a) Magnitude response (b) Phase response.

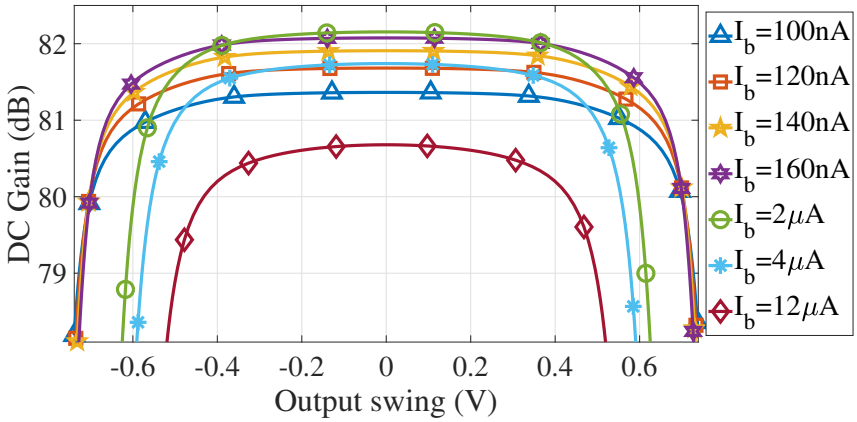


Figure 4.12: FC OTA DC Gain vs. output swing.

4.3.2 Digital Control logic unit

The block level diagram of digital control logic circuit is shown in figure 4.13. It is designed using verilog-A and then synthesized. The resolution of ADC is programmable using a 3-bit select bus $res[2:0]$. The SAR resolution controller programs the counter as per the chosen resolution. The counter starts counting on every positive edge of clock and generates EoC signal when it reaches the upper limit. Meanwhile, the comparator output (D_{out}) is stored in SIPO for every clock cycle. At the end of conversion, EoC signal triggers SIPO and gives out the N- bit digital data. The switch control logic takes the comparator output (D_{out}), EoC and clk as input signals and generates the control signals for all switches ($S_{1:16}$) in every clock cycle.

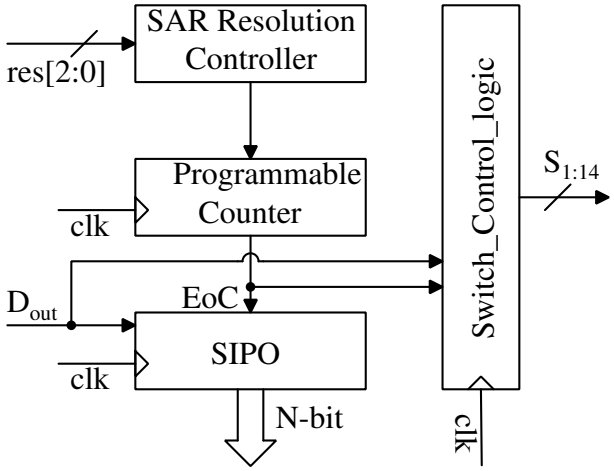


Figure 4.13: Block diagram of digital control logic.

4.4 Results

The proposed programmable resolution ADC is laid out in UMC 180 nm 1P6M CMOS technology as shown in figure 4.14 and occupies an area of 725 μm x 315 μm. The capacitors C_1=C_2=C_3=C_4=1 pF and C_5=C_6=3.3 pF are implemented using MIM capacitors and dummy capacitors are placed around this capacitor bank to minimize the interference as well as mismatch. Also, the analog and digital layouts are separated by guard rings and distinct supply voltages are used to reduce cross talk. Further, the post layout simulations are carried out with an ADC full scale range of 1.8 V differential with a Nyquist sampling frequency of 2 kS/s. Figure 4.15 and 4.16 show the ADC

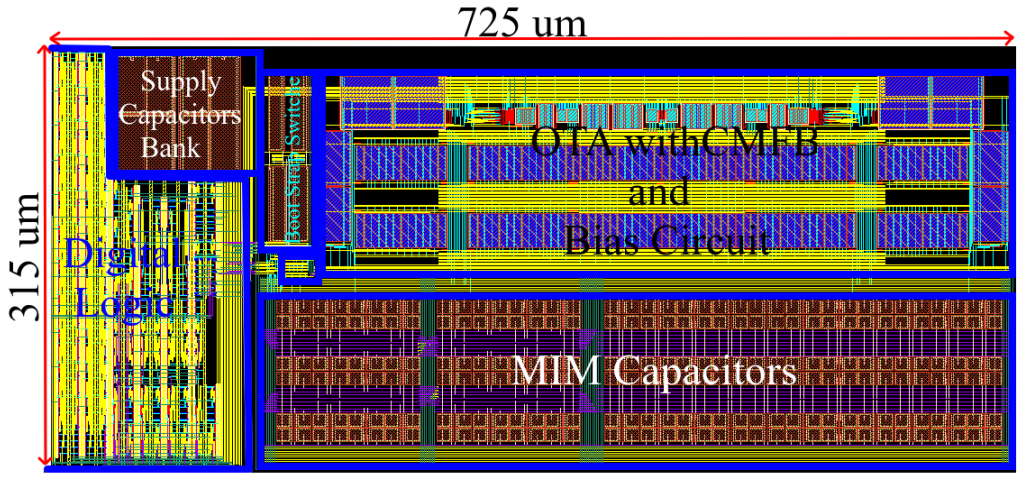
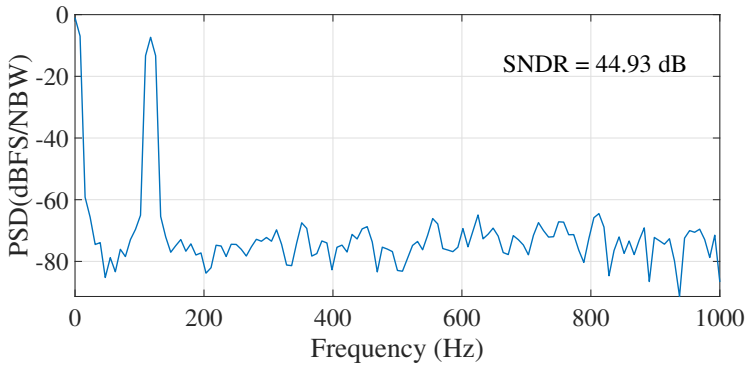


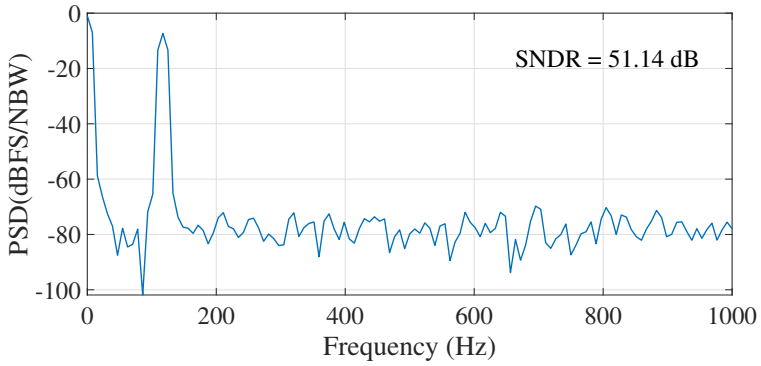
Figure 4.14: Layout of PADC.

output spectrum for resolutions from 8-bit to 15-bit respectively. The first-order noise shaping (20 dB/decade) can be observed in the resolution modes 12-bit to 15-bit. The number of FFT points used for ADC simulations from 8-bit to 11-bit is 256. 12-bit and 13-bit ADC simulations used 4,096 FFT points. 14-bit ADC simulations used 8,192 FFT points and 15-bit ADC simulations used 32,768 FFT points. The results of ADC simulations for various resolution modes (8-bit to 15-bit) are summarized in table 4.4. The proposed ADC offers adequate ENoB for each resolution mode.

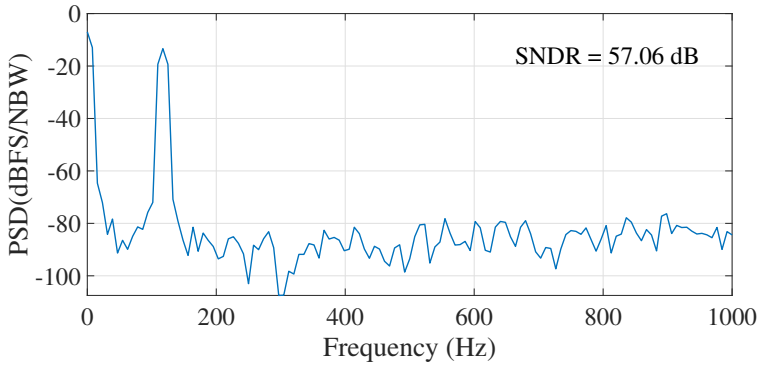
Figure 4.17 shows the plot of SNDR of the proposed ADC over a normalized input with respect to full signal swing for all resolution modes (8-15 bit). Also, figure 4.18 depicts a consistent SNDR over an input signal frequency for all target resolutions. Figure 4.19 shows the stacking diagram of power consumption by OTA, digital control logic, DAC and comparator. Table 4.5 shows the comparison of the performance of



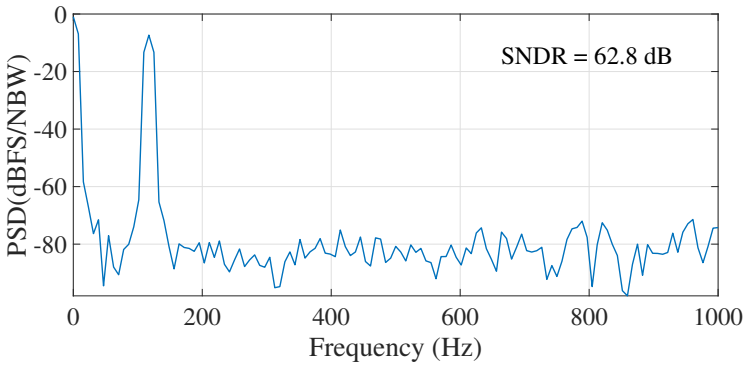
(a)



(b)

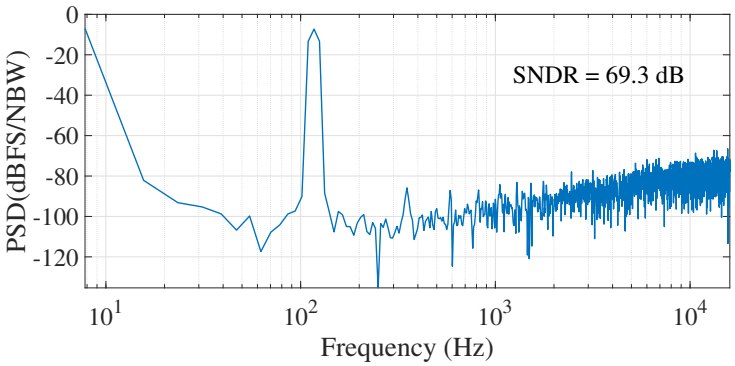


(c)

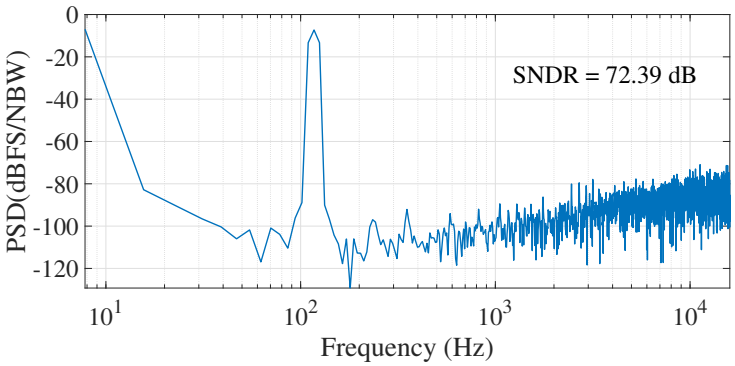


(d)

Figure 4.15: PADC output spectrum for various resolutions @f_{in} = 117 Hz, 256 FFT points (a) 8-bit, (b) 9-bit, (c) 10-bit, (d) 11-bit.

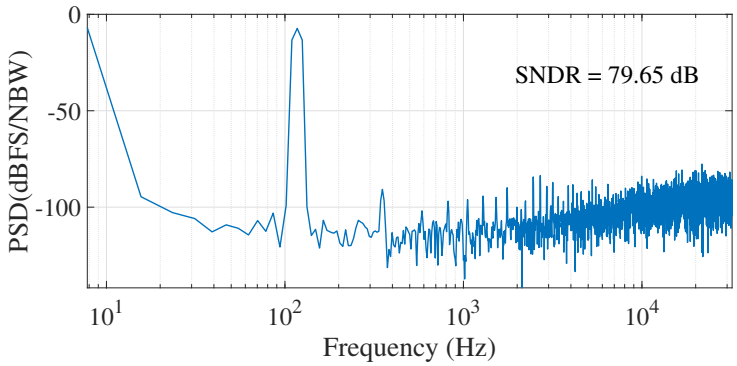


(a)

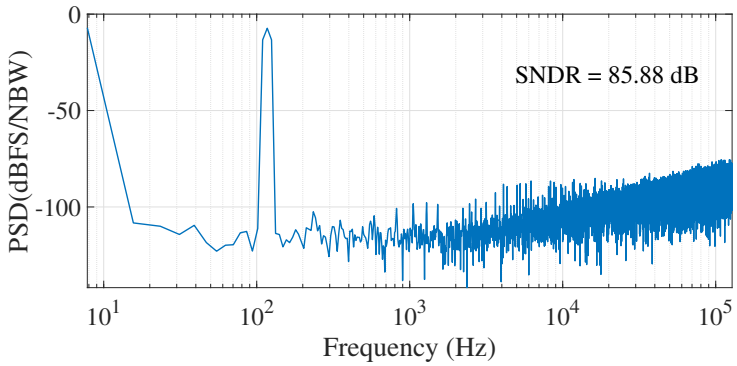


(b)

proposed ADC with similar type ADCs. It can be seen that the proposed ADC is on par with many designs found in state-of-the-art and demonstrated a new approach to implement programmable resolution ADC.



(c)



(d)

Figure 4.16: PADC output spectrum for various resolutions @f_{in} = 117 Hz (a) 12-bit, 4096 FFT points (b) 13-bit, 4096 FFT points (c) 14-bit, 8192 FFT points (d) 15-bit, 32768 FFT points.

Table 4.4: PADC post layout simulation results summary.

Target resolution	OSR	SAR	f_{clk}	ENoB (bits)	SFDR (dB)	Power (μW)
8	1	8	18	7.17	58.37	0.856
9	1	9	20	8.2	63.5	1.02
10	1	10	22	9.18	69.14	1.17
11	1	11	24	10.14	66.3	1.287
12	16	7	256	11.22	76.4	12.47
13	16	8	288	11.73	77.8	14.95
14	32	8	576	12.9	83.7	33.06
15	128	6	1792	13.97	91.63	98.35

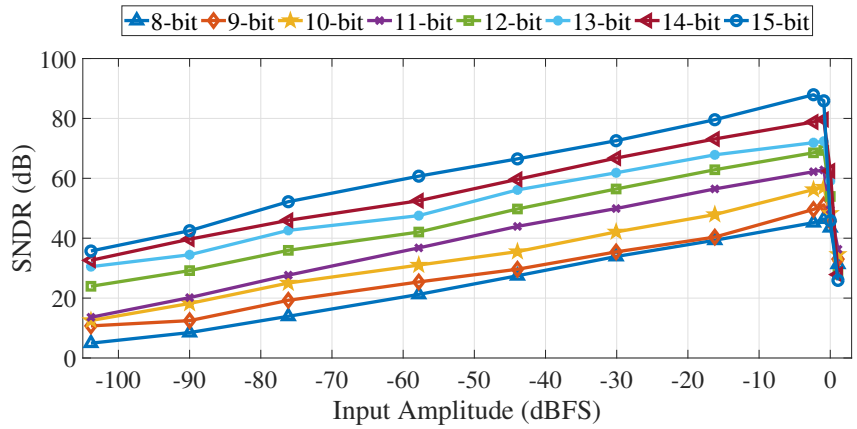


Figure 4.17: Variation in SNDR with input amplitude for various resolutions.

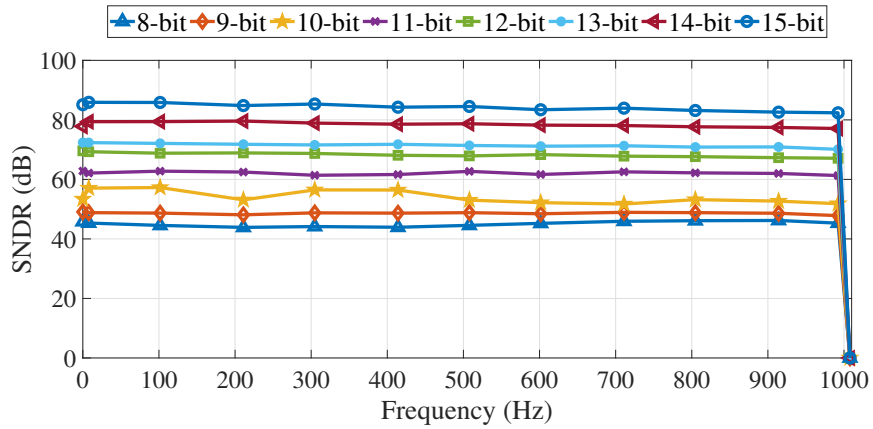


Figure 4.18: Variation in SNDR over input signal bandwidth for various resolutions.

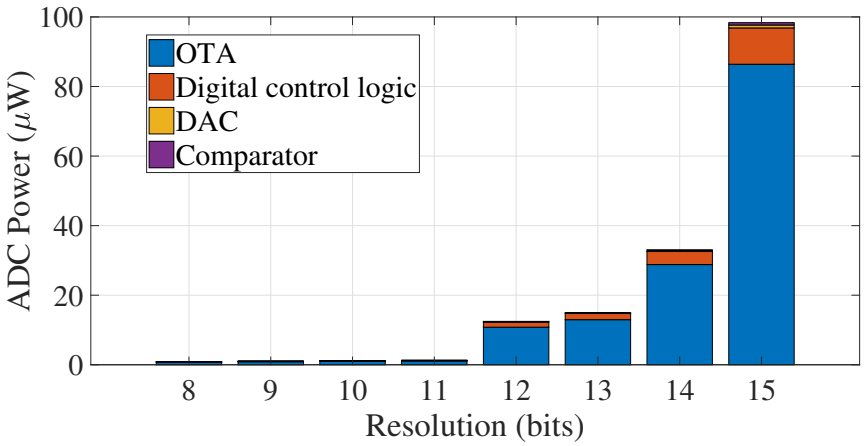


Figure 4.19: PADC power consumption vs. resolution.

Table 4.5: A summary of performance and comparison of programmable resolution ADC.

	Kumar *et al.* (2009)	Varshney *et al.* (2013)	Yip and Chandrakasan (2013)	Chaturvedi *et al.* (2013)	Zhu *et al.* (2014)	Nasserian *et al.* (2019)	**This Work**
Technology (nm)	65	45	65	130	180	180	180
Supply voltage (V)	0.8	1.2	1	1	0.5 - 0.9	1	1.8
Resolution (bits)	8, 10, 12	4, 5, 6	5 - 10	1 - 8	6 - 10	1 - 10	8 - 15
Sampling rate	200 MS/s	240 MS/s	200 kS/s	1 MS/s	2 MS/s	5 kS/s	2 kS/s
Area (mm^2)	-	-	0.3525	0.1638	0.21	0.0205	0.228
SNDR (dB)	69.1 @ 12	23.4 @ 4 28.8 @ 5 35.4 @ 6	30.4 - 55	48.1 @ 8	36.8 - 56.4	57.59 @ 10	45 - 86
Power (μW)	16000 @ 8 20000 @ 10 24000 @ 12	80 @ 4 96 @ 5 1150 @ 6	0.91 - 2.77	1.76 - 8.8	10.4 - 22.1	0.42 @ 10	0.86 - 98
FoMS (dB)	168.3 @ 12	148.17 @ 4 152.87 @ 5 78.6 @ 6	143.8 - 163.5	98.65 @ 8	149.6 - 165.9	158.35 @ 10	138.7 - 159.1

Chapter 5

CONCLUSIONS AND FUTURE DIRECTIONS

5.1 Conclusions

SAR ADC is well suited for moderate resolution and energy efficient applications such as biomedical signal acquisition. Therefore, this research is focused in the direction of optimizing the power consumption and area aspects of conventional SAR ADC. In this approach, a novel energy efficient differential switching scheme for feedback DAC used in SAR ADC is proposed to reduce the power consumption as well as area. The proposed switching scheme utilizes single reference voltage V_{cm} (i.e. $0.5V_{ref}$) and improves the switching energy efficiency. The proposed switching scheme is 96.88 % energy efficient and 50 % capacitor area efficient than conventional switching scheme. A 10-bit SAR ADC is designed and simulated in UMC 90 nm CMOS 1P9M process technology with supply voltage of $0.5\,V$. The proposed SAR ADC achieves 55.93 dB SNDR, which is equivalent to ENoB of 9 bits. The obtained SFDR for SAR ADC is 77.17 dB. The FoMW is calculated, and it is 38.67 fJ/conv.

Further, a switched capacitor based SAR ADC is proposed based on passive reference charge sharing and charge accumulation technique which uses less number of capacitors compared to conventional SAR ADC. The passive charge sharing technique is used to generate the necessary reference voltages for SAR ADC. To validate the functionality of the proposed SAR ADC design, a model has been developed in MATLAB and the behavioral simulations are carried out. Later, the non-idealities of practical amplifier and their effects on the proposed ADC are discussed. These non-idealities

are incorporated into MATLAB model and their effects on the ADC characteristics are evaluated. The proposed ADC is designed using UMC 180 nm 1P6M CMOS technology for a target resolution of 11-bits. The post–layout simulations prove that the ADC achieved 10.14 bits of ENoB, FoMW of 0.12 pJ/conv-step by consuming 0.28 μW and occupies an area of 0.17 mm^2. Also, the histogram testing shows that both INL and DNL are less than $\pm$ 1 LSB.

In addition, a novel fully differential switched-capacitor integrator based programmable resolution hybrid ADC architecture is proposed. An 8-bit to 15-bit programmable resolution ADC is implemented to verify the proposed method. Also, the effects of non-idealities of OTA, such as finite values of gain, UGB and slew rate on ADC characteristics are modelled and studied through behavioural simulations. Further, the non-linearity in ADC characteristics due to the capacitors' mismatch is also calculated. The proposed ADC is designed and laid out in UMC 180 nm 1P6M CMOS technology and occupies an area of 0.228 mm^2. Post layout simulations show that the proposed ADC achieves an adequate SNDR in all resolution modes (8-bit to 15-bit). The total design consumes 0.86 μW to 98 μW in 8 to 15-bit resolutions respectively from a supply voltage of 1.8 V.

5.2 Future Directions

The supply voltage plays a crucial role in the linearity of SAR ADC transfer characteristics. Also, the large capacitors in the feedback DAC need to be charged in less time with greater accuracy. Therefore, it will be quite interesting to design on-chip low-dropout (LDO) regulators to generate supply voltages for large load capacitors with wide range of load currents.

In this thesis, the design of input buffers for ADCs, which drive the large sampling capacitors in the feedback DAC, is not investigated. Also, to support the high ADC sampling rates, the input buffer needs to be designed with high slew rate as well as UGB, which requires very large bias currents. Therefore, it will be a challenging task to design input buffer circuits with low power consumption.

In recent years, multiple recording channels become popular in low frequency applications. These applications demand either high sample rate ADCs for time multiplexing or dedicated ADCs for each channel. The proposed switched capacitor based ADCs are using OTA as one of their main blocks. The OTA contributes major portion

of the ADC power consumption. Also, the finite gain, slew rate and UGB of OTA limits the ADC linearity. High sampling rate ADCs need large slew rate as well as UGB. Therefore, designing a simple OTA with all the requirements operating with low voltage, consuming less power will be quite challenging.

The higher order modulators with SAR quantizer can achieve high resolutions with low OSR. This relaxes the required specifications of OTA. Therefore, there is a high scope for research to design higher order cascode architectures using SAR quantizer.

The future IC trends depend a lot more on migrating to smaller technology nodes because of the ultra-low voltage operation, reduction in chip area and integration of more functions at a lesser cost. Migrating to sub 100 nm technology reduces the area occupied by capacitors. However, the real challenge is the design of some of the analog blocks such as OTA with sub 100 nm technologies. Analog blocks at sub 100 nm technology nodes lead to significant short channel effects and degrade the performance severely. Therefore, there is a scope for the design of analog blocks such as OTA in sub 100 nm technologies that are robust in their performance and reliability.

The major challenge in wireless sensor networks wherein the sensors are located at remote places and the data is transmitted wirelessly is that the power consumed by the wireless data transceivers is much higher than the power consumed by the sensors in capturing the data. Therefore, the field of ultra-low-power transceiver design has great scope, and research in this field can revolutionize sensor networks.

Appendix I
ADC Characterization metrics

The performance of ADC is determined from both transfer characteristics and dynamic characteristics. Optimization of application specific critical metrics help in achieving an improved performance. Some significant characterization metrics used for ADC are discussed here.

A-1 Static Metrics

The accuracy of signal is limited by deviation of transfer characteristics of ADC from ideal one. Ideally, this characteristic is a staircase with perfectly uniform and identical steps with step size 1LSB over full scale dynamic range as shown in figure A.1a. Deviations from this ideal transfer characteristics are measured in terms of DC Characterization metrics of the converter.

Quantization error

The output of ADC is N-bit digital sequence which has finite number of values $\left(2^N\right)$ whereas the input is infinite valued signal. Here N is known as the resolution of the ADC. The input dynamic range is divided into 2^N discrete levels. The difference between adjacent reference levels is called as LSB which signifies the minimal change at the output. Thus, the sampled input value is rounded off to nearest reference level. This round-off process is known as quantization which adds an error signal (Q_e).

$$Q_e = V_{in} - V_{out} \tag{A.1}$$

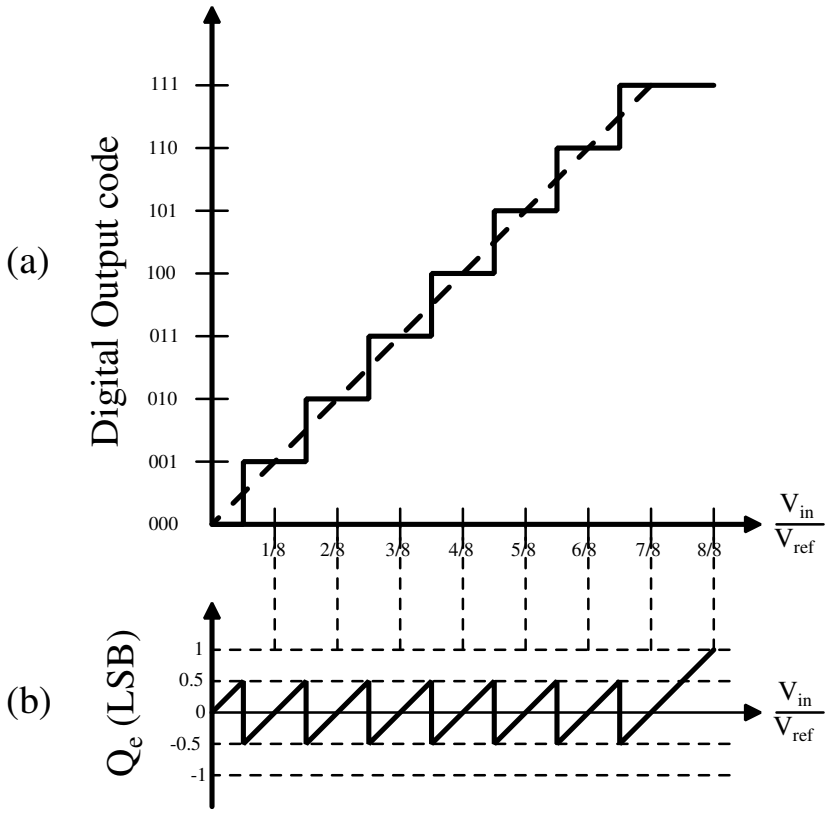


Figure A.1: 3-bit Ideal ADC characteristics (Baker 2008*a*) (a) Transfer characteristics (b) Quantization error.

This quantization error puts a theoretical upper limit on achievable resolution even in ideal ADC . Figure A.1b shows the variation of quantization error with input signal. Ideally, the quantization error is limited to ± 0.5 LSB when input lies within the dynamic range of ADC. On the other hand, when the input signal overloads the quantizer, (i.e. input signal exceeds quantizer dynamic range) the quantization error increases. This phenomenon is known as quantizer saturation. The rms value of the quantization error (Q_e) is calculated as in equation (A.2) (Baker 2008*a*)

$$Q_{e,rms} = \sqrt{\frac{1}{V_{LSB}} \int_{-0.5V_{LSB}}^{0.5V_{LSB}} (V_{LSB})^2 dV_{LSB}} = \frac{V_{LSB}}{\sqrt{12}} \tag{A.2}$$

Offset

The deviation of the first code transition from 0.5 LSB is defined as offset error. It shifts all code transitions by the same amount leading to deviation in the mean value

of quantization error which can be corrected digitally. The graphical representation of offset is shown in figure A.2.

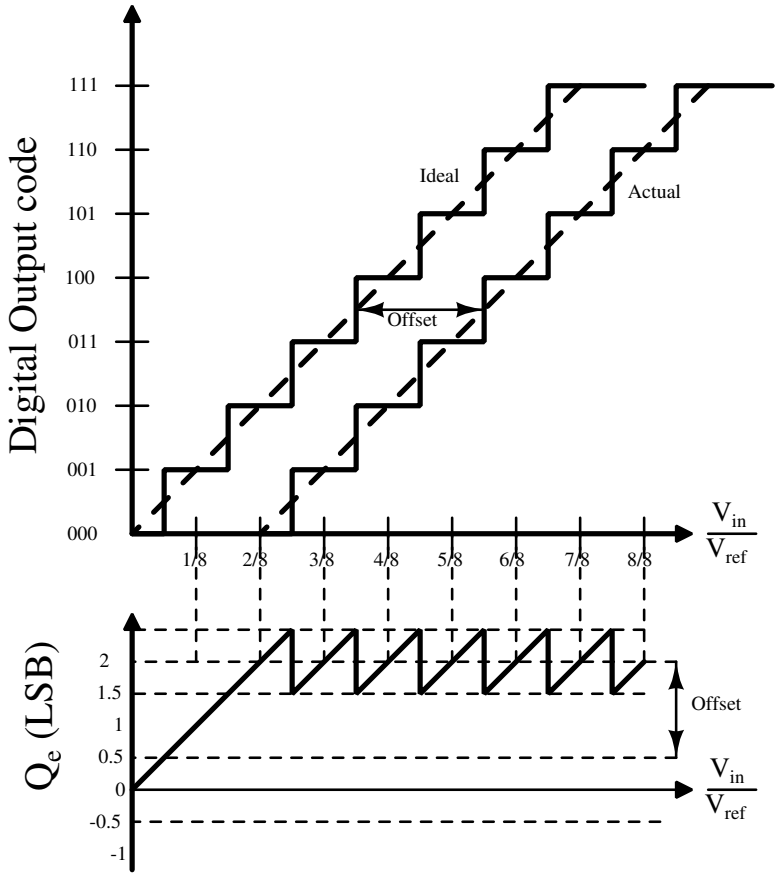


Figure A.2: 3-bit ADC transfer characteristics with Offset (Baker 2008*a*).

Gain error

The gain of an ADC is defined as the slope of straight line by interpolating the transfer characteristic of an ADC. The deviation of gain from the ideal ADC gain is known as gain error or scale factor error. Figure A.3 shows the transfer characteristics and quantization error of an ADC which has gain error. Gain error gives information about mean deviation of LSB from ideal one. In most of the applications small gain error and offset errors are tolerable because the linearity of transfer characteristics are not affected. Moreover, these errors can be calibrated digitally.

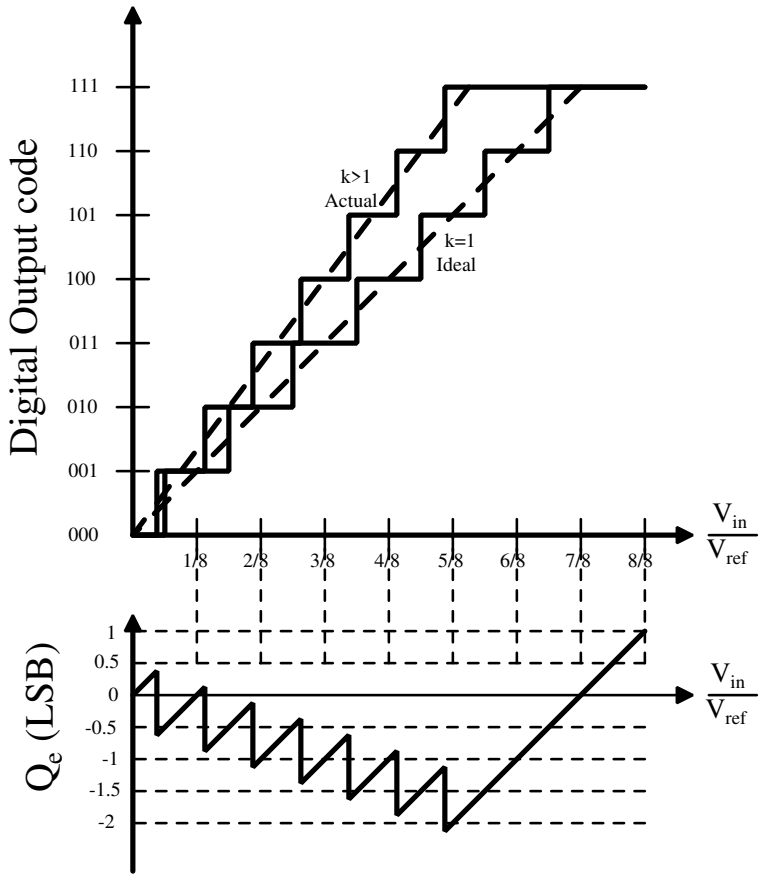


Figure A.3: 3-bit ADC transfer characteristics with Gain error (Baker 2008*a*).

Non linearity

In practical ADC, the step size of all transition codes is non-uniform. This introduces non linearity in transfer characteristics as shown in figure A.4. Thus, the random variation of step sizes given by DNL and the correlation between successive step sizes specified by INL. All information about transfer characteristics of an ADC can be measured by mentioning all code widths or code transitions. Figure A.4 illustrates INL and DNL.

DNL

DNL is defined as the normalized deviation of each individual code step size from LSB (i.e. ideal step size).

$$DNL(k) = \frac{V_{k+1} - V_k}{LSB} - 1 \qquad k = 0, 1, ...N - 1 \qquad \text{(A.3)}$$

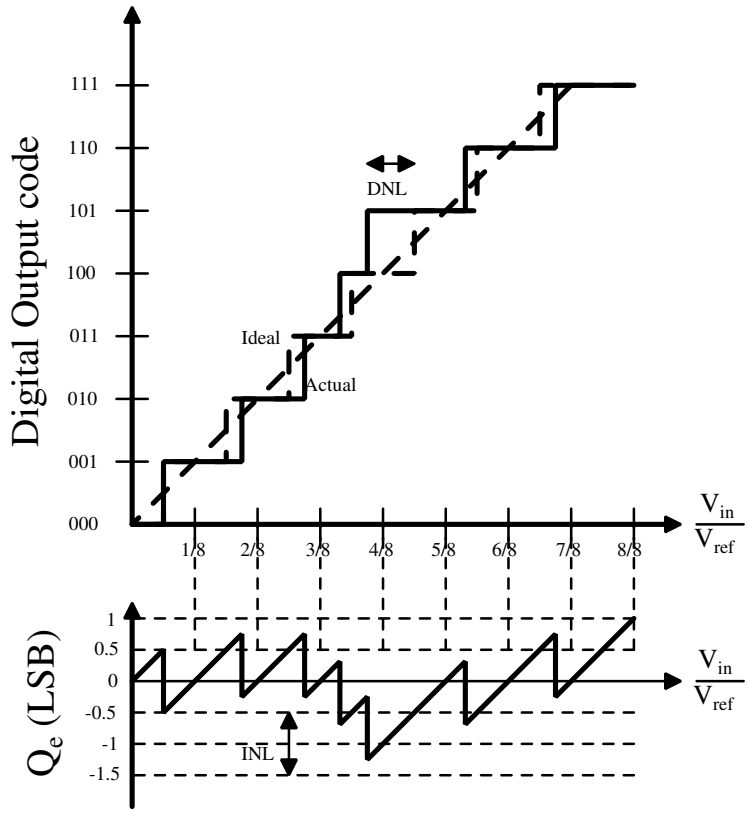


Figure A.4: 3-bit ADC characteristics with non linearity (Baker 2008*a*).

Here, V_k is the input voltage at which the output of ADC changes from code $(k-1)$ to k. DNL gives information about the slope of transfer characteristics of ADC at local point. If any step size is 0, then the corresponding code does not exist. Thus, DNL $\leq$ -1 LSB implies missing code. Thus, an absolute value of DNL less than one LSB ensures that all codes exist and is also a sufficient condition for preserving the monotonicity of transfer characteristics. The increase in quantization error is directly proportional to absolute value of DNL.

INL

INL is defined as the normalized deviation of each individual code transition from the ideal one. Graphically, INL is interpreted as the deviation in transfer characteristics of an ADC from a straight line passing through the first and last code transitions.

$$INL(k) = \frac{V_k}{LSB} - k \qquad\qquad k = 0, 1, ...N-1 \qquad\qquad (A.4)$$

INL and DNL are dependent on each other and both present same information in two ways. INL gives the broader picture of transfer characteristics where as DNL gives the granularity in a certain region.

$$INL(k) = \sum_{i=0}^{k-1} DNL(i) \qquad k = 0, 1, ...N-1 \tag{A.5}$$

$$DNL(k) = INL(k+1) - INL(k) \tag{A.6}$$

There are certain applications in which DNL is more important than INL and vice versa. For example, the feedback systems and displays need low DNL and communication systems need low INL characteristics.

A-2 Dynamic Metrics

The overall performance of an ADC is limited by the distortion, that occurs due to several dynamic aspects. All these dynamic effects are studied in spectral analysis of the ADC output (Baker 2008*b*).

Aliasing

The sampling process introduces alias of the original signal at different frequencies in input signal spectrum. These alias components can be filtered using low pass filter, if all aliasing frequencies are greater than the actual input signal frequency. Thus, the sampling frequency must satisfy Nyquist criteria.

$$f_{alias} = f_{in} + kf_s \qquad (k = ... - 1, 0, 1, ...) \tag{A.7}$$

Aperture error

The sampling clock jitter changes the sampling instant slightly. This introduces an error for a sample input signal and it depends on the local slope of input as shown in figure A.5. This distortion appears as noise and degrades the signal to noise ratio, since clock jitter is a random variable. Equation (A.8) shows that the rms error increases with the frequency of input signal.

$$\text{Sampling error at } nT_s = \text{Slope of signal at } nT_s * \delta t$$

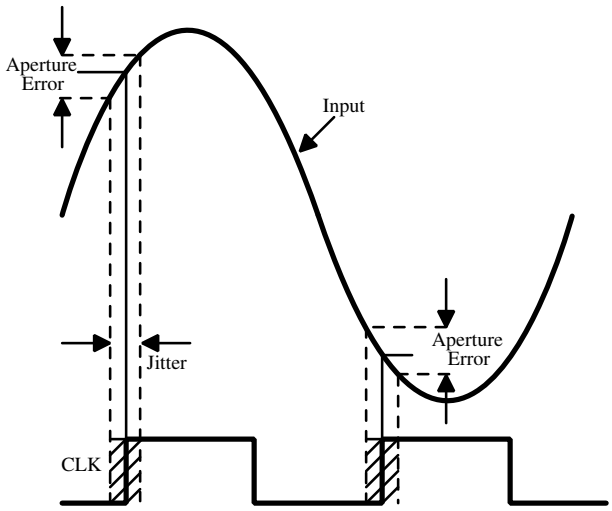


Figure A.5: Aperture Error (Baker 2008*a*).

Here δt is the uncertainty of clock from ideal one at nT_s.
Let $V_{in} = A\ sin\ 2\pi f_{in}t$ and δV_{in} be the sampling error then,

$$\begin{aligned} \delta V_{in} &= \frac{dV_{in}}{dt}\Big|_{nT_s} * \delta t \\ \delta V_{in} &= 2\pi f_{in} A\ cos\ 2\pi f_{in} nT_s * \delta t \\ \delta V_{in,rms} &= \sqrt{2}\pi f_{in} A \end{aligned} \tag{A.8}$$

Signal to Noise and Distortion Ratio (SNDR)

In ideal case, an ADC adds quantization noise only. Thus the SNR at the output of an ADC is calculated theoretically using equations (A.9) and (A.10).

$$SNR_{ideal,dB} = 20\log_{10}\left(\frac{V_{in,rms}}{Q_{e,rms}}\right) \tag{A.9}$$

$$= 20\log_{10}\left(\frac{\frac{V_{REF}}{2\sqrt{2}}}{\frac{V_{REF}}{2^N\sqrt{12}}}\right)$$

$$SNR_{ideal,dB} = 6.02N + 1.76 \tag{A.10}$$

The deviation of transfer characteristics from ideal one results in additional distortion in practical ADC. Aperture error caused by clock jitter also adds some noise. Moreover, thermal and flicker noise of circuit components and harmonic distortion also appear in the spectrum of output signal. All these noise components deviate the SNR from its theoretical value. SNDR is defined as the ratio of input signal power and total rms power of noise and distortion, as given in equation (A.11). SNDR is also referred to as SINAD.

$$SNDR_{dB} = 10\log_{10}\left(\frac{V_{in}^2}{2(V_{Q_e}^2 + V_{Distortion}^2)}\right) \tag{A.11}$$

Effective Number of Bits (ENoB)

In practice, an ADC introduces not only quantization noise but also some additional noise as discussed above. ENoB is a measure of the effective resolution of an ADC accounting for all noise components including quantization noise. The relation between ENoB and SNDR is given in equation (A.12).

$$ENoB = \frac{SNDR - 1.76}{6.02} \tag{A.12}$$

where SNDR is measured in dB.

Spurious Free Dynamic Range (SFDR)

SFDR relates the input signal and the largest spike in the output spectrum upto nyquist frequency. SFDR strongly correlates with input signal because the harmonic components of input are reflected as highest peaks in output spectrum at larger inputs, as given in equation (A.13).

$$SFDR(dBc) = \text{input signal}(dB) \ - \ \text{higest spur}(dB) \tag{A.13}$$

Dynamic Range (DR)

Ideally, the dynamic range(DR) is defined as the ratio of maximum output signal change over minimum output signal change, as in equation (A.14).

$$DR = 20\log_{10}\left(\frac{V_{REF+} - (V_{REF+} - V_{REF-})/2^N - V_{REF-}}{(V_{REF+} - V_{REF-})/2^N}\right) = 6.02N \tag{A.14}$$

A further way to specify DR is the ratio of input signal amplitude when SFDR is 0 dBc to the input signal amplitude when SNDR is 0 dB.

A-3 Figures of Merit

The main performance metrics of an ADC are represented in terms of resolution, bandwidth and power consumption. There is a trade-off between these three and ADCs are designed according to the application. Hence, difficulty arises when comparing several ADC architectures. This leads to evolution of figures of merit (FoM) after reviewing a huge number of ADCs. This allows designers to compare energy efficiency of ADCs operating in different conditions.

Figure of Merit by Walden (FoMW)

FoMW is introduced by (Walden 1999) assuming that the power consumption of an ADC increases linearly with sampling frequency and SNDR. This defines the energy required per conversion-step in terms of pico Joules per conversion step (pJ/conversion-step) is given in equation (A.15).

$$FoMW = \frac{Power}{2^{ENoB} f_{sample}} \tag{A.15}$$

Figure of Merit by Schreier (FoMS)

The accuracy of high resolution ADCs is mostly limited by thermal noise. The reduction in thermal noise by half leads to four times increase in power consumption. Initially, this constraint was explored by (Rabii and Wooley 1997) and a new expression for FoM was proposed. Later, this was reformulated by (Schreier *et al.* 2005) in dB scale, as given in equation (A.16) which is known as FoMS. Here, power consumption of an ADC is measured in watts.

$$FoMS = SNDR_{dB} + 10 \log_{10} \left(\frac{2 f_{in}}{Power} \right) \tag{A.16}$$

Bibliography

Allen, P. E., **D. R. Holberg**, **P. E. Allen**, and **P. Allen**, *CMOS analog circuit design*. Holt, Rinehart and Winston New York, 1987.

Alvarez-Fontecilla, E. and **A. Abusleme** (2015). Passive reference-sharing SAR ADC. *Microelectronics Journal*, **46**(8), 750–757.

Aminzadeh, H. (2019). A Low-Cost Tiny-Size Successive Approximation ADC for Applications Requiring Low-Resolution Conversion with Moderate Sampling Rate. *Circuits, Systems, and Signal Processing*, **38**(1), 242–258.

Asghar, S., **S. S. Afridi**, **A. Pillai**, **A. Schuler**, **M. José**, and **I. O'Connell** (2018). A 2-MS/s, 11.22 ENOB, extended input range SAR ADC with improved DNL and offset calculation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **65**(11), 3628–3638.

Babayan-Mashhadi, S. and **R. Lotfi** (2014). Analysis and design of a low-voltage low-power double-tail comparator. *IEEE transactions on very large scale integration (vlsi) systems*, **22**(2), 343–352.

Baker, R. J., *CMOS: circuit design, layout, and simulation*, volume 1. John Wiley & Sons, 2008*a*.

Baker, R. J., *CMOS: mixed-signal circuit design*. John Wiley & Sons, 2008*b*.

Chang, A. H. T. (2013). *Low-power high-performance SAR ADC with redundancy and digital background calibration*. Ph.D. thesis, Massachusetts Institute of Technology.

Chang, Y.-K., **C.-S. Wang**, and **C.-K. Wang**, A 8-bit 500-KS/s low power SAR ADC for bio-medical applications. *In Solid-State Circuits Conference, 2007. ASSCC'07. IEEE Asian*. IEEE, 2007.

Chaturvedi, V., **T. Anand**, and **B. Amrutur** (2013). An 8-to-1 bit 1-MS/s SAR ADC with VGA and integrated data compression for neural recording. *IEEE transactions on very large scale integration (VLSI) systems*, **21**(11), 2034–2044.

Chen, B., **M. Maddox**, **M. C. Coln**, **Y. Lu**, and **L. D. Fernando** (2018). Precision passive-charge-sharing SAR ADC: Analysis, design, and measurement results. *IEEE Journal of Solid-State Circuits*, **53**(5), 1481–1492.

Chen, C.-H., **Y. Zhang**, **J. Ceballos**, and **G. Temes** (2013). Noise-shaping SAR ADC using three capacitors. *Electronics Letters*, **49**(3), 182–184.

Chen, S.-L., **J. F. Villaverde**, **H.-Y. Lee**, **D. W.-Y. Chung**, **T.-L. Lin**, **C.-H. Tseng**, and **K.-A. Lo** (2017). A power-efficient mixed-signal smart ADC design with adaptive resolution and variable sampling rate for low-power applications. *IEEE Sensors Journal*, **17**(11), 3461–3469.

Çikan, N. N. and **M. Aksoy**, Analog to digital converters performance evaluation using figure of merits in industrial applications. *In 2016 European Modelling Symposium (EMS)*. IEEE, 2016.

Craninckx, J. and **G. Van der Plas**, A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90nm digital CMOS. *In 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*. IEEE, 2007.

Das, I., **M. Sahoo**, **P. Roy**, and **H. Rahaman**, A 45 uW 13 pJ/conv-step 7.4-ENOB 40 kS/s SAR ADC for digital microfluidic biochip applications. *In 18th International Symposium on VLSI Design and Test*. IEEE, 2014.

Fazel, Z., **S. Saeedi**, and **M. Atarodi** (2016). Pipelining method for low-power and high-speed SAR ADC design. *Analog Integrated Circuits and Signal Processing*, **87**(3), 353–368.

Ginsburg, B. P. and **A. P. Chandrakasan**, An energy-efficient charge recycling approach for a SAR converter with capacitive DAC. *In Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*. IEEE, 2005.

Hariprasath, V., **J. Guerber**, **S.-H. Lee**, and **U.-K. Moon** (2010). Merged capacitor switching based SAR ADC with highest switching energy-efficiency. *Electronics Letters*, **46**(9), 620–621.

Jespers, P., *The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches*. Springer Science & Business Media, 2009.

José, M. (2011). Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **58**(1), 1–21.

José, M., **R. Schreier**, **K.-P. Pun**, and **S. Pavan** (2015). Next-generation delta-sigma converters: trends and perspectives. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **5**(4), 484–499.

Kumar, A. M., **S. Veeramachaneni**, and **M. Srinivas**, A novel low power, variable resolution pipelined ADC. *In 2009 IEEE International SOC Conference (SOCC)*. IEEE, 2009.

Le, H., **J. Singh**, **L. Hiremath**, **V. Mallapur**, and **A. Stojcevski** (2005). Ultra-low-power variable-resolution successive approximation ADC for biomedical application. *Electronics letters*, **41**(11), 634–635.

Liu, C.-C., **S.-J. Chang**, **G.-Y. Huang**, and **Y.-Z. Lin** (2010). A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits*, **45**(4), 731–740.

Mahmoud, S. A., **H. A. Salem**, and **H. M. Albalooshi** (2015). An 8-bit, 10 KS/s, 1.87 μW Successive Approximation Analog to Digital Converter in 0.25 μm CMOS Technology for ECG Detection Systems. *Circuits, Systems, and Signal Processing*, **34**(8), 2419–2439.

McCreary, J. L. and **P. R. Gray** (1975). All-MOS charge redistribution analog-to-digital conversion techniques. I. *IEEE Journal of Solid-State Circuits*, **10**(6), 371–379.

Mekkattillam, Y., **S. Mohapatra**, and **N. R. Mohapatra**, Design and Calibration of 14-bit 10 KS/s Low Power SAR ADC for Bio-medical Applications. *In International Symposium on VLSI Design and Test*. Springer, 2019.

Murmann, B. *et al.* (2016). ADC performance survey 1997–2016. *Online: http://www. stanford. edu/murmann/adcsurvey. html*.

Nasserian, M., **A. Peiravi**, and **F. Moradi** (2019). An adaptive-resolution signal-specific ADC for sensor-interface applications. *Analog Integrated Circuits and Signal Processing*, **98**(1), 125–135.

O'Driscoll, S., **K. V. Shenoy**, and **T. H. Meng** (2011). Adaptive resolution ADC array for an implantable neural sensor. *IEEE Transactions on Biomedical Circuits and Systems*, **5**(2), 120–130.

Pavan, S., **R. Schreier**, and **G. C. Temes**, *Understanding delta-sigma data converters*. John Wiley & Sons, 2017.

Pelgrom, M. J., **A. C. Duinmaijer**, and **A. P. Welbers** (1989). Matching properties of mos transistors. *IEEE Journal of solid-state circuits*, **24**(5), 1433–1439.

Polineni, S. and **A. K. Gupta**, 8-bit Nano watt level crossing ADC for bio-medical application. *In 2015 International Conference on Computer, Communication and Control (IC4)*. IEEE, 2015.

Quinn, P. J. and **A. H. Van Roermund**, *Switched-capacitor techniques for high-accuracy filter and ADC design*. Springer Science & Business Media, 2007.

Rabii, S. and **B. A. Wooley** (1997). A 1.8-V digital-audio sigma-delta modulator in 0.8-/spl mu/m CMOS. *IEEE Journal of Solid-State Circuits*, **32**(6), 783–796.

Rabuske, T. and **J. Fernandes**, *Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications*. Springer, 2017.

Rahimi, E. and **M. Yavari** (2014). Energy-efficient high-accuracy switching method for SAR ADCs. *Electronics Letters*, **50**(7), 499–501.

Razavi, B. (2015). The bootstrapped switch [a circuit for all seasons]. *IEEE Solid-State Circuits Magazine*, **7**(3), 12–15.

Sanyal, A. and **N. Sun** (2013). SAR ADC architecture with 98% reduction in switching energy over conventional scheme. *Electronics Letters*, **49**(4), 248–250.

Schreier, R., **G. C. Temes**, *et al.*, *Understanding delta-sigma data converters*, volume 74. IEEE press Piscataway, NJ, 2005.

Srinivasan, S. and **P. Balsara** (2014). Energy-efficient sub-DAC merging scheme for variable resolution SAR ADC. *Electronics Letters*, **50**(20), 1421–1423.

Suarez, R. E., **P. R. Gray**, and **D. A. Hodges** (1975). All-MOS charge-redistribution analog-to-digital conversion techniques. II. *IEEE Journal of Solid-State Circuits*, **10**(6), 379–385.

Ting, H.-W., **B.-D. Liu**, and **S.-J. Chang** (2008). A histogram-based testing method for estimating A/D converter performance. *IEEE Transactions on Instrumentation and Measurement*, **57**(2), 420–427.

Varshney, S., **M. Goswami**, and **B. Singh**, 4-6 bit variable resolution ADC. *In 2013 International Symposium on Electronic System Design*. IEEE, 2013.

Walden, R. H. (1999). Analog-to-digital converter survey and analysis. *IEEE Journal on selected areas in communications*, **17**(4), 539–550.

Xie, L., **J. Su**, **J. Liu**, and **G. Wen** (2015). Energy-efficient capacitor-splitting DAC scheme with high accuracy for SAR ADCs. *Electronics Letters*, **51**(6), 460–462.

Xie, L., **G. Wen**, **J. Liu**, and **Y. Wang** (2014). Energy-efficient hybrid capacitor switching scheme for SAR ADC. *Electronics Letters*, **50**(1), 22–23.

Yazdani, B., **A. Khorami**, and **M. Sharifkhani** (2015). Low-power DAC with charge redistribution sampling method for SAR ADCs. *Electronics Letters*, **52**(3), 187–188.

Yazdani, B., **A. Khorami**, and **M. Sharifkhani** (2016). Low-power bottom-plate sampling capacitor-splitting DAC for SAR ADCs. *Electronics Letters*, **52**(11), 913–915.

Yip, M. and **A. P. Chandrakasan** (2013). A resolution-reconfigurable 5-to-10-bit 0.4-to-1 V power scalable SAR ADC for sensor applications. *IEEE Journal of Solid-State Circuits*, **48**(6), 1453–1464.

Yuan, C. and **Y. Lam** (2012). Low-energy and area-efficient tri-level switching scheme for SAR ADC. *Electronics letters*, **48**(9), 482–483.

Zheng, Z., **U.-K. Moon**, **J. Steensgaard**, **B. Wang**, and **G. C. Temes**, Capacitor mismatch error cancellation technique for a successive approximation A/D converter. *In Circuits and Systems, 1999. ISCAS'99. Proceedings of the 1999 IEEE International Symposium on*, volume 2. IEEE, 1999.

Zhu, Y., **C.-H. Chan**, **U.-F. Chio**, **S.-W. Sin**, **U. Seng-Pan**, **R. P. Martins**, and **F. Maloberti** (2010). A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS. *IEEE Journal of Solid-State Circuits*, **45**(6), 1111–1121.

Zhu, Z., **Z. Qiu**, **M. Liu**, and **R. Ding** (2014). A 6-to-10-Bit 0.5 V-to-0.9 V Reconfigurable 2 MS/s Power Scalable SAR ADC in 0.18 μm CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **62**(3), 689–696.

Zhu, Z., **Y. Xiao**, and **X. Song** (2013). V CM-based monotonic capacitor switching scheme for SAR ADC. *Electronics Letters*, **49**(5), 327–329.

Publications Based on the Thesis

Journals:

1. **Polineni, S.**, Bhat, M. S., & Rajan, A. (2019). A 10-Bit Differential Ultra-Low-Power SAR ADC with an Enhanced MSB Capacitor-Split Switching Technique. *Arabian Journal for Science and Engineering*, *Springer*, **44**(3), 2345–2353.

2. **Polineni, S.**, Bhat, M. S., & Rekha, S. (2020). A Switched Capacitor-Based SAR ADC Employing a Passive Reference Charge Sharing and Charge Accumulation Technique. *Circuits, Systems, and Signal Processing*, *Springer* **39**, 5352–5370. https://doi.org/10.1007/s00034-020-01437-3

3. **Polineni, S.**, Rekha, S., & Bhat, M. S. (2021). A fully differential switched-capacitor based programmable resolution hybrid ADC architecture for biomedical applications. *IET Circuits Devices Syst.*, **15**(2), 141–155. https://doi.org/10.1049/cds2.12014

Conferences:

1. Aparna, T., **Polineni, S.**, & Bhat, M. S., A three-stage operational transconductance amplifier for delta sigma modulator. *In 2018 IEEE Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER)*. IEEE, 2018.

2. Bonthala, S., Uppoor, Y., Nayak, A., **Polineni, S.**, & Bhat, M. S., Design of High Resolution Delta Sigma Modulator in 180 nm CMOS technology. *In 2019 9th International Symposium on Embedded Computing and System Design (ISED)*. IEEE, 2019.

BIODATA

NAME : SREENIVASULU POLINENI

DoB : 05/07/1992

CONTACT DETAILS

Address : Vennuru,

Kondapi Mandal, Prakasam dist.,

Andhra Pradesh, India-523279.

Email ✉ : polineni91@gmail.com

Phone ☎ : +91 8073480379, +919896003553.

EDUCATIONAL QUALIFICATIONS

Doctor of Philosophy (Ph.D)

National Institute of Technology Karnataka, Surathkal 2015–2021

Master of Technology (M.Tech)

National Institute of Technology Kurukshetra, Haryana. 2013–2015
Specialization: VLSI Design.

Bachelor of Technology (B.Tech)

Jawaharlal Nehru Technological University, Anantapur, A.P. 2009–2013
Branch: Electronics and Communication Engineering.

RESEARCH INTERESTS

Low power analog and mixed signal circuit design, Analog front end design, Analog to digital converters, Analog filters, Phase locked loops, Low-drop out regulators, Voltage reference generators and DC-DC Converters.

PUBLICATIONS

Number of Journals : 5
Number of Conferences : 5