

DESIGN AND DEVELOPMENT OF DUAL-INPUT DC - DC CONVERTER BASED HYBRID POWER SUPPLY SYSTEM FOR TELECOM LOAD

Thesis

Submitted in partial fulfillment of the requirements for the degree of

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by

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JULY 2023

DECLARATION

by the Ph.D. Research Scholar

I hereby declare that the Research Thesis entitled “**Design and Development of Dual-Input DC-DC Converter Based Hybrid Power Supply System for Telecom Load**” which is being submitted to the **National Institute of Technology Karnataka, Surathkal** in partial fulfillment of the requirement for the award of the Degree of **Doctor of Philosophy** in **Department of Electrical and Electronics Engineering** is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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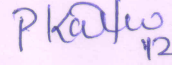
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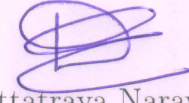
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CERTIFICATE

This is to *certify* that the Research Thesis entitled “**Design and Development of Dual-Input DC-DC Converter Based Hybrid Power Supply System for Telecom Load**” submitted by **Kiran R** (Register Number: 177109EE006) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

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Abstract

Telecommunications has become an imperative part of our life day-to-day activities from education to business. Power supply reliability is a critical challenge for telecommunication industries due to the deteriorating of fossil fuels with rising power demand. In most cases, telecom towers rely on diesel generators as a basis of power generation, which emits pollutants and is rather expensive. Due to climatic conditions and decreasing cost of solar PV panels, combination with biomass power, this technology could be used to provide clean electricity to various remote locations telecom load, where grid is not available. The proposed system will satisfy to afford reliable power supply for telecom load by completely eliminating the grid and diesel generators. This study emphasis on interactive based hybrid power supply solution for telecom load. An appropriate utilization and management of the PV/Biomass/Battery energy sources aids in greater reliability and enhanced efficiency of the system. Consequently, a literature review pertaining to multi-input converter topologies, Bidirectional DC-DC converter and voltage regulation technique have been presented.

Therefore, research in this thesis focuses on integrating energy systems suitable for telecom load use with sustainable power generation technologies, such as biomass power and photovoltaics. Among the research areas addressed in this perspective are dual-input DC-DC converter configurations, modelling and control strategy of the converter topologies, means for storing energy, Bidirectional DC-DC converter and voltage regulation technique. The multiport system structure is proposed as a means of integrating primary sources and energy storage. An integrated power conversion is possible by utilizing only one power processing stage in comparison to the conventional structure that utilizes multiple converters. Power conversion for a hybrid power source is integrated using a single power stage to interface multiple power inputs. In contrast with the conventional techniques that utilises multi-input converters, this structure eliminates redundant power stages. Thus, this study focuses on development of dual-input converter for providing power supply to meet the requirement of telecom load. The implementation has been concentrated

on developing a dual-input converter topology with charging the battery. Three converter topologies were realized. The first converter topology is modular dual-input full-bridge DC-DC step-down converter, in which both the output of the secondary rectifier are connected in parallel structure. The converter provides power supply to both telecom load and simultaneously charge the battery. Second converter is modified modular dual-input Full-Bridge step-up DC-DC converter. The converter has two individual input modules with three-leg semi active rectifier connected in parallel at secondary side for achieving constant voltage across the load with reduced circulating power. Further, third converter is modular dual-input half-bridge DC-DC converter. The presented converter has two individual input modules with three-leg active converter connected in parallel at secondary side. Further, a bidirectional buck-boost converter with only two active switches to charge and discharge the battery has been investigated in this research. The presented topologies results in an advantage of having compact structure with reduced number of components. The complete design and steady state analysis of the converters have been investigated.

There have been several improvements for the presented converter topologies aimed at zero voltage switching, reduced current stress, and greater efficiency in order to take into account the specific operating characteristics of the renewable energy sources with energy storage devices. The developed converter configurations have been tested with laboratory prototypes. The performance of the converters was investigated for a closed-loop control implemented with FPGA based digital controller. The power flow in the system is proved to be controllable. A significant enhancement in the efficiency when using the zero voltage switching and voltage power balance control method is witnessed. Further, telecom load functions in a pulsed-power manner intermittently. Moreover, the power consumption will be determined by signal traffic. The major task during pulsed power operation, is to maintain the regulated voltage across DC load terminals. Hence, in this study, Type II compensator is developed to maintain the constant load voltage with reckless response time. The stability investigation of the system with Type II compensator is evaluated by utilising the MATLAB/Simulink tool.

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List of Abbreviations

BMS	Battery Management System
BTS	Base Transceiver Station
CAPEX	Capital Expenditure
CUF	Capacity Utilization Factor
CV_b	Calorific Value of the Biomass
C_o	Output Capacitor
C1, C2	Input Capacitors of Module 1
C3, C4	Input Capacitors of Module 2
C_{r1}, C_{r2}	Resonant Capacitor Across Switches S1 and S2
C_o	Output Capacitor
DI-HBC	Dual-Input Half Bridge DC-DC Step-up Converter
D_{13}	Phase Shift Between Module 1 and Secondary Three Leg Converter
D_{23}	Phase Shift Between Module 2 and Secondary Three Leg Converter
DGs	Diesel Generators
DOD	Depth of Discharge
DI-HBC	Dual-Input Half-bridge DC-DC Step-up converter
ESS	Energy storage system
EV	Electrical Vehicle
FBR	Full-Bridge Rectifier
GMPCS	Global communication by satellite
HFT	High frequency transformer
HFT_1	High Frequency Transformer 1
HFT_2	High Frequency Transformer 2
I_{ph}	Photo Current Generated from the Solar Insolation
I_d	Diode Reverse Saturation Current
I_{pv}	Currents of PV Cell
I_b	Battery Current
I_{LB}	Current Across Inductor
i_{p1}	Primary Current of HFT_1
i_{p2}	Primary Current of HFT_2
i_{s1}	Secondary Current of HFT_1
i_{s2}	Secondary Current of HFT_2

I_o	Output Current,
I_{Lb}	Current Across Inductor During Charging of Battery
L_{r1}	Leakage inductance of HFT_1
L_{r2}	Leakage inductance of HFT_2
L_{p1}	Primary inductance of HFT_1
L_{p2}	Primary inductance of HFT_2
MIC	Multi-Input Converter
MPC	Multi-Port Converter
OPEX	Operational Expenditure
M_b	Total Biomass Accessible for Generation of Power
n	Turns ratio
PV	Photovoltaic
PHEV	Plug-in Hybrid Electric Vehicles
V_b	Battery voltage
PWM	Pulse Width Modulation
RESs	Renewable Energy Sources
RUL	Remaining useful life
R_l	Load
R_s	Leakage Resistance
R_p	Leakage Resistance
TRX	Transceivers
TLC	Three leg converter
VOC	Voltage Controlled Oscillator
V_{pv}	Voltage of PV Cell
V_{Lr}	Voltage Across Inductor
V_o	Output Voltage
V_{in1}	Input Voltage of Source1
V_{in2}	Input Voltage of Source 2
v_{p1}	Primary Input voltage of HFT_1
v_{p2}	Primary input voltage of HFT_2
v_{s1}	Secondary output voltage of HFT_1
v_{s2}	Secondary output voltage of HFT_2
V_{Lb}	Voltage across inductor during charging of battery
ZVS	Zero Voltage Switching

Chapter 1

INTRODUCTION

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1.1 GENERAL

The current chapter presents an introduction to the thesis, including research background, renewable energy sources (RESs), conventional architectures of telecom load, multi-input and bidirectional converters. At the end, the research motivation and organization of the thesis are incorporated.

1.2 RESEARCH BACKGROUND

The telecommunication industry is one of the major sectors that has witnessed rapid growth in cellular, radio paging, value added services, internet and global communication by satellite (GMPCS) services. In addition to playing a vital role in our everyday lives, telecommunication networks connect the entire world, enabling us to conduct business worldwide. In recent years, telecommunications have become such an integral part of modern life that it would be impossible to live without them. The power utility companies in developing countries are unable to meet the demand for reliable and quality power due to shrinking coal reserves and deprived infrastructure. There is a huge dependence of the energy on many conventional energy sources. But these energy sources lead to the increased greenhouse gas emissions and are hazardous to environment by creating air pollution. Beside the antagonistic issue of global warming, there is a necessity for a reduction in the burning of hydrocarbons to accomplish sufficient air quality. The development of efficient, clean and environmental friendly distributed power generation is becoming increasingly important in today's era.

The RESs are the most attractive substitute for non-renewable energy sources that are exhaustible and have a contrary influence on the environment. RESs like solar, biomass, wind, hydro and energy conversion technologies such as fuel cells are potential energy sources for providing efficient, clean and environmental friendly electrical power.

The power supply equipment requisite for the telecom network is accommodated by BTS. Normally, telecom loads are categorized into three clusters based on their power consumption levels (Liu et al., 2013). It is estimated that a telecom station with a small power rating consumes 400 to 1000 watts, a medium power rating station consumes 1000 to 2000 watts, and a super macro (high power rating) station consumes over 2000 watts. Electric grid is generally used to power these telecom loads, that is

the conventional energy derived from fossil fuels.

Rural areas lack reliable or uniform electrical grid power, which makes telecom towers more unlikely to be located there. As a result, it can be concluded that the telecom industry's greatest challenge today is supplying continuous and uninterrupted power to remote and rural telecom loads. Diesel Generators (DGs) are the chief source for power generation in these regions. As a result of maintenance, fuel requirements, and fuel transportation, these DGs have high long-term costs. Alternative sources of energy such as DG cost three times as much as grid power (Prema et al., 2014). As a result of unburned hydrocarbons, carbon monoxide, and nitrogen oxide, DG can cause noise and pollutant emissions that harm health and the environment. Burning one liter of diesel produces 2.7 kg of CO₂ (North, 2006)

As an alternative to fossil fuels, RESs are becoming increasingly popular for powering telecom loads. In a country like India, Biomass and solar energy are the renewable sources, which is available in abundant and reliable due to the geographical locations. The average intensity of solar radiation received is 20 MW/sq.km. The typical intensity of solar radiation expected is 20 MW/sq.km. The average solar insolation in India is 6 kWh/m²/day (Boyd et al., 2011). Therefore, it can be justified that, PV with biomass is cost effective and reliable preference for electrification in remote areas where affordable energy can be harnessed in a sustainable way with available natural resources. In conventional telecom loads where admittance to grid electricity is accessible, it utilises DG and batteries as backup sources in case of power outages. Moreover, to meet the requirement of entire telecom load, battery acts as a main source of power supply as energy price per unit of battery is very less as compared to DG per unit cost.

1.3 POWER SUPPLY CONFIGURATIONS FOR TELECOM LOAD

Fig. 1.1 illustrates the schematic of traditional power supply system of telecom load where grid power is accessible. Most of the time DG functions with 20% to 30% of its estimated load in the conventional system. This leads to more consumptions of fuel that results in higher carbon footprint. To eradicate this issue, (Liu et al., 2013) have proposed a new approach. Here, DG facilitates the power to both load as well as

battery simultaneously. The proposed approach results in enhancing efficiency of DG where it is able to supply power to load and battery, rather than only to load as in traditional system. Investigation of literature illustrates that the hybrid systems such as PV/Biomass/Battery, PV/DG and PV/Battery hybrid structures diminishes the use of diesel consumption and operative cost of the system for telecom loads where the access to grid supply is unavailable. (Yamegueu et al., 2011), (Ajan et al., 2003) have described experimental examination of PV/DG hybrid system, where PV and DG are evaluated to encounter peak load of the system, throughout sunlight times PV is organised to meet the requirement of the load, in the absence of PV, DG has to deliver the power to meet load. In this arrangement CAPEX and OPEX is reduced, however smooth power flow is a main task as power from PV source is indeterminate. The conventional configuration PV/wind/Battery used for standalone mode is shown in Fig.1.2 (Kaur et al., 2018). In countries like India where solar insolation is abundant and with the reduced PV panel price, it is substantial for the optimum design and effective utilization of PV/Battery configuration to diminish the utilization of DG consumption. Further, maximum of the PV/Battery based power supply system utilises the traditional gel based lead acid batteries as storage of energy that is unsafe to the environment (McKenna et al., 2013) and (Robinson, 2009). Additionally, it has reduced life span (i.e. 600 cycles) considering 80% Depth of Discharge (DOD) at standard test circumstances. So, it is essential to swap the battery for one and half year, if it is charged and discharged every day. This would results in surge in recurring cost. Very fewer emphasis has been put on new battery technologies in the circumstance of ESS in RES system.

Therefore, in this study dual-input converter based power supply for BTS will be studied. Moreover, this study investigates the bi-directional DC-DC converter topology for battery charging application. The block diagram of the PV/biomass/battery power supply system used for powering telecom load is shown in Fig. 1.3.

1.3.1 PV System

Photovoltaic (PV) cells are the fundamental blocks for the construction of PV power system. The incident sunlight on PV cell generates the charge carriers which produces the electric current. A single PV cell is very small and can produce typically 1-2 W of power. An assembly of PV cells are coupled in series to create a module which can

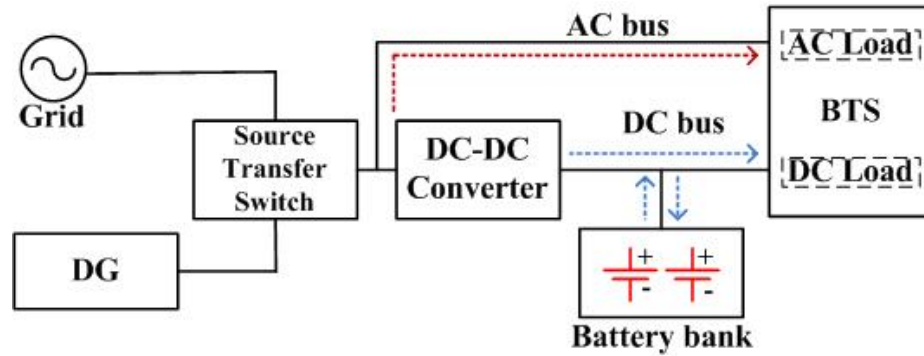


Figure 1.1: Conventional power supply scheme for telecom load in grid connected mode

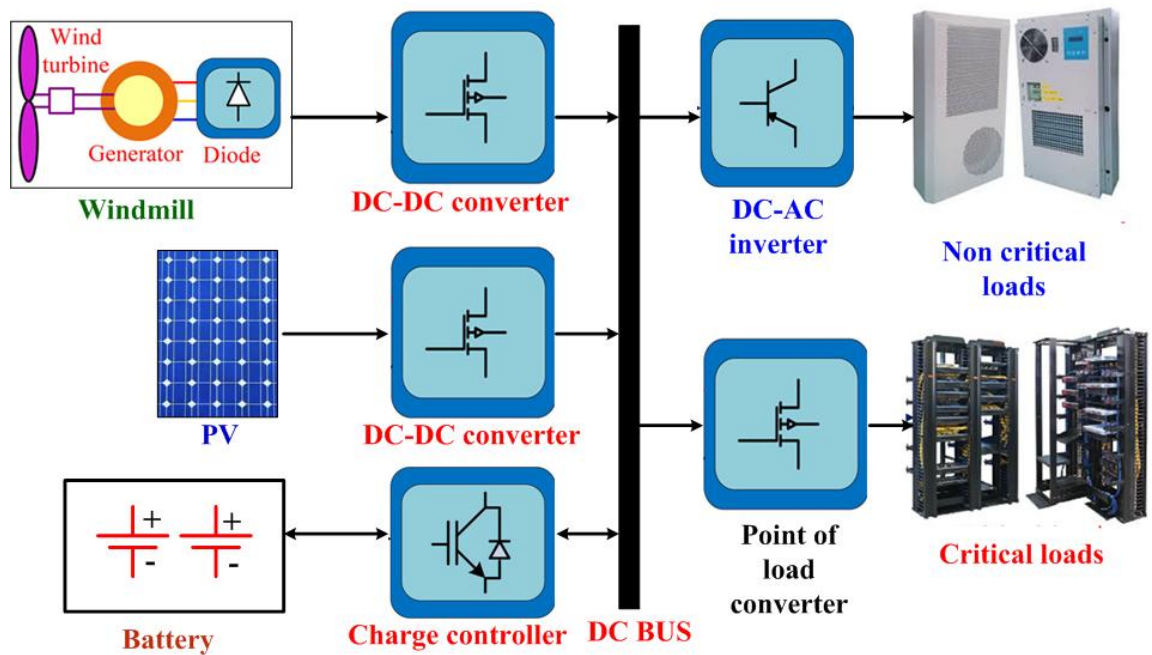


Figure 1.2: Conventional configuration of PV/wind/Battery based power supply system for telecom load

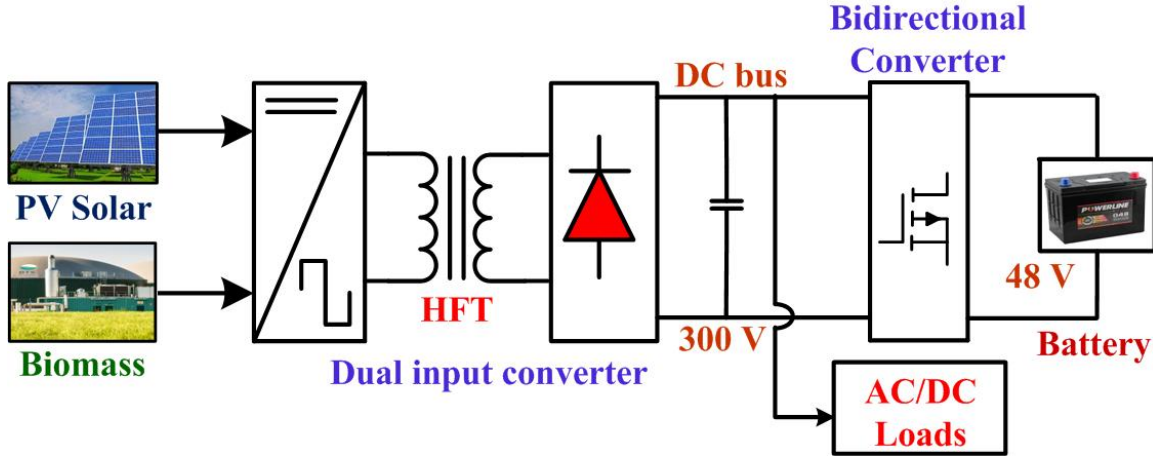


Figure 1.3: Schematic of the developed PV/Biomass/Battery based standalone mode system for telecom load

produce power in the range of a few hundred watts. Further, to enhance the power rating of the system PV modules are connected in series and/or parallel to form a PV array. The power generated by PV cell depends on solar insolation (irradiation) on its surface and operating temperature of the PV cell. Therefore, to examine the electrical features of PV cell and PV array in various operating conditions, mathematical model of a PV cell will be discussed in next section.

1.3.1.1 Mathematical Model of PV Cell

An electrical equivalent of PV cell is required to analyze the characteristics of PV cell for the modification in solar insolation and temperature conditions. However, there are various equivalent circuit models viz. single diode model (shown in Fig. 1.4 (a)), two diode model (shown in Fig. 1.4(b)) (Villalva et al., 2009). Amongst these, single diode model is the most popular and simple (Villalva et al., 2009). Single diode model of a PV cell is established by utilising the Schokley diode equation. The electrical equivalent circuit of PV cell considers the solar insolation and PV cell operating temperature as the inputs. In this study single diode model of a PV cell will be studied. The equation for the PV current is described as,

$$I_{pv} = I_{ph} - I_d - \frac{V_{pv} + I_{pv}R_s}{R_p} \quad (1.1)$$

where, I_{ph} is the photo current produced from the solar insolation, I_d is the diode reverse saturation current, R_s and R_p are resistance because of material interactions and leakage resistance correspondingly and V_{pv} and I_{pv} are voltage and currents of PV cell correspondingly. The equation for I_d is described as follows

$$I_d = I_o \left[\exp \left(\frac{V_{pv} + I_{pv} R_s}{AV_t} \right) \right] \quad (1.2)$$

where, I_o is the reverse saturation current of the diode, V_t is the thermal voltage of the diode and A is the ideality factor of the diode. To simplify the computation ideality factor (A) is considered as 1. The photo current (I_{ph}) is expressed as follows,

$$I_{ph} = I_{scSTC} \left[\frac{R_s + R_p}{R_p} + K_i \Delta T \right] \frac{G}{G_{STC}} \quad (1.3)$$

where, I_{scSTC} is the short circuit current of PV cell at STC condition,

$$(\Delta T) = T_{cell} - T_{STC} (T_{STC} = 25C) \quad (1.4)$$

G is the solar insolation (W/m^2) falling on PV cell and G_{STC} is the insolation at STC ($1000W/m^2$) The constant K_i is the short circuit current coefficient in $mA/^\circ K$ which will be provided by the manufacturer. The diode saturation current with variation in temperature is given by,

$$I_o = I_{scSTC} + \frac{K_i \Delta T}{\left(\exp \left(V_{ocSTC} + \frac{K_v \Delta T}{AV_t} \right) \right)} - 1 \quad (1.5)$$

K_v is the open circuit voltage coefficient in $mV/^\circ K$ provided in the data sheet.

V_{ocSTC} is the open circuit voltage of PV cell at STC. The temperature dependent thermal voltage of the diode is expressed as follows,

$$V_t = \frac{KT}{q} \quad (1.6)$$

where K is boltzman's constant (1.238×10^{-23}) J/K) T is the ambient temperature in K and q is the electron charge (1.69×10^{19}) C. Therefore, a PV module can be

modeled by connecting n_s series cells and n_p parallel cells using the equation (1.7).

$$I_{pv} = n_p I_{ph} - n_p I_o \exp\left(\frac{n_p V_{pv} + n_s I_{pv} R_s}{n_s n_p A V_t}\right) - 1 - \left(\frac{n_p V_{pv} + n_s I_{pv} R_s}{n_s n_p R_p n_p / n_s}\right) \quad (1.7)$$

1.3.1.2 Electrical Characteristics of a PV Array

As discussed in section 1.3.1.1 the power generated from the PV cell is dependent on solar irradiance and surface temperature of the cell. The photo-current I_{ph} generated from the solar cell is directly proportional to the solar insolation. Variation in insolation due to cloud or earth movement will change the amount of power generated from the PV cell. The variation of I-V and P-V characteristics of a rated PV array with change in solar irradiance is shown in Figs. 1.4 - 1.6. Variation in temperature has an effect on V_{oc} and I_{sc} of the solar cell. Fig. 1.6 shows I-V characteristics for various temperature conditions. From the Figs. 1.4- 1.6, it is clear that PV array produces a single maximum power point (MPP) on its power-voltage (P-V) curve. Therefore, a MPPT algorithm is required to operate the PV system at its MPP. To date, many researchers have developed various MPPT techniques. These techniques are classified into two categories. Indirect method: MPP is projected from numerous constraints

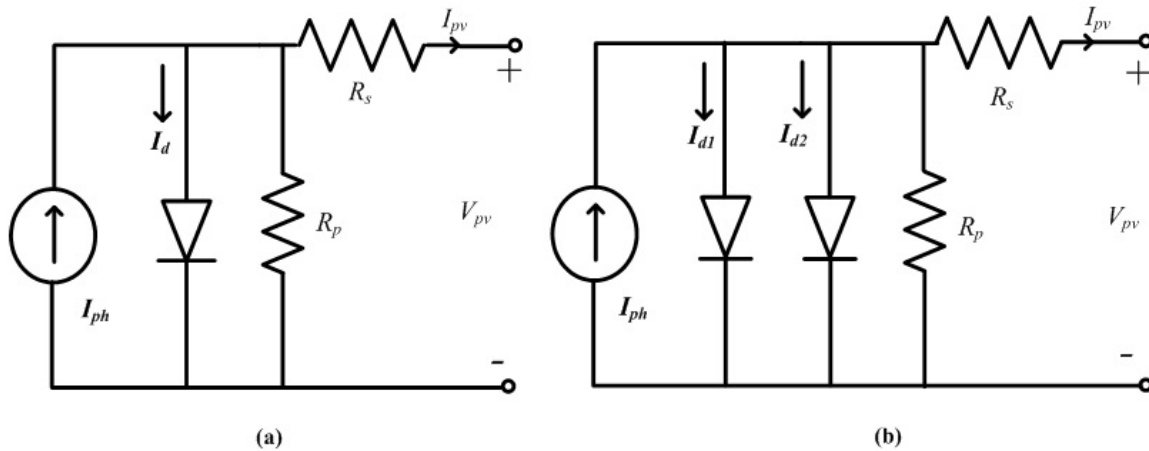


Figure 1.4: (a) Single diode model of a PV cell, (b) Two diode model of a PV cell.

such as voltage, current, irradiance temperature, by utilising experimental data or using scientific expression. This valuation is accepted for particular PV system. Some of these approaches are:

- Curve fitting method

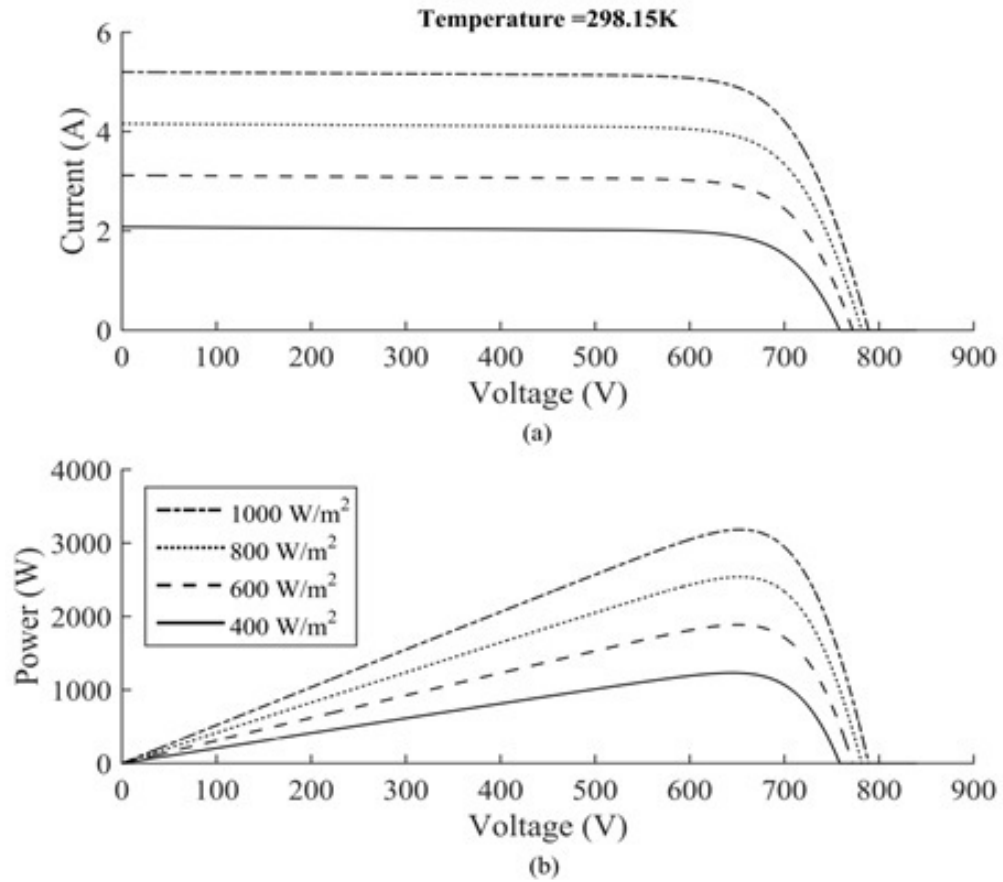


Figure 1.5: Electrical characteristics of PV array for different uniform insolation conditions (a) I-V characteristics (b) P-V characteristics

- Lookup table method
- Fractional OC method
- Fractional SC method

Direct methods: This method does not necessitate any preceding acquaintance about PV panel and are self-governing of temperature, insolation or deprivation levels. They necessitate measurement of PV voltage or current to track MPP.

Some of these techniques are:

- Perturb and Observe (P and O) /Hill climbing Method
- Incremental Conductance Method (INC)

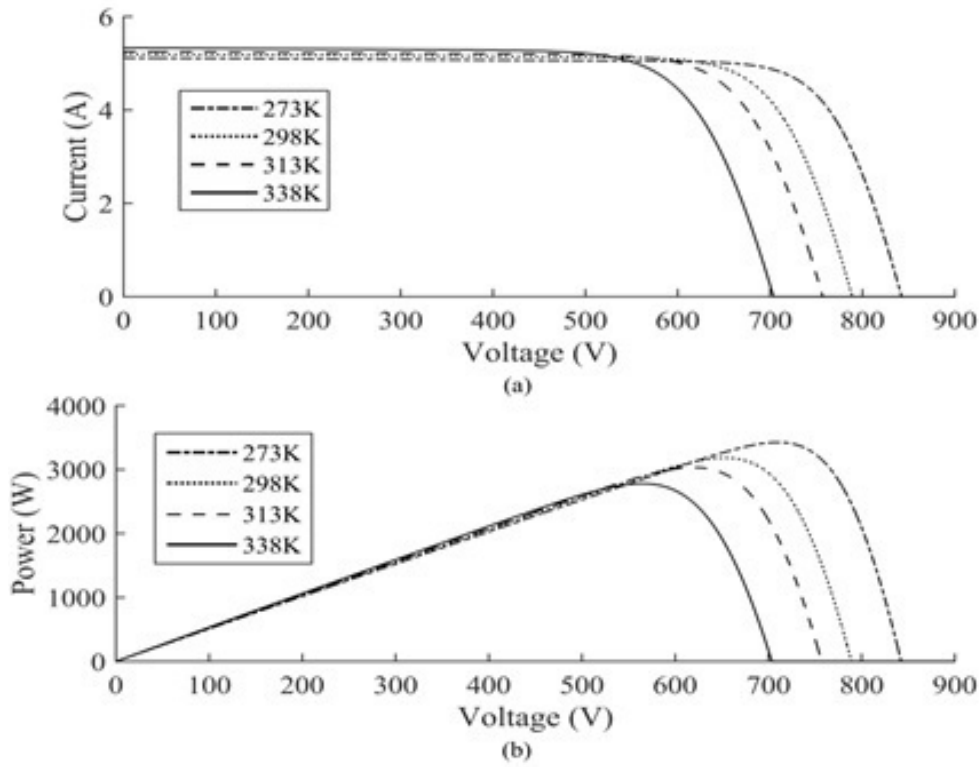


Figure 1.6: (a) Single diode model of a PV cell, (b) Two diode model of a PV cell.

- Fuzzy Logic Control
- Sliding Mode Control Method

Among these techniques, the P&O and the INC algorithms are the most popular. Both the methods works on the principle of hill climbing (HC), which makes the operating point to move in the direction in which maximum power is available. HC methods are most popular due to their excellent performance and less complex in implementation. Other methods such as fractional open circuit and fractional short circuit methods are not effective as they work on approximated assumptions.

1.3.2 Biomass

Fig. 1.7 illustrates the architecture of power generation from biomass power plant. Biomass gasification technology includes partial combustion of bio residues under controlled air supply that process gas fuel. Produced gas is fed as input for combus-

tion engine that will generate electricity in form of AC. Capacity utilization factor (CUF) decides the annual electricity, E_{annual} , of a particular biogas system P_b . The expression (1.8) is used to calculate CUF

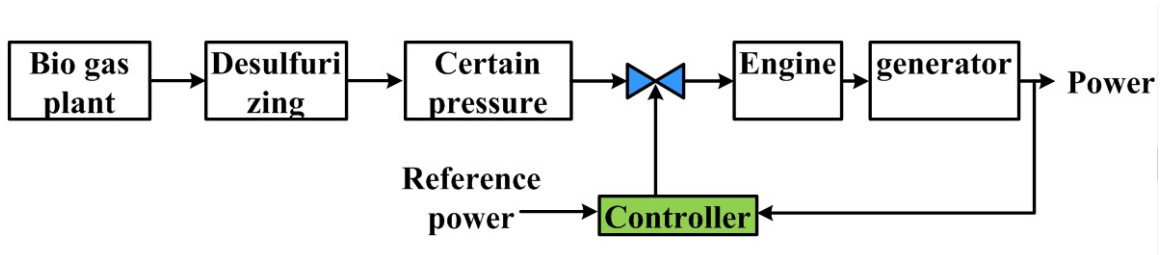


Figure 1.7: Architecture of power generation from bio mass power plant

$$E_{annual} = 8760P_b(CUF) \quad (1.8)$$

The maximum rating of biogas can be calculated from equation (1.9)

$$P_b = 1000M_bCV_b\left(\frac{n_b}{365}\right)8608t_b \quad (1.9)$$

Where M_b is total biomass accessible for generation of power and is efficiency of the plant, t_b is number of hours operating of bio mass system and CV_b is calorific value of the biomass available.

1.3.3 Multi-Input Converters

With environmental concerns and advancing technology, renewable energies are becoming increasingly popular due to the fact that manufacturing costs are rapidly declining and the technology is becoming more sophisticated. In spite of this, the intermittent nature of RESs and the impulsive nature of load demand create a main challenge for the extensive advancement of these RESs. Hence, power converters with ESS are generally utilised to transform the output power from the RESs to meet the requirement of load, to progress the dynamic and steady-state features of the green generation systems. Moreover, it is utilised for MPPT control, and to integrate the battery system with RESs to deal with the challenge of the irregular nature of the RESs and the impulsiveness of the demand of load.

Conventionally, the RESs are linked to the load through a conventional DC-DC

topologies and further, the ESS is associated to either the input or the output port of the conventional DC-DC topology through a bi-directional DC-DC converter configuration for charging and discharging of battery. The main drawback of these traditional clarifications is the reduced efficiency due to the employment of the supplementary converter for the battery system. Moreover, the multi-stage design might consequence in increased size, small power density, and comparatively high cost.

A MIC topology is a solution to fulfil the necessities of some applications that necessitate the integration of numerous diverse types of input RESs such as fuel cells, wind mills, biomass and PV. A single-stage converter of this type can be utilised to provide the essential power to the load.

1.3.4 Energy Storage System and Li-Ion Battery Technologies

Rechargeable batteries play a vital part in the field of hybrid EVs, distributed energy storage and emergency lighting systems. The knowledge of battery aging mechanism will helps to replace the battery at right time to improve the consistency of the system also it ensures the uninterrupted operation of the system. Battery aging is influenced by factors such as excess charge, yawning discharge, ambient temperature, and discharge rate. RUL is a measurement that defines the condition of the battery and its enactment associated with the new battery. By knowing the health of the battery in advance, it helps us to configure the correct time to swap the battery. Rapid advancements in the technology of Lithium ion (Li-Ion) batteries resulted in high specific power and energy density ((Goud et al., 2021)).

Consequently, Li-Ion batteries have developed customary in EVs and RESs. Moreover, these batteries have sophisticated cycle lifespan than any other rechargeable batteries, charge preservation of Li-Ion batteries is excellent and the batteries can be cycled over a thousand times. Preliminary price of Li-Ion is expensive compared with the other batteries. In spite of this, Li-Ion batteries are becoming most popular and standard. There are several other Li-Ion chemistries are available like Lithium Cobalt Oxide (LiCoO₂), Lithium Iron Phosphate (LiFePO₄ or LFP), Lithium Nickel Cobalt Aluminium Oxide (LiNiCoAlO₂ or NCA).

1.3.5 Telecom Load

Telecom base station is composed with a tower for mounting antennas, TRX, signal processors, electrical power converters, power amplifiers and energy storage elements. BTS stations are further classified into categories such as indoor type and outdoor type. Most of the BTS stations in India are indoor type, which consists of 3 to 12 TRXs along with control circuits and antennas. The largest power consuming element in BTS is power amplifier which consumes about 65 % of total consumption (Mangu et al., 2011). Generally, DC loads in BTS operates at voltage range of (43 - 60V) but in most of the applications BTS loads are designed for 48V.

1.4 RESEARCH MOTIVATION

With speedy progress, India has seen a flow in telecommunication all across the countryside comprising inaccessible and rural areas. In the present era, telecommunication has become an imperative part of our day-to-day life activities from commercial to education to infotainment. Telecom providers need regular and reliable power supply for BTS in order to provide effective service for the people. Telecom providers in India are utilizing grid as main source of power supply and diesel generators as standby that is uneconomical due to its huge cost and high maintenance (Mishra et al., 2018). Presently, more importance is preferred to DGs to power these exchanges in this segment, specifically in countryside areas. Telecom providers in India are facing tough challenge to ensure uninterrupted and regular power supply for base BTS. Because of high cost, finite availability, excess depletion of fossil fuels and environmental interest with nonrenewable energy sources adding with advancement in power electronics and renewable energy sources are attracting greater attention in the present days. So, there is a need for providing regular power supply to telecom load by utilizing renewable energy sources in standalone mode condition.

Most challenging part in the dual-input converter is designing of the converter topology to achieve high efficiency. The proposed dual-input converter in the literature have limitations of isolation, more number of switches, low power rating and high voltage application with complex control strategy. Further, minimising circulating power between different sources plays a vital role in designing of converter for achieving higher efficiency. A proper control strategy for power sharing and maintenance

of regulated DC output voltage at load end has to be achieved. Further, an appropriate control strategy is required for proper voltage regulation and voltage charging of the battery.

1.5 THESIS ORGANIZATION

The research study has been concentrated on design and development of interactive based hybrid power supply system for telecom load. The study emphasis on design and development of various dual-input converter topologies for telecom load. Further, a bi-directional DC-DC converter for charging battery and discharging battery has been presented. A tight voltage regulation for the buck converter has been discussed in the thesis.

The whole thesis is organized into six chapters, as follows:

- Chapter 1:** This chapter outlines the brief introduction to the telecom load, different power supply configurations for telecom load, limitations of conventional power supply configurations and introduction to the multi-port converter based power supply system by utilizing renewable energy sources.
- Chapter 2:** State-of-the-art related to dual-input converter topologies, Bi-directional DC-DC converter topologies, voltage regulation for telecom load, identified research gaps and research objectives are discussed in this chapter.
- Chapter 3:** This chapter presents an isolated voltage source fed modular dual-input DC-DC converter with battery storage system for telecom load application. Complete design of the developed converter with FPGA based digital control strategy have been presented in this chapter. The simulation analysis of the converter has been executed utilizing MATLAB Simulink environment. A laboratory prototype has been developed and tested for 1.1 kW power. Further, a modified modular dual-input DC-DC step-up converter that is suitable for telecom load applications is presented in this chapter. The modified dual-input DC-DC converter has two individual input modules with three-leg semi active rectifier connected in parallel at secondary side for achieving constant voltage across the load with reduced circulating power. This results in an advantage of having compact structure with reduced number of components. The complete design and steady

state analysis of the converter has been analysed in detail. FPGA based digital control strategy have been investigated for the developed converter. A scaled down laboratory prototype of 1 kW has been developed and the robustness of the converter is validated by extensive test results under variable input voltage and load conditions. Further, a bidirectional DC-DC converter for battery charging and discharge condition has been developed. A laboratory prototype has been conducted for the bi-directional DC-DC converter topology to achieve both buck and boost operation during charging of battery in CC/CV mode and boost operation during discharge mode whenever required by load.

Chapter 4: This chapter addresses a dual-input half-bridge DC-DC converter for proper utilization of renewable energy sources. The converter topology includes two different variable sources to examine the power distribution in each module, two high-frequency transformers and a three leg converter at secondary. The three leg converter is connected in parallel structure to gain reduced circulating power between input modules. This consequences in obtaining a compact design with minimum number of switches. Complete steady state analysis, control strategy of the converter have been analyzed in detail. Digital closed loop control has been implemented using FPGA controller to minimize the complexity of the control strategy. A laboratory prototype has been developed to justify the feasible operation of the converter.

Chapter 5: For the safe operation of DC loads of BTS, it is required to maintain 48V constant DC supply at the load terminals. However, with the signal traffic load current varies and which effects the load voltage regulation. Therefore, in this chapter a voltage regulation technique is developed and tested in MATLAB/Simulink platform. Moreover, its performance characteristics are discussed in this chapter.

Chapter 6: This chapter concludes the contributions of research work carried out and discusses the possible future scopes.

Chapter 2

LITERATURE REVIEW

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2.1 GENERAL

Since the present study deals with the integration of renewable energy sources (RESs) to feed the telecom load by utilising multi-input converter topology and bidirectional converter to charge and discharge the battery, state-of-the-art related to multi-input converter and bi-directional converter topology are discussed in this chapter.

RESs are progressively being utilised due to the ecological concern and developments in technology and briskly dwindling engineering price. Though, the irregular nature of the RESs and the impulsiveness of the load mandate harvest a tough task for the extensive advancement of these clean RESs. Hence, power electronic converters with ESS are customarily utilised to transform the output power from the PV source to meet the requirement of the load mandate and to enhance the dynamic and steady-state features of the eco-friendly systems. Further, it aids to facilitate MPPT control, and to integrate the ESS to contract with the task of the irregular nature of the RESs and the impulsiveness of the load demand. Conventionally, the RESs are associated to the load through a traditional DC-DC converter and then the ESS is connected through a bidirectional DC-DC topology for charging and discharging of battery. The main hindrance of these conventional resolution is the reduced efficiency because of the utilization of the supplementary converter configurations for the ESS. Correspondingly, the multi-stage structure may consequence in amplified size, reduced power density, and comparatively increase in price. A multi-input converter (MIC) is an answer to gratify the necessities of particular applications that entail the integration of various RESs such as fuel cells, wind mills, biomass and PV. This type of topology can be utilised to afford the required power to meet the load demand by utilising a single stage method.

2.2 MULTI-INPUT CONVERTER TOPOLOGIES

Traditional approach involves the integration of multiple sources of energy by a single converter that is connected to a single DC bus (Chen et al., 2015), (Lin et al., 2011), (Hirose and Matsuo, 2012). Yet these converters are not utilized in an effective way as powering stages are more and lead in more losses of the system. A significant number of literatures exist on wind/solar based hybrid system for power generation. Since both the sources are variable it's challenging to control both the

renewable sources. There are very fewer configurations are made to optimize the circuit configuration with reliable, high efficient and low price. Integrated PV-wind energy systems are presented in (Daniel and AmmasaiGounden, 2004), (Wandhare and Agarwal, 2015) . It is observed interesting from studies that combination of PV with Biomass power is cost-effective and reliable preference for electrification in remote areas where affordable energy can be harnessed in a sustainable way with available natural resources (Singh and Kaushik, 2016), (Lai and McCulloch, 2017), The above stated advantage has motivated to research on integration of PV-biomass and battery system. In order to meet the demand of load and to progress the power from different renewable energy sources in a hybrid system with reduced number of components, researchers have proposed various DC-DC converters.

A MIC is a solution to satisfy the necessities of particular applications that entail the integration of various RESs such as fuel cells, wind mills, biomass and PV. For the integration of different energy sources, a MIC can be preferred over conventional power electronic converters that are connected separately from sources to DC bus. The main advantage of these MIC is low number of components that results in reduced cost and high power density compared to conventional converters that are connected individually (Bhattacharjee et al., 2019) , (Reddi et al., 2018). Mainly, MICs can be divided into three different classes as completely isolated, partially isolated, and non-isolated (Wu et al., 2015). Among these partially isolated and non-isolated MICs provides a compact design, minimum cost, greater power consistency, and high efficiency (Zhang et al., 2015), (Debnath and Chatterjee, 2015). Though, in these topologies it's difficult to achieve zero voltage switching (ZVS) that leads in more losses of the system with reduced efficiency.

2.2.1 Classification of Multi-Input Converters

In the traditional approach of integrating multiple RESs, there exists DC bus with high/low voltage. Individual DC-DC conversion stages are engaged for separate RESs. These topologies are organised at a common DC bus. Further, individual controllers are facilitated for the same. So, to integrate more than one RESs, such as PV, wind, biomass, fuel cell and to achieve an appropriate voltage regulation various MICs are proposed in the literature. A MIC constitutes of more than one input as source. The energy link is further connected to separate DC-DC converter topology as illustrated

in Fig. 2.1. Table 2.1 provides a compressive comparison of conventional converter with MICs.

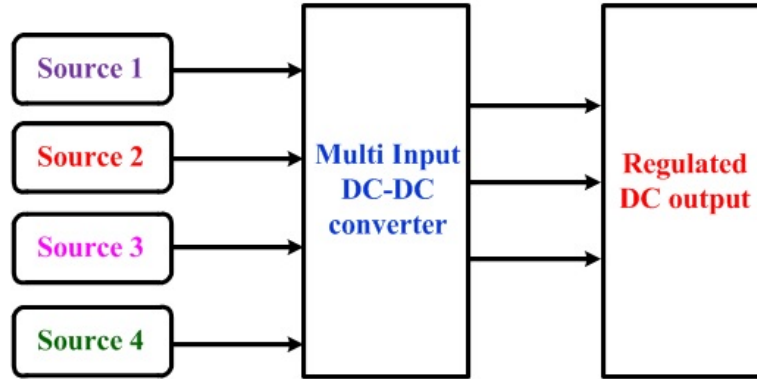


Figure 2.1: Basic block diagram of multi-input converter for connecting different RESs to achieve regulated output

In the conservative architecture, there customarily occurs a joint high or low voltage DC bus integrating numerous RESs. Distinct DC-DC transformation phases are regularly utilised for distinct sources. Those topologies are electrically connected together at the DC bus and are generally has separate control scheme for distinct converter topology.

Table 2.1: Comparison on conventioanl multi-input convert with integrating multi input converter

Comparision	Conventional DC-DC Converter	Multi-input converter
Number of devices	More	Less
Control scheme	Separate	Centralized control
Conversion stages	More	Less
Complexity	Structure complex	Control complex
Efficiency	Less	High

The key operational concern of a hybrid energy system is the location of the ESS. A benefit of this topology is that it is conceivable to elect an optimum voltage for the ESS. Conventionally, MICs are utilised to afford interfaces for power inputs of the system. In standard, any basic power converter configuration can be utilised to design for a hybrid power system. The MIC has a benefit above the traditional approach.

It is illustrated that the conversion phases in the traditional structure can be minimised by identifying idleness in the power processing. In a MIC, it is conceivable

to segment the system resources (i.e., conversion devices) and to eradicate the idleness. This aids in enhancement of the system efficiency. Further, the efficiency can be enhanced by eradicating redundant power stages and their related losses. A MIC is predominantly interesting for on-site, low power, suburban power generation systems where energy is to be harvested from a diversity of RESs in combination and a means of ESS available. Multi-input DC-DC converters are broadly categorised as isolated and non- isolated topologies as shown in Fig. 2.2.

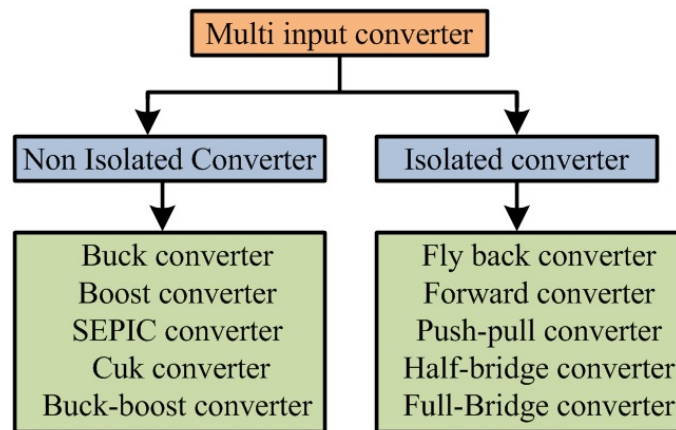


Figure 2.2: Classification of multi-input converter

2.2.2 Dual-Input Non-Isolated Topologies

Multi input based non-isolated topologies (Athikkal et al., 2019), (Faraji and Farzanehfar, 2018) have been proposed to meet the load requirement. But, these topologies suffer from ZVS and there will be no isolation between source and load. This leads to more losses in the system and efficiency will be reduced. A Modular dual-input DC-DC converter for High/low voltage sources are presented in literature (Ding et al., 2013), (Chen et al., 2006b). The advantage of the proposed topology is that, it can be operated in both series and parallel configuration with an appropriate switching and control scheme. Further, the converter can be operated to extract power from individual source or simultaneously.

Yet, the topology has a disadvantage of limited voltage gain and suffers from hard switching. In (Li et al., 2017), A multi-input single output (MISO) bridge-type step-down topology is developed for PV applications. The advantage of the proposed topology is, it facilitate to charge the battery under light or no-load conditions.

Though, it has drawback of more number of extra switches that are utilised for attaining a flexible control system which is projected for plug-in hybrid electric vehicles (PHEVs) (Onar and Khaligh, 2011).

In this method coupled inductor is utilised as a substitute of two distinct inductors. However, coupled inductor is bulky in size. (Varesi et al., 2017b), has presented an enhanced MISO converter topology. The main advantage of the proposed topology is, it can be operated in step-down, step-up, and buck-boost mode of operation that facilitates the bidirectional operation with charging of battery simultaneously. Conversely, it has drawback of more number of switches that leads to increased cost and significant switching losses.

A bidirectional MISO configuration is presented in literature (Akar et al., 2015). The proposed topology has an advantage of facilitating power sharing between input RESs with ESSs. The dynamic performance of the proposed topology has been tested in contrast to a variation in load by using the ECE15 drive cycle. However, the number of active and passive devices are higher as compared to bidirectional MIC.

A multi-input step-up converter topology is proposed (Zhou et al., 2012) to achieve high voltage gain for generating power from PV. The converter topology has a special features such as low stresses on the switching devices and facilitate to achieve high output voltage low with low functioning duty cycle. However, the converter topology suffers from large number of active and passive device, resulting in undesirable price and likewise, enhance the size of the topology. Various MISO converter topologies are being design and developed for application of hybridizing the RESs with the potential of high voltage gain, ESS, and bidirectional for RESs, grid, and EVs applications in (Marchesoni and Vacca, 2007), (Deihimi et al., 2017), (Haghighian et al., 2017), (Rezaee and Farjah, 2014), (Banaei et al., 2014a), correspondingly. Further, multiple RESs can be connected in the input side. The control scheme for regulating output voltage is also complex. Literature (Marchesoni and Vacca, 2007) proposes a multi-input converter topology. The converter topology suffers from high number of passive elements and active devices (Deihimi et al., 2017), (Haghighian et al., 2017), (Rezaee and Farjah, 2014), correspondingly. This results in increased cost and size of the converter topology will be large in size. Three switches leg based MISO (Azizi et al., 2016a) converter topology is proposed with potential features. The converter topology evade terminals floating and DC bus shoot through, when operating with both switches of the same leg are turned ON. Further, the converter leg has two ter-

minals that can be suitable for multi-port converter applications. However, because of step-up and step-down operation of the DC-DC converters modulation index value is restricted. Furthermore, the topology has more number of devices and complex control strategy. Literature (Hou et al., 2015) introduces a MISO step-up converter topology. The proposed topology is designed and developed based on switched-diode-capacitor for voltage accumulator applications. A MISO boost converter is presented in literature (Varesi et al., 2017a). Realization of high gain dual-input step-up configuration is presented in literature (Varesi et al., 2017a). The voltage gain of the proposed topology is depending on charging in parallel operation and similarly, discharges in series by utilising an appropriate transition of the main switch. A MISO bi-directional converter is presented in literature (Varesi et al., 2017a). The advantage of the proposed topology is, it has reduced voltage stress on the active switches and facilitates high voltage gain. Though, for n inputs the converter topology desires $n+1$ inductor, $n+1$ capacitor, $n+1$ switch, and $n+1$ diode that results in high cost and increased size with complex control scheme for power transform. A high step-up MISO converter topology is presented in literature (Tomar and Mishra, 2016) for PV water pumping applications. The proposed system facilitates to reduce mismatch phenomena and the effect of partial shading when PV modules are connected in series structure. Though, the topology suffers from more number of inductors and $n+3$ active switches for n - input systems. So, it results in system being complex. Many of the MICs are suffering from duty cycle limitations in PV applications that results in limits the utilization of RESs. Further, a wide range of duty cycle operation is not possible (Song and Kwasinski, 2009). This drawback can be overwhelmed by replacing the coupled inductor at the common output end. A MISO is proposed in literature (Yuan-mao and Cheng, 2013). The proposed topology is established based on a switched capacitor approach. The proposed technique aids in integrating the two different voltage sources and magnetic components are substituted by switched capacitors to attain the regulated output voltage. Further, it aids in minimising the price and size of the converter topology.

In order to integrate two different RESs time-sharing model is utilised (Dobbs and Chapman, 2003). The proposed topology has three power devices that significantly reduce the cost and power loss. The proposed technique has simple control strategy. However, the proposed topology suffers as output voltage is negative and bi-directional power flow will not be possible. A simple configuration of MISO converter

is proposed in literature (Thiyagarajan and Gokulavasan, 2014) . The proposed converter configuration has an advantage of sharing power flow in bidirectional way with high efficiency. Though, the output voltage will be negative and it necessitates supplementary switches in series along with the leading switches to evade the circulating currents between the RESs.

MISO buck-boost converter is presented in literature (Athikkal et al., 2017a) , it progresses the utilization of RESs as compared to the developed topology in literature (Dobbs and Chapman, 2003), (Thiyagarajan and Gokulavasan, 2014). Conversely, in the case of RESs $V_1 < V_2$, it may necessitate the supplementary active switches in series with individual input source for the suitable operation. A non-inverting MISO topology is proposed in literature (Khaligh et al., 2009). The proposed topology is able to achieve operation of step-up, step-down and buck-boost modes. Nevertheless, only one RESs is permissible to provide power supply at a particular time. Moreover, the proposed converter is extended with ESS and enhance the performance of the topology for EV applications with the integration of RES (Balaji et al., 2017). Correspondingly, a MISO bridge-type buck-boost converter topology is proposed in literature (Athikkal et al., 2017b). The proposed topology progresses the gain of the output voltage as compared with the proposed converter in literature (Khaligh et al., 2009). Moreover, the topology can perform in step-up, step-down and buck-boost mode of operation. Nevertheless, as active switches are in series with input RESs that leads to a surge in the cost of the converter.

In order to integrate various RESs a MISO converter topology is proposed (Kumar and Jain, 2013). The proposed topology can be operated for step-down and buck-boost modes. The proposed topology utilises an intermediate synchronization switching technique, which aids in enhancing the utilization of RESs and proper output voltage regulation is achieved. A multi-input buck-boost converter configuration is introduced in literature (Kanhav and Chaudhari, 2018), that has features of minimum part count that's aids in reducing size of the converter and complexity of converter. Though, the bidirectional operation is difficult to operate. A MISO converter is presented in literature (Vural, 2013) , for the hybridization of FC and ultra-capacitor (UC). The proposed configuration has an advantage of reduced reverse recovery losses and minimum stress on the device. Further, switching losses are minimum during discontinuous conduction mode (DCM) of operation. Additionally, the converter configuration is able to achieve reduced conduction losses with min-

imum ripple current during continuous conduction mode (CCM) of operation and core losses are minimised during CCM mode of operation. Conversely, it has large size coupled inductor and needs more number of switches. A bidirectional three port converter topology is proposed for ESS along with two unidirectional power ports. The unidirectional power modules are developed to interface the asymmetrical RESs (Nejabatkhah et al., 2011), (Ahrabi et al., 2016).

The topology is able to attain proper power management between RESs, ESS, and the load. However, the topology suffers from complex control strategy that results in complex system. In literature (Wu et al., 2012), an organized methodology is proposed for developing the various MISO and SIMO topologies. The advantage of the presented converter configuration is conversion of power from RESs to load will occur in single stage system that leads to high efficiency with minimum losses. Though, the topologies suffer from more number of devices which results in increase in cost and size of the topology. Three port boost converter is proposed in literature (Solero et al., 2005) that is verified for 60kW power for HEV applications. The proposed topology has gained a proper dynamic behaviour under different driving cycles. A dual input single output (DISO) converter configurations are introduced in literature (Sun et al., 2014), (Dhananjaya and Pattnaik, 2019). The proposed topology is able to operate in single input mode of operation even if other source is short circuited. Further, the converter topology is able to meet the load voltage with the support of the charging capacitor. However, fault tolerance is developed in single input failure condition and increase the part count.

Multi-input multi-output (MIMO) with a single inductor is proposed in literature (Behjati and Davoudi, 2011). The proposed topology is able to achieve two RES by utilising multiplexing concept by performing various voltage and current characteristics. Conversely, it necessitates $n+m+1$ switch for n inputs m outputs, and the outputs are associated in series. A MIMO topology is proposed in literature (Behjati and Davoudi, 2013). The proposed MIMO topology discusses on cross-regulation difficulties during CCM operation. In order to overcome the drawbacks of (Behjati and Davoudi, 2011) a model predictive control based MIMO converter is proposed in literature (Wang et al., 2016). The converter topology is able to diminish the problems associated with cross-regulation problems, reduce the voltage ripples, and able to maintain desired output voltages. Literature (H bajeti et.al) proposes a single-stage MIMO converter. The converter topology make use of single inductor, thereby

reducing size and overall price of the converter. However, for MIMOs necessitate an $n+m+1$ active switches, that results in minimising the efficiency because of high switching losses. Further, complexity of the converter increases significantly. A novel configuration MIMO topology is presented in literature (Nahavandi et al., 2014), for EV applications. In this configurations, both the voltages of output end is higher than the input voltages and are restricted by the output switches. Though, only one input RES can be permitted to supply power at a time and a wide choice of duty cycle operations cannot be possible.

A single inductor based multi input DC/DC converter is proposed in literature (Mohseni et al., 2019), (Li et al., 2020). The converter configuration has an advantage of less magnetic component and the design enables the sources to supply power simultaneously. But the topology suffers from lack of soft switching due to which losses are more. Moreover, inductor size will be large for high current application that leads to higher losses. It also suffers from isolation between source and load.

Lately, the TPC topology have been deliberate to integrate the RES and ESS topologies into single stage converter with dual-inputs. TPC configuration can receive two inputs. The output of the TPC DC-DC converter configuration can be associated to the DC load directly or to the grid or AC load. Many TPC topology, that can fulfil the MPPT and ESS charging and discharging constraint, have been described in the literature.

A systematic synthesis of multiple-input isolated and non-isolated DC/DC converter has been reported in literature (Li et al., 2010), (Wang et al., 2011). Similarly, an organised approach of the derivation of non-isolated TPC topology has been addressed in (Wu et al., 2014). Meanwhile all of the TPC are connected directly, this type of configurations can be utilised in those applications where the galvanic isolation is not mandatory (Rehman et al., 2015), (Banaei et al., 2014b). Alternative drawback of the non-isolated TPC is that the converter topology have a restricted voltage gain. That results in restriction of usage in modulation for the conversion of high voltage. Various literature address the use of coupled-inductor to enhance the voltage conversion ratio to overcome this concern (Hu and Gong, 2014), (Tang et al., 2015). In comparison to the non-isolated TPC, partly-isolated TPC, that utilise high-frequency transformer (HFT) to provide galvanic isolation between the sources and load with other two common-grounded ports (Wu et al., 2014), can achieve sophisticated voltage gain with a higher turn's ratio of the HFT. Alike to the partly isolated topologies, the

isolated topologies are based on the use of a HFT, that aids them to well balance the dissimilar voltage levels among the different ports. Nevertheless, the number of the devices utilised in this kind of topology is very high meanwhile the devices are seldom shared. While both of the partly-isolated and isolated topologies can be functioned with ZVS/ZCS on the switches by means of suitable control scheme and modulation techniques.

2.2.3 Dual-Input Isolated Topologies

A multi-input bidirectional DC-DC converter is presented in (Mangu et al., 2016) for household applications, that has an advantage of less number of components. However, the converter suffers from high power application in which the magnetic size will be large that leads to high power loss of the system and the proposed system has complex control strategy for power flow management. A systematic approach for synthesizing multi-input DC-DC converters have been introduced (Liu and Chen, 2009) along with pulsating sources. The pulsating sources are combined to provide the power from different sources. A systematic approach for deriving dual-input converters by utilizing a single-pole triple-throw switch is presented in (Gummi and Ferdowsi, 2010). In order to achieve high power rating of system, the converters can be connected in parallel that leads to reliable and high efficient method of increasing power rating, particularly current rating of the system (Chen et al., 2012). An isolated multi-input ZCS DC-DC front-end converter based multilevel inverter is presented (Reddi et al., 2018) for low power application. The main benefit of this converter is, it has only two active switches with a full-bridge rectifier at the front-end. However, the converter will have high stress on the switches which leads to more switching losses when it is implemented for high power applications. A multi-input based on three switches leg is presented in (Azizi et al., 2016b) for high current applications. It has an advantage of less number of components and still, the topology suffers from isolation between the input and load side. Single input source with parallel output configuration is explained in literature (Lin et al., 2017). The advantage of converter configuration is the simple control strategy, but the topology cannot meet the load if the source is unavailable. A multi-input DC/DC converter based on flux additivity has been reported in literature (Chen et al., 2002). The converter has an advantage of single HFT and a rectifier but still the topology suffers from magnetic losses when

high current low voltage application is adopted.

So, an isolated MPC that has AC link through HFT is preferred for its cost, size, safety and low leakage current in distributed systems (Mozaffari and Amirabadi, 2019). A CLL resonant converter-based MPC is proposed in literature (Asa et al., 2015) that consist of two CLL-tanks, HFTs, and a diode bridge rectifier. This MPC configuration diminishes the circulating currents but, the isolation between the two modules during dual-input mode of operation will end in either the elevated losses or inadequate outputs. Dual-input single output with secondary rectifier connected in parallel configuration is presented in (Kiran and Kalpana, 2018) maintains constant voltage but circulating current in the HFT will be high during short circuit condition of transformer at fixed voltage condition. An isolated multi-input bidirectional dual active bridge DC/DC converter is presented in literature (Karthikeyan and Gupta, 2018). The advantage of the converter configuration is the circulating power of the converter is less. But topology suffers from more number of devices and lack of ZVS due to which the losses of the converter is more and efficiency of the system is reduced. Among the isolated MPC configurations presented in the literature triple port converter (TPC) (Zhao et al., 2008), (Dao et al., 2020), (Jakka et al., 2018) is found to be the most significant configuration that has key features like soft switching, flexible voltage and power flow between different energy sources and proper isolation etc.,. TPC utilizes a three winding HFT in its isolation stage. Hence, if two input sources are providing AC voltage with phase difference across two of its windings, then the respective fluxes, due to these input sources oppose each other and as an outcome the resultant flux diminishes. Consequently, the induced voltage of HFT windings reduces and high inrush current flows through the input module converter sources switches. This will lead to excess on state switching losses. Moreover, TPC configuration is inconvenient for the application where two variable RESs are connected to meet the load requirements. This is due to the fact that, if there is a small variation in magnitude and phase between their respective AC voltage that leads to high circulating power between energy sources because of small leakage inductance between there interconnection winding of the transformer (Wang et al., 2018). Therefore, high circulating power leads in higher losses of the system. The ports of TPC cannot be isolated by switching ON and OFF the converter as windings are connected to the same core and antiparallel diode of the switches form the same path.

Moreover, TPC has a disadvantage of complex control strategy for sharing power

between two RESs (Huang et al., 2018), (Irfan et al., 2018), (Ma et al., 2020). In order to minimise the circulating power between input ports a complex control scheme with decoupling approach that includes composite mathematical design is needed. The prevalent isolated TPC DC-DC converter topology is voltage source fed ones. Rendering to the type of the ESS, the converter configuration essentially comprises the inductor-type and resonant-type ones. Because of the magnetic coupling amongst the windings of the HFT, that leads to power coupling between the input ports of the topology, which effects the ports to be unsuccessful to transfer power required by the load (Dao et al., 2020). The inductor-type converter configuration fails to realize power decoupling at the converter configuration level. Further, stress of current the in inductor type converter configuration is twice the operative output current. This results in surge in current stress on the active switches, that signifies in reduced efficiency and increase in the cost of the converter topology (Hu et al., 2018). A TPC isolated DC-DC topology such as power decoupling and the nonzero rapid power of the standby port, a TPC isolated bidirectional current-fed series resonant DC-DC topology is presented in literature (Wang et al., 2021).

However, TPC configuration is inconvenient for the application where two variable RESs are connected to meet the load requirements. This is due to the fact that, if there is a small variation in magnitude and phase between their respective AC voltage that leads to high circulating power between energy sources because of small leakage inductance between there interconnection winding of the transformer.

The following problems were identified from the literature,

1. High circulating current in the HFT as windings are on the same core in TPC.
2. Isolation of the ports cannot be done by switching as antiparallel diode of switches conducts even all the switches are turned off.
3. Lack of ZVS for the switches with complex control strategy.

So, in order to mitigate the above discussed problems from the literature and to reduce circulating power between input modules, this study presents a modified dual-input DC-DC converter that are connected in modular configuration for providing power supply to telecom load and charging of the batteries simultaneously. The proposed converter allows the source ports to operate with the extended range of phase delays and magnitudes to obtain the wide-ranging outputs with significantly reduced

circulating currents as compared to the three-winding transformer-based TPC. A proper control technique with digital control system to regulate the output voltage has been presented in this thesis. Fig. 2.4 shows the architecture of telecom power supply in standalone mode condition.

2.3 BI-DIRECTIONAL DC-DC CONVERTER

Bidirectional DC-DC converter is a converter topology that facilitates the electric energy to be transferred bi-directionally with the invariable polarity. Non-isolated bidirectional DC-DC converter configuration with an capability of transfer power from source to load and vice versa, has been extensively employed in numerous industrial applications, such as EV, UPS, space crafts, ESS etc., (Jain et al., 2000) (Moon et al., 2012). The HFT based converter configuration is an attractive one to achieve isolation between the source and load. However, with respect to enhance the efficiency of the system with size, weight , number of device and price a HFT less type converter configuration is more attractive. Therefore, for spacecraft or system with high power applications where size and efficiency is prime factor a HFT less non isolated topologies are more preferred. In order to increase the power density and minimising usage of inductance a bi-directional DC-DC converter topology has been presented in literature (Zhang et al., 2007), (Urciuoli and Tipton, 2006). The bidirectional DC-DC topology simplifies the system configuration and reinforces the permanency, providing for the employed characteristics of each energy ESS (Chen et al., 2001). The non-isolated bidirectional DC-DC topology can be categorised into Buck , Boost and Buck-Boost type (Chen et al., 2006a), among which Buck-Boost type will be a most supreme choice (Liu and Li, 2006), (Hosseini et al., 2008), (Peng et al., 2004), (Jose and Mohan, 2002). Moreover, maximum of the spacecraft in small earth orbit employ PV, in which the bidirectional DC-DC converter plays a vital role (Wu et al., 2010) . According to the operational mode of the drive, F. Caricchi et al. (Caricchi et al., 1998) offer the investigation, comparison, and modelling of two Bidirectional DC-DC converter topologies for changing battery voltage level to either high or low. Several charger converter configurations with ESS for grid-connected EV and power electronics converters are applied in bidirectional EV chargers together with DC-DC synchronous step-down and step-up converters, is proposed in literature (Sahinler and Poyrazoglu, 2020). H.Wang et. al. in (Wang et al., 2020a)

proposed the design and control scheme for bi-directional DC-DC converter topology for HEV. In this system, the power to the DC bus will be transferred by both PV and ESS under low adequate sunlight conditions. W. Yongqing et. al (Yongqing and Haiyan, 2019) proposed the control scheme for PV and ESS system under stable bus voltage. RES such as PV requires DC-DC voltage conversion to alter DC voltage. R. Kaye et. al has proposed a brief review in literature (Kaye and Kalam, 2019) of various DC/DC converter topologies for power conversion at PV array output for AC loads. N. Dubey et. al. (Dubey and kumar Sharma, 2019) has presented the quadratic nature of charging and discharging of bi-directional converter configuration for attaining greater voltage gain ratios in step-down and step-up operation. Further, the topology is able to achieve reduced ripple during both charging and discharging of battery. A DC-DC converter configuration is presented by E. -S. Kim et. al in (Kim et al., 2019) employing bi-directional DC-DC converter topology for battery charging applications. The charging is step-down mode and discharging is step-up mode. Modelling and designing of BDC is presented in (Yaoqin et al., 2018), (Xu et al., 2016). A small-signal discrete-time model of bi-directional DC-DC converter topology is proposed in (Aziz et al., 2018) and it has been compared with continuous-time average model. AC-DC and DC-AC Bidirectional EV battery charger topology is presented in literature (Prasanna et al., 2016). The proposed converter facilitates to operate in all four quadrant of P-Q plane. L. Prasanna et. al. (Verma and Singh, 2016) proposed control of hybrid energy storage system for EV application using bi-directional DC-DC converter topology and performance is examined of normal speed and regenerative braking. (Pooja and Rubymeena, 2020) proposed control scheme for charging and discharging by utilizing bi-directional DC-DC converter topology.

From the literature, it is found that bidirectional nature of the bi-directional DC-DC converter topology is very expedient when it comes to application in charging-discharging of the battery. This nature is utilized in this thesis and a topology is developed to charge the battery and discharge the battery whenever required by the load. Further, CC/CV (Li and Ma, 2022), (Chen et al., 2019), (Wang et al., 2020b) mode of charging has been implemented for presented topology.

2.4 TELECOM LOAD PROFILE

The transceivers in BTS station operates in a pulsed-power mode intermittently also the power consumption of BTS depends on signal traffic. (Liu et al., 2005) have modelled the BTS load profile based on the assumptions that the TRX operates for 200s out of every 250s. During the on state condition, TRX draws the high amount of power for 10sec and for the next 10sec TRX draws low power. (Lorincz et al., 2012) have given the 5 days load profile of working BTS station which is shown in Fig. 2.3. The DC loads in BTS stations requires the constant DC voltage (i.e. 48V). However, due to pulsed power consumption of DC loads voltage will have fluctuations. Therefore, for safe operation voltage across DC loads has to be maintained constant.

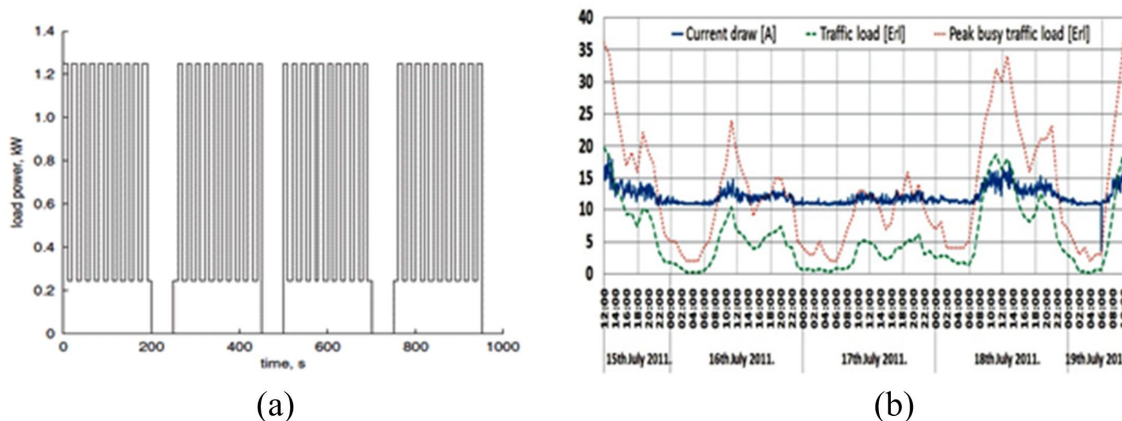


Figure 2.3: Power consumption and load current profile of BTS load. (Lorincz et al. (2012))

2.5 IDENTIFIED RESEARCH GAPS

The following research gaps are worth highlighting based on the concise review conducted in the previous section:

At present, MIC topologies are developed with enhanced efficiency and minimum number of active and passive devices. Though, the problem associated with minimizing quantity of the output ripples have not been taken much attention. Traditional approach for integrating several RESs places them either in parallel or series structures. For MICs that are connected in parallel structure, the current on the load end

will be the addition of current from each individual converter topology. Whereas, MICs that are connected in series structure the voltage at the load end is the summation of the voltage from each individual converter topology. Therefore, the ripples of voltage and current at the load end surges when the ripples are summed up from individual topology, which leads to condense the performance of the converter topology. Conversely, in traditional approaches for dual input voltage sources coupled in series, a control switch has to be facilitated for individual DC sources to act as by-pass short circuit for input current of other source. Moreover, for a parallel structure, due to the dissimilarity between two DC voltage amplitudes, only one of the two sources can be operated at a time. Hence, it will be very challenging to accomplish the desired regulated output voltage from both series and parallel structures of configurations. The foremost challenges of designing a dual-input DC-DC converter topology is to handle RESs with an altered value and to progress the converter parameters such as reduced current ripple, minimum ripple voltage, and high efficiency.

The proposed multi-input converter in the literature have limitations of isolation, more number of switches, low power rating and high voltage application with complex control strategy. However, in the BTS load applications the DC link voltage has to be isolated and maintained constant. Therefore, overall count and cost of the converter are increased in the system. However, DC loads of BTS operates in the pulsed power mode and also the average load current varies with signal traffic, the conventional voltage regulation control may fail to maintain 48V across the DC loads. In this study, a dual-input converter with appropriate load sharing control strategy with low ripple and high performance has been proposed.

Further, the proposed voltage regulation algorithms in literature have a common limitation of slow response during the pulsed load variation conditions. However, DC loads of BTS operates in the pulsed power mode and also the average load current varies with signal traffic, the conventional voltage regulation algorithms fails to maintain 48V across the DC loads.

2.6 RESEARCH OBJECTIVES

The presented works aims to analyse, design and develop a renewable based hybrid power supply system for powering standalone Telecom load. After detailed literature review of dual-input converter for Telecom load the following objectives were identified

for carrying out the research work. The block diagram of the PV/Biomass/Battery based standalone hybrid power supply system is shown in Fig. 2.4.

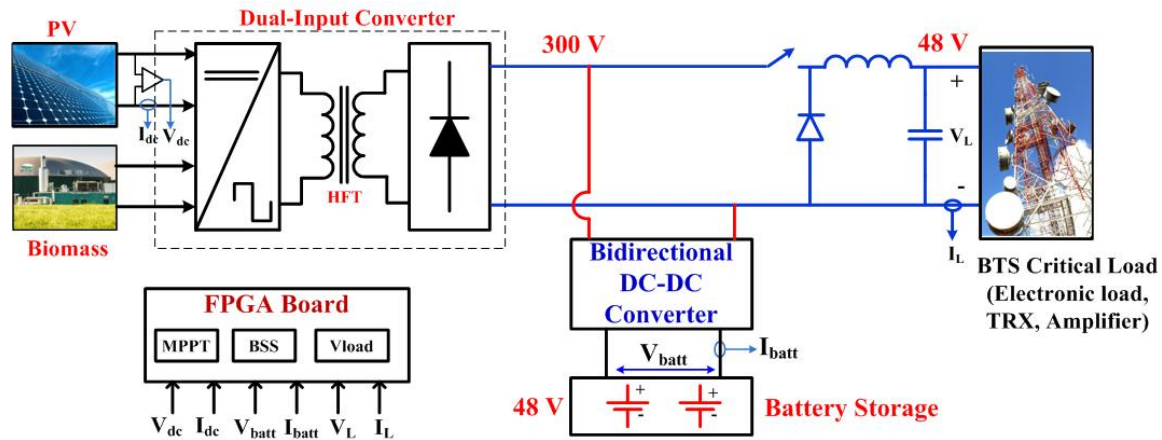


Figure 2.4: Schematic of developed hybrid power supply system for telecom load

1. To propose a Dual-Input DC-DC converter for Telecom load by integrating renewable energy sources in standalone mode condition
 - Design, analysis and simulation of the dual-input full-bridge DC-DC converter.
 - Experimental validation
2. To propose a Dual-Input half-bridge DC-DC converter for Telecom load by integrating renewable energy sources in standalone mode condition
 - Design, analysis and simulation of the dual-input half-bridge DC-DC converter.
 - Experimental validation
3. Development of voltage regulation control algorithm that maintains output voltage constant for the pulsed-power mode operation of DC-DC converter used for Telecom load.

Chapter 3

DESIGN AND DEVELOPMENT OF MODULAR DUAL-INPUT FULL-BRIDGE DC-DC CONVERTER FOR TELECOM POWER SUPPLY

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3.1 GENERAL

In this chapter, three converter topologies are discussed. First, a modular dual-input DC-DC converter topology is presented. Complete design and analysis of the converter is presented in detail. The presented system has two individual inputs with rectifiers that are connected in parallel at secondary circuit for achieving constant voltage across the load. The presented system integrates two energy sources resulting in an advantage of having compact structure with less number of components. Complete design of the presented converter with FPGA based digital control strategy have been presented in this chapter.

Secondly, in order to reduce number of components and minimise circulating power between the ports, a modified modular dual-input DC-DC converter topology is designed and an extensive laboratory prototype has been discussed in this chapter. The presented converter has two individual input modules with three-leg semi active rectifier connected in parallel at secondary side for achieving constant voltage across the load with reduced circulating power. This results in an advantage of having compact structure with reduced number of components.

Further, a bidirectional DC-DC converter topology for charging and discharging of battery is presented. The chapter is systematized as follows. Section 3.2 illustrates the details of modular full-bridge DC-DC converter topology. Section 3.3. presents modified modular dual-input full-bridge DC-DC converter topology. Similarly, section 3.4 briefly discuss the bidirectional DC-DC converter topology for charging the battery. Finally, simulation and experimental results of all the converter is presented in this chapter. Further, a detailed comparative analysis is illustrated.

3.2 MODULAR DUAL-INPUT FULL-BRIDGE DC-DC BUCK CONVERTER

The schematic of modular based dual-input DC-DC converter for telecom load with battery charging application is shown in Fig. 3.1. In order to achieve constant voltage across the load side with stable current sharing of converter the full-bridge converters are connected in parallel from two individual variable sources. It consists of HFT that provides isolation between the systems and aids in reducing the compact size with low magnetic losses for high current applications.

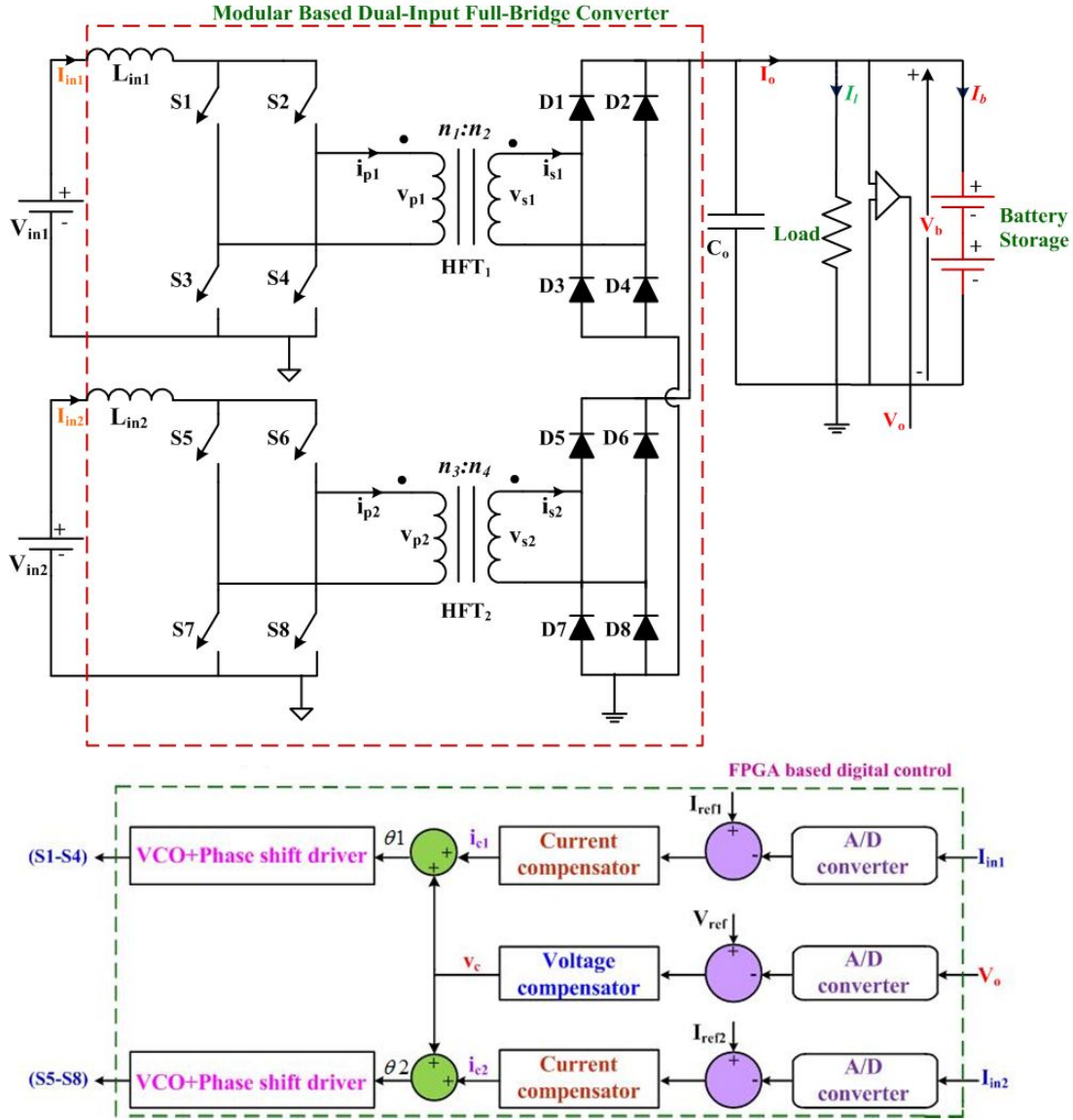


Figure 3.1: The schematic of the modular based dual-input DC-DC step-down converter for telecom load with battery charging application

The significance of connecting the system in parallel is to maintain constant voltage across the load and simultaneously charge the battery. The full-bridge rectifier reduces the size of HFT by reducing number of turns compared to center tapped HFTs which has twice the number of turns. Since both the sources are variable the presented converter aids in providing constant voltage for load and battery charging simultaneously. The presented converter can provide the required voltage for both load and battery simultaneously, even if one of the source is unavailable. The devel-

oped modular dual-input DC-DC converter will help in providing regular and stable power supply for BTS in standalone mode condition. Further, the battery voltage can be utilized for AC loads of BTS. Hence the presented system plays a significant role in eliminating DG and providing clean power solution to BTS in standalone mode condition. The complete design of the presented converter with FPGA based digital control scheme using DSP builder is presented in next section.

3.2.1 Operation and Analysis of the Converter

Fig. 3.1 illustrates the dual input modular based full bridge DC-DC topology for telecom load and battery charging applications. It consist of two HFTs and a common output stage at secondary circuit connected in parallel configuration that is driven by two different renewable energy sources. HFT_1 and HFT_2 are buck transformer in which the voltage will be stepped down to meet the requirement of telecom load. According to the topology the operation can be analyzed as dual input mode and single input mode. Operation and analysis of the dual input mode topology is discussed in this section.

3.2.1.1 Dual-Input Mode of Operation

The key waveforms for the operation of presented dual-input converter is shown in Fig. 3.2. It illustrates the modes of operation for different interval of dual-input step-up full-bridge converter. Each pair of driven signal has 180 degree phase shift for switches S1, S4 and S2, S3. Similarly switches S5, S8 and S6, S7 are driven from same gate signals. The assumptions that are considered to streamline the examination of the proposed topology are as follows:

1. An ideal HFTs with insignificant leakage and magnetizing inductance and ideal switching devices and diodes.
2. The input inductance L_{in1} and L_{in2} are large enough to sustain the continuous current.
3. Inductor L_{in1} and L_{in2} are considered as constant current sources and the output capacitor C_o is deliberated to be large enough to sustain ripple free constant output DC voltage.

Interval 1 Interval 1 ($t_0 < t < t_1$):

As illustrated in Fig. 3.3 (a) at this stage all the switches S1-S8 and D1 - D8 are turned off. So there will be no transfer of power from either of the sources to load. On the same way the power to load will be transferred from the output capacitor C_o .

Interval 2 ($t_1 < t < t_2$):

Module 1: As illustrated in Fig. 3.3 (b) at this stage diagonal switches S2, S3 of leading, lagging leg respectively and D2, D3 will conduct to deliver the power from sources1 to load via HFT₁.

Module 2:

At this stage same gating signal will be given to diagonal switches S6, S7. Similarly as module 1 switches S6, S7 conducts to deliver power from source2 via HFT₂ through D6, D7 to the load. At this stage power from both the sources will be transferred to load continuously and simultaneously. As both the secondary side rectifiers are connected in parallel the voltage will be maintained and current will be transferred to load. The resulting output voltage V_o is directly related to on state time of switches and the relation can be derived from integrating the voltage v_{p1} and v_{p2} over one time period T_s . The average voltage V_o is given by

$$V_o = \frac{1}{T_s} \int_0^{T_s} v_{p1}(t) dt \quad (3.1)$$

$$V_o = \frac{1}{T_s} \int_0^{t_{on}} \frac{n_2}{n_1} V_{in1} dt + \int_{t_{on}}^{T_{off}} 0 dt \quad (3.2)$$

$$V_o = 2 \frac{n_2}{n_1 T_s} V_{in1} D T_s \quad (3.3)$$

$$\frac{V_o}{V_{in1}} = 2 \frac{n_2}{n_1} D \quad (3.4)$$

Similarly, for the second source output voltage equation can be expressed as follows

$$\frac{V_o}{V_{in2}} = 2 \frac{n_4}{n_3} D \quad (3.5)$$

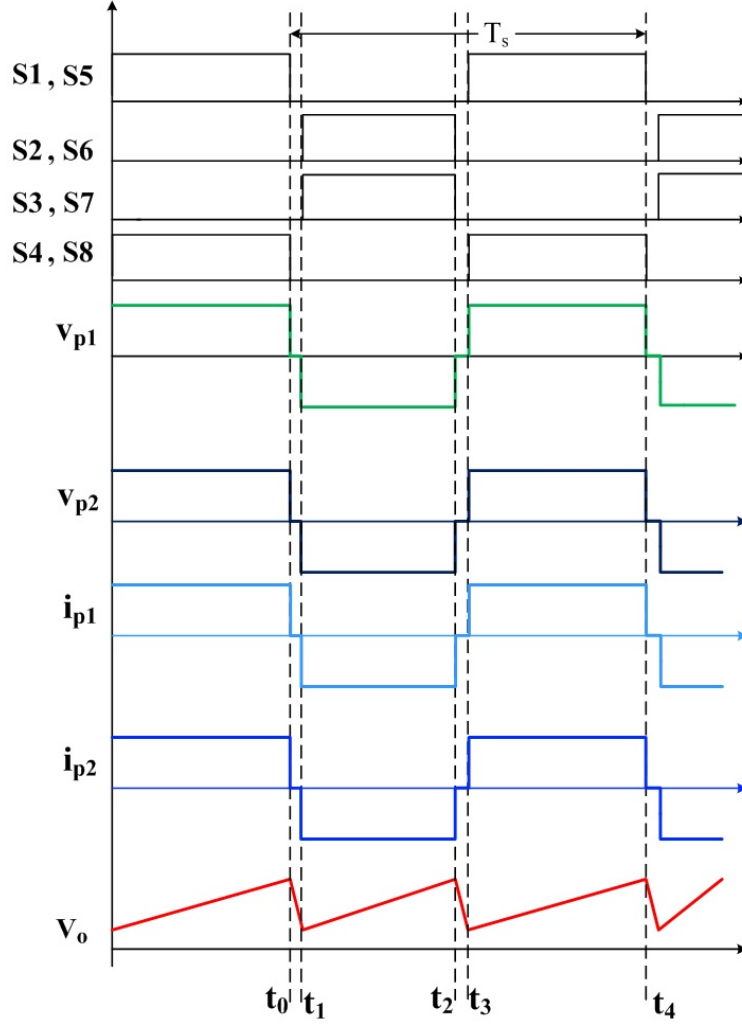


Figure 3.2: Key waveforms of modular based dual-input DC-DC step-down converter for telecom load

RMS current of each converter can be expressed as

$$I_{1,RMS} = \sqrt{\frac{1}{2T_s} \int_0^{2T_s} i_{p1}^2(t) dt} \quad (3.6)$$

$$I_{1,RMS} = \frac{n_2}{n_1} I_o \sqrt{D} \quad (3.7)$$

Similarly, RMS current at secondary winding of HFT_1 can be expressed as

$$I_{2,RMS} = \frac{1}{2} I_o \sqrt{1 + D} \quad (3.8)$$

where D is duty ratio of each switch. Similarly current expression for HFT_2 can also be derived on the same basis.

Interval 3 ($t_2 < t < t_3$):

As illustrated in Fig. 3.3 (c) at this stage all the switches will be turned off. Hence, no power will transform from source and the power to load will be satisfied from output capacitor.

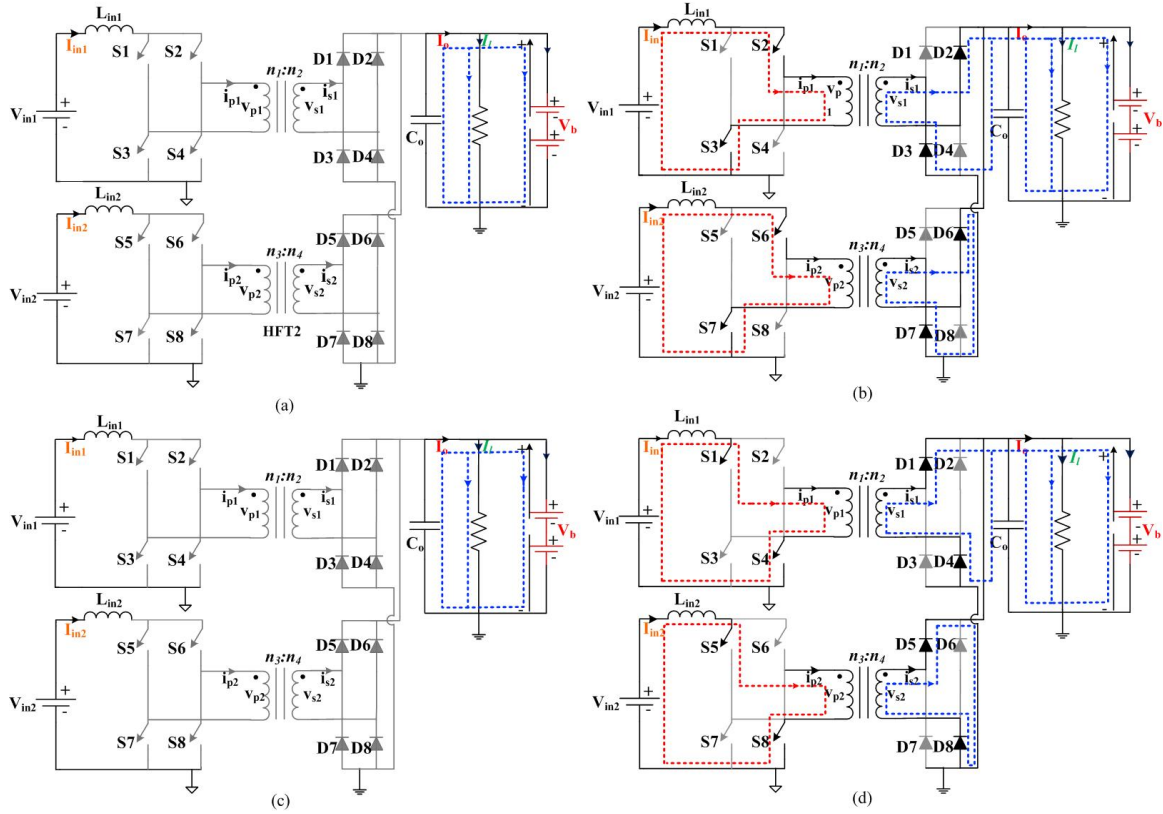


Figure 3.3: Modes of operation of modular based step-up full-bridge DC-DC converter (a) Interval 1 (b) Interval 2 (c) Interval 3 (d) Interval 4.

Interval 4 ($t_3 < t < t_4$):

Module 1: As illustrated in Fig. 3.3 (d) at this stage diagonal switches of leading and lagging leg $S1, S4$ and diode $D1$ and $D4$ will conduct to deliver power from source 1 to load via HFT_1 .

Module 2: At this stage as same gating signal are given to switches S5, S8. The power from source 2 to load will be transferred via HFT₂. At this interval diode D5 and D8 will conduct to transfer power from source to load.

From equation (3.4) and (3.5), it is clear that the presented converter can be decoupled into two independent buck converter based on PWM modulation strategy. Neglecting losses and considering all parasitic components are loss less the power P_o is summation of both input sources. Single input mode also works on the same principle since both are separately connected and outputs are parallel the presented configuration will aid in providing power supply to load and battery charging even in the absence of the one of the sources.

3.2.1.2 Design of the Modular Dual-Input DC-DC Converter

The design illustration of the components is discussed in this section. The designed values are utilized for simulation and experimental prototype of the presented system.

Design Consideration of HFT:

The parameters that effect design of HFT includes the selection of switching frequency, core, and calculation of turn's ratio. Turns ratio required to step-down voltage of 48 V can be calculated from the equation

$$n = \frac{((V_o/2)D_{max}) + 1}{V_{in} - 2} \quad (3.9)$$

n₁=0.3, where V_o is the output voltage and D_{max} is duty ratio of single switch V_{in} is the input DC voltage of the converter. Similarly, n₂ is 0.3. The selection of switching frequency plays a significant role in designing an HFT that makes compact size of the converter. Hence, switching frequency of f_s=20 kHz is preferred for both the HFTs.

Depending on power rating and frequency of the presented converter the chosen core for both HFT is U101/76/30. Effective magnetic cross section and window area is represented by Ac and Aw respectively, from the specification area product (Ap) can be calculated as Area product Ap= AcAw=8.48 cm⁴. Inductance of HFT primary and secondary winding can be found from the expression (3.10). The magnetizing inductance Al is selected from specification of core manufacturer.

$$L = A_t n^2 \quad (3.10)$$

Design of filter capacitor (C_o):

In order to minimize the voltage ripple of DC output voltage an output filter capacitor is designed. So, the output filter capacitor (C_o) can be designed from the equation (A I Pressman)(3.11)

$$C_o = \frac{(80 \times 10^{-6})\Delta I}{\Delta V} \quad (3.11)$$

where I represents the ripple current considering 2% of estimated current and V represents ripple voltage of 0.48 V considering 1% of rated output DC voltage. The value of C_o from calculation is 4.6 μ F.

Design of Battery system

From the literature, it's found that the aging of battery rely upon Depth of Discharge (DoD), running temperature, the charging voltage, and charging/discharging current. So, by considering the maximum DoD as 80 %, the size of battery can be found from equation (3.12)

$$Capacity(A_h) = P_t \left(\frac{N}{n_{bat}} \right) (DoD(V_b)) \quad (3.12)$$

where V_b represents the battery voltage and N represents number of back up hours required. As multi input sources are considered for power generation there will always be surplus energy available for the system.

3.2.2 Control Scheme for the Modular Dual-Input Converter

An appropriate control strategy is required for proper voltage regulation of the presented converter. A control strategy scheme for closed loop operation of the presented modular converter configuration is shown in Fig. 3.1. The implementation of digital control is a viable option that gives robust and precise control performance. The voltage control algorithm has been implemented using FPGA board. The control scheme consist of sensor gain, 12 bit A/D converter, two current compensator, one voltage compensator and has two phase shift driver circuit and modulator. I_{in1} , I_{in2} are actual input currents from both the sources, I_{ref1} and I_{ref2} are reference current and V_o is rated output voltage and V_{ref} is the reference voltage. Error signal that

is fed to current compensators are generated by comparing actual currents with reference currents. Phase shift control signal θ_1 is addition of voltage control signal V_c and current control signal i_{c1} similarly θ_2 is addition of voltage control signal V_c and current control signal i_{c2} . The phase shift percentage gate signal for each input can be determined by θ_1 and θ_2 that are given to phase shift drivers. By proper fine tuning of phase shift percentage with suitable current control signals the output voltage regulation can be obtained and balanced power flow from source to load can be achieved. VCO with digital control is designed for the presented topology. Based on the controlled voltage VCO is an analog circuit that can be utilized to yield a variable frequency that can be realized using a digital signal processor. The relation between the input signal V_{ctr} and output signal ω_o is represented as $\omega_o = \omega_1 - K_{vco} V_{ctr}$ Where free running frequency of the VCO is represented by ω_1 and K_{vco} is the gain of the voltage controller. Fig. 3.4 illustrates the block diagram of VCO.

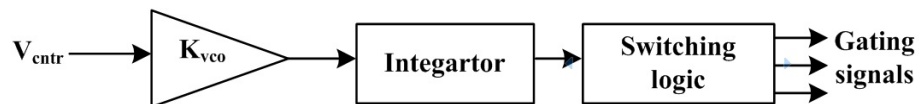


Figure 3.4: Block diagram of VCO

3.2.3 Results and Discussion

The presented modular based dual-input DC-DC converter with feedback control loop by utilizing designed parameters has been simulated in MATLAB environment. The modular based dual-input converter is designed for 48 V and power rating of 3 kW. Simulation and experimental results for the the presented converter topology is discussed in this section. Fig. 3.5 (a) shows waveforms of input voltage and current of source 1. Fig. 3.5 (b) shows the waveform of input voltage and current of source 2. The waveforms shows that both the sources have different voltage and power rating. Fig. 3.6 (a) and (b) shows the waveforms of primary input and secondary output voltages of both HFTs. Voltage v_{p1} , v_{s1} are input and output voltage waveforms of HFT₁ respectively. Voltage v_{p2} , v_{s2} are primary and secondary voltage waveforms of HFT₂ respectively. The resulted waveform shows that input primary voltages of both the HFTs are different and secondary waveforms shows that the voltage is stepped down to 48 V. Fig. 3.7 (a) shows the rectified DC voltage V_o and current I_o . The resulted

waveform shows ripple free constant voltage of 48 V. The dynamic performance of the presented modular converter has been deliberated by switching the load from steady state condition.

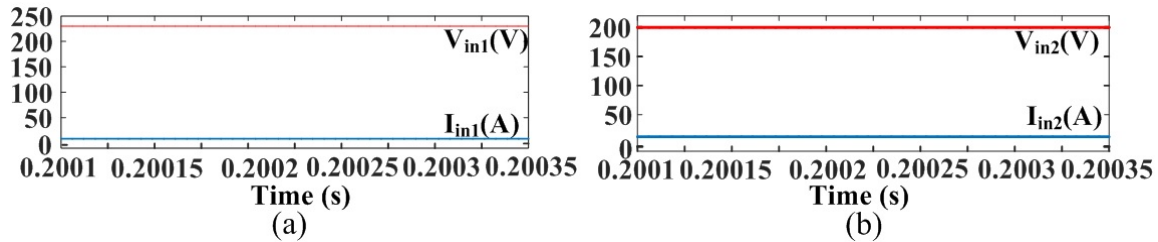


Figure 3.5: Simulation waveform of (a) input voltage and current of source1. (b) Input voltage and current of source 2.

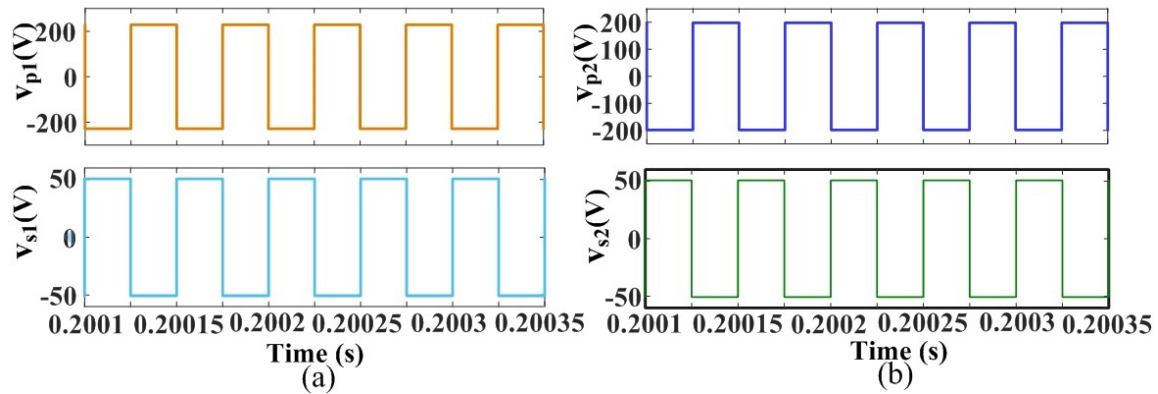


Figure 3.6: Simulation waveform of (a) Waveforms of Input and output voltage of HFT₁. (b) Waveforms of Input and output voltage of HFT₂.

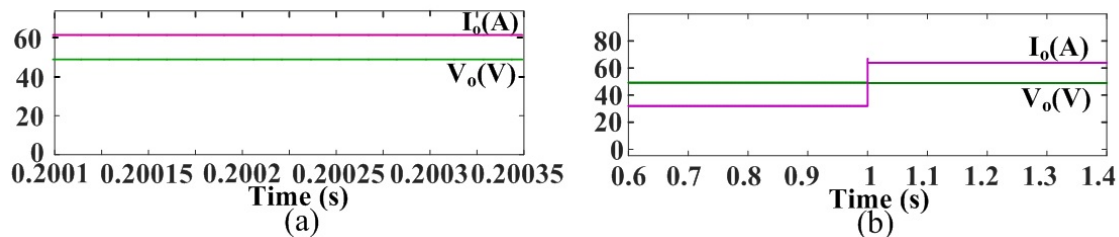


Figure 3.7: Simulation waveform of (a) Voltage and current waveforms of rectified DC output voltage and current. (b) Waveform of dynamic behaviour under step load condition from half load to full load.

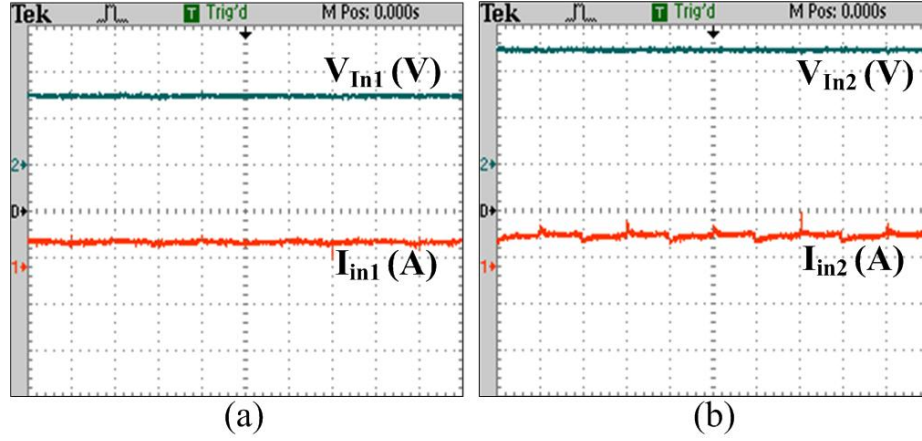


Figure 3.8: Experimental waveforms of (a) Input voltage (200 V/div) and current (5 A/div) of source 1. (b) Input voltage (100 V/div) and current (5 A/div) of source 2.

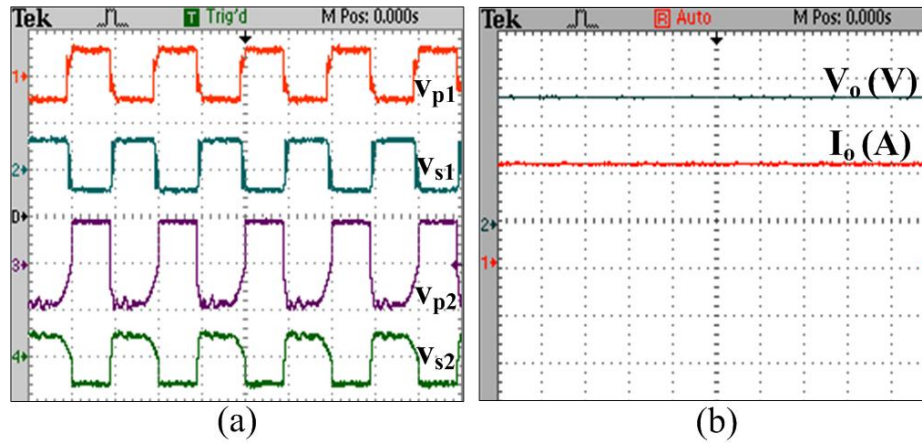


Figure 3.9: Experimental waveforms of (a) Voltage waveforms of HFT₁ ($v_{p1}=500\text{V/div}$, $v_{s1}=100\text{V/div}$) and HFT₂ ($v_{p2}=200\text{V/div}$, $v_{s2}=100\text{V/div}$). (b) DC output voltage (20 V/div) and current I_o (10 A/div).

Fig. 3.7 (b) shows the dynamic behaviour under step load condition from half load to full load. The resulted waveform shows that the output voltage remains to be constant irrespective of load changes.

To examine and justify the feasible operation of presented modular based converter a laboratory prototype is developed for 1 kW power for both load and charging the battery for lower voltage rating. FPGA board is used to implement the control algorithm of the proposed modular dual-input converter. One of the converter input is connected from 230 V/2.2 A current and the other converter is connected from 240 V/3.2 A source. Fig. 3.8 (a) shows the input voltage/current waveform of input

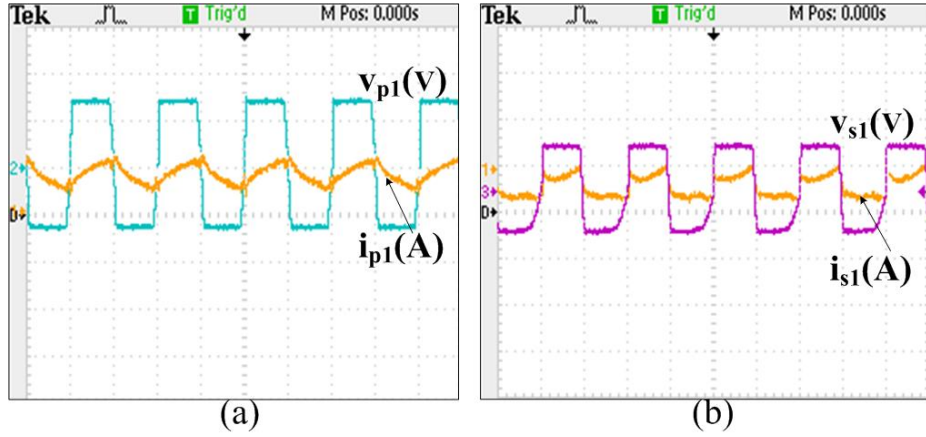


Figure 3.10: Experimental waveforms of (a) Experimental waveform of input voltage (200 V/div) and current (5 A/div) of HFT₁. (b) Experimental waveform of output voltage (50 V/div) and current of HFT₁.

source1 and Fig. 3.8 (b) shows the input voltage/current waveform of source 2. Fig. 3.9 (a) shows the experimental voltage waveforms of both the HFTs. The resulted waveform shows that both HFTs secondary are stepped down to 48 V. Fig. 3.9 (b) shows the experimental waveforms of ripple free DC output voltage and current waveform. It shows that voltage 48 V remains constant and currents are shared between the load and battery charging. Fig. 3.10 (a) shows input voltage and current waveform of HFT₁. Fig. 3.10 (b) shows output voltage and current waveform of HFT₁. Fig. 3.11 (a) shows the experimental waveforms of dynamic behaviour under step load condition. The waveform shows that voltage V_o remains to be constant irrespective of load changes and currents is varied accordingly. Fig. 3.11 (b) shows output voltage and current waveform of HFT₁. The experimental waveforms verifies the feasible operation of the presented modular configuration in delivering power to telecom load even one of the source is not supplying power.

3.2.3.1 Comparison of Modular Dual-Input Converter Topology with other Configurations Available in the Literature

In order to demonstrate the dominance of presented topology over the other presented converter a comparison has been deliberated. Table 3.1 shows the comprehensive comparison of the proposed topology with other converters in terms of component counts, isolation between the circuit, stresses on device with respect to loss consideration for high power application and also the complexity of control strategy has been preferred

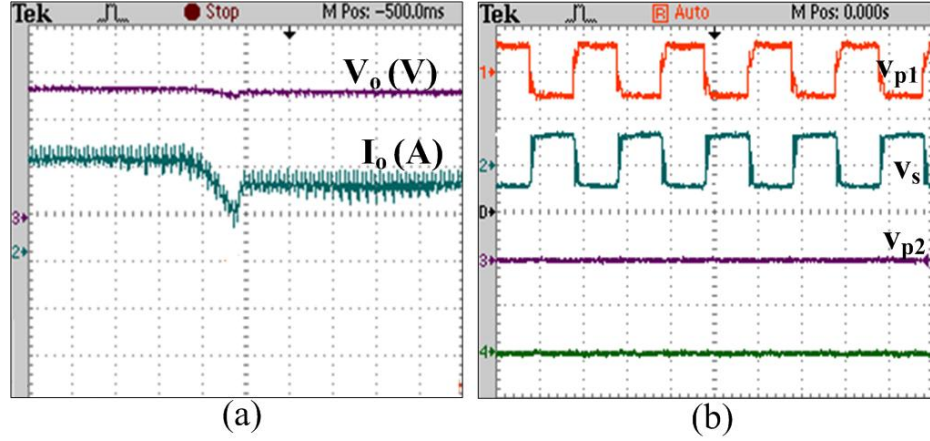


Figure 3.11: Experimental waveforms of (a) Output voltage ($V_o=20$ V/div) & I_o (10 A/div) waveform for load change condition. (b) Voltage waveforms of HFT1 ($v_{p1}=500$ V/div, $v_s= 100$ V/div and $v_{p2}=0$ V/div).

for the analysis. It can be observed from the illustration of Table 3.1 that the presented system has an advantage of reducing magnetic size for high current application which reduces system losses. The advantage of presented converter that it can supply power to both load and battery charging simultaneously even if one of the source is unavailable. Since, FPGA based digital control algorithm has been realized for control strategy, it aids a superiority over other compared converter configurations

Table 3.1: Comparison of modular dual-input converter with other converters available in the literature

Parameters	Mangu et al. 2016	Reddi et al. 2018	Azizi et al. 2016	Presented converter
Input Sources	2	2	2	2
Output Capacitors	3	1	1	1
Active Switches	10	2	6	8
No. of HFTs	1	1	0	2
Passive Device	0	4	6	8
Controller	complex	complex	complex	moderate

3.3 MODIFIED MODULAR DUAL-INPUT FULL-BRIDGE DC-DC BOOST CONVERTER

The dual-input converter configuration as discussed in the previous section has a greater number of passive device and circulating current of the HFT may be high during parallel operation of the converter. Hence, to diminish the circulating current in HFT and to minimize the number of passive devices the configuration has been modified as shown in Fig. 3.12. The primary side of modified modular dual-input converter configuration has two active bridges comprising of eight switches S1-S4 and S5-S8 that are connected from two different energy sources. The output of the two HFTs is connected to a three-leg rectifier at secondary side. The equivalent circuit for secondary side rectifier is exemplified in Fig. 3.13 to illustrate the three-leg rectifier connection noticeably. It is a semi active bridge that consists of one active leg with switches S9, S10 and two passive legs with diodes D_{r1} - D_{r4} . The active switches S9 and S10 and the passive leg D_{r1} , D_{r2} will build one full-bridge rectifier (FBR) for HFT₁. Whereas, the passive leg is composed of D_{r1} - D_{r4} builds another full-bridge rectifier circuit for HFT₂. The passive leg composed of D_{r1} and D_{r2} shares the two FBRs. The output of two full-bridge is in parallel to achieve proper voltage regulation with extended voltage range. The inductance L_{r1} and L_{r2} can be either leakage inductance of a transformer or it can be built separately to gain the desired value is a significant element in determining the power handling capacity. The modified modular dual-input converter configuration offers two HFTs as shown in Figure 3.12. Hence, there is no direct leakage inductance between the inputs active bridges that aids in minimizing the leakage power between the two sources. Therefore, the modified configuration benefits in reducing circulating current between the modules of HFTs as compared to other triple active bridge converter. The modified converter configuration can be connected from different energy sources to operate with increased phase shift ratio with magnitudes that adds an advantage in obtaining regulated output with significantly minimum circulating current in HFT. Further, ZVS is achieved over an extended range of output that gains in enhancing the efficiency of the complete system with minimum losses. Along with this, the output is connected to bidirectional converter with minimum switches to charge the battery and same way to discharge the battery whenever required by the load.

The assumptions that are made to streamline the examination of the modified

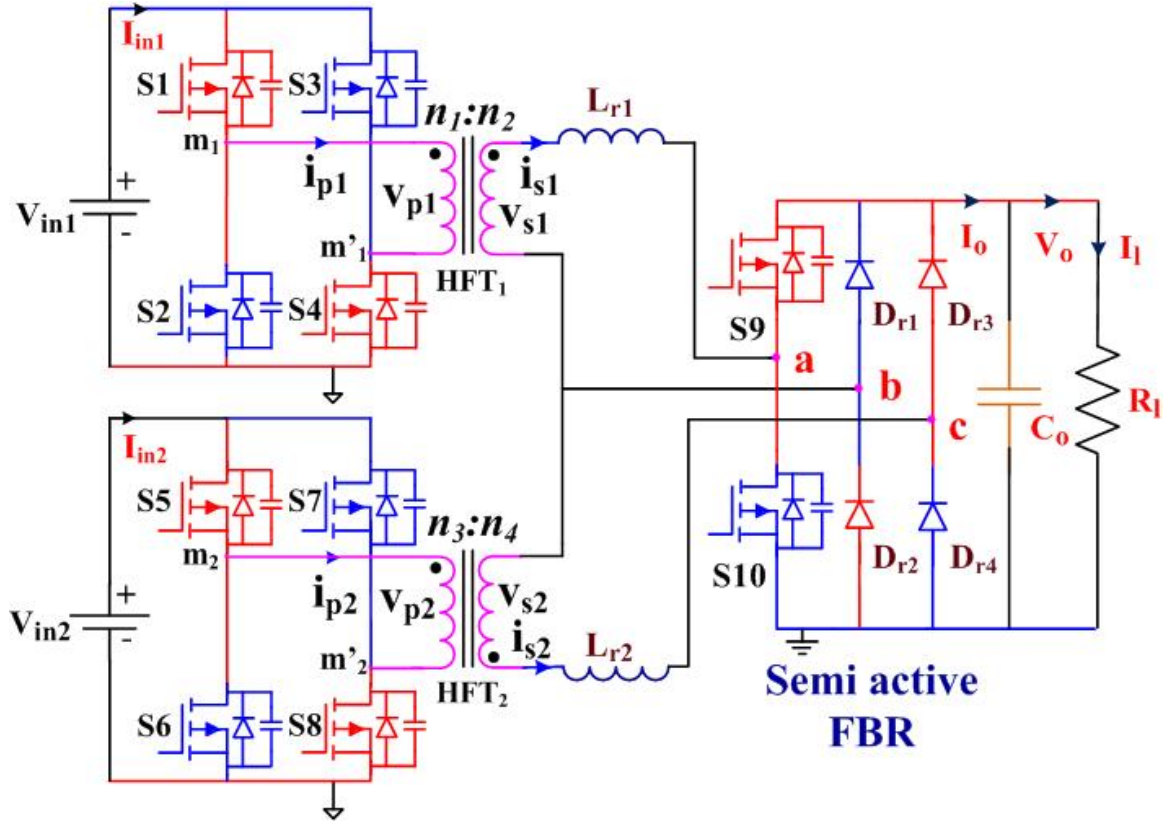


Figure 3.12: Schematic of modified modular dual-input full-bridge DC-DC converter configuration

modular dual-input converter configuration are:

1. HFTs are considered to be ideal with insignificant leakage and magnetizing inductance.
2. All diodes and switching devices are considered to be ideal. Output Capacitor C_o value is large enough to maintain constant output voltage

3.3.1 Modes of Operation

The modified modular dual-input converter configuration can be operated in two different mode as dual-input mode when both the sources are available and single input mode when one of the sources will be active and load. In this section dual-input mode of operation is explained in detail. The steady state operating waveforms for the operation of modified dual-input converter is shown in Fig. 3.14.

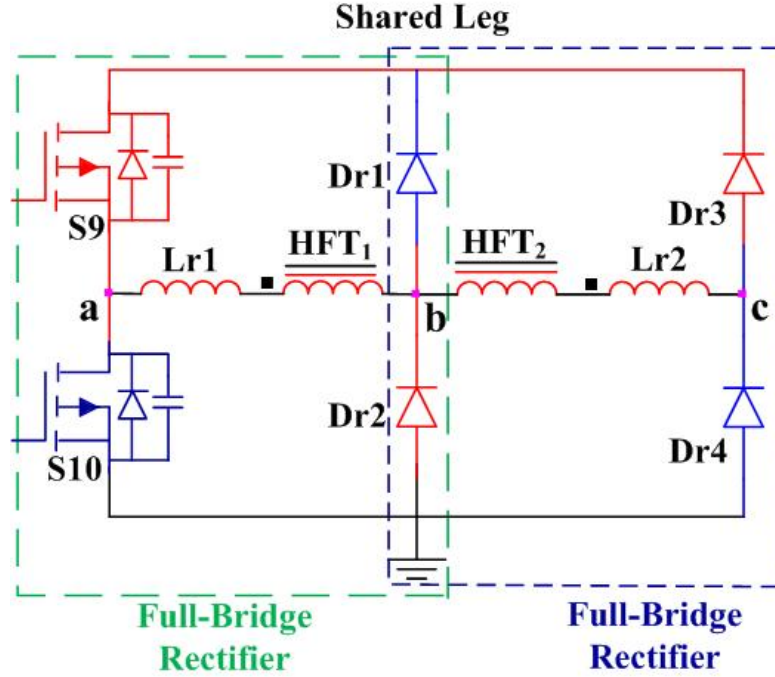


Figure 3.13: Three leg semi active full-bridge rectifier

The operation over a complete switching cycle has been divided into six different time intervals. The equivalent circuits of the modified dual-input converter circuits depicting the conduction status of switches and HFT winding currents in closed loop condition is shown in Fig. 3.15. It is considered that for analysis of new interval, the secondary currents i_{s1} and i_{s2} are having negative values and switches S2, S3, S6, S7, and S9 are turned ON and all other switches are turned OFF. D_{r2} , D_{r3} are ON and D_{r1} and D_{r4} are in OFF condition.

Interval 1 ($t_o < t < t_1$)

This interval begins when S2 and S3 are turned OFF as shown in Fig. 3.14 . Here the secondary voltage V_{s1} shifts from negative to positive polarity. The input current i_{p1} changes from S2, S3 to D1, D4 correspondingly in natural way. Where D1 and D4 are antiparallel diodes of switches S1 and S4 respectively. S1 and S4 are turned ON once secondary current i_{s1} becomes zero at Z_1 as shown in Fig. 3.14. Hence, ZVS is achieved at this instant. Fig. 3.15 (a) shows the equivalent circuit diagram for closed loop path for primary and secondary winding current flow during this interval. The secondary current expression from the steady state waveform with respect to interval

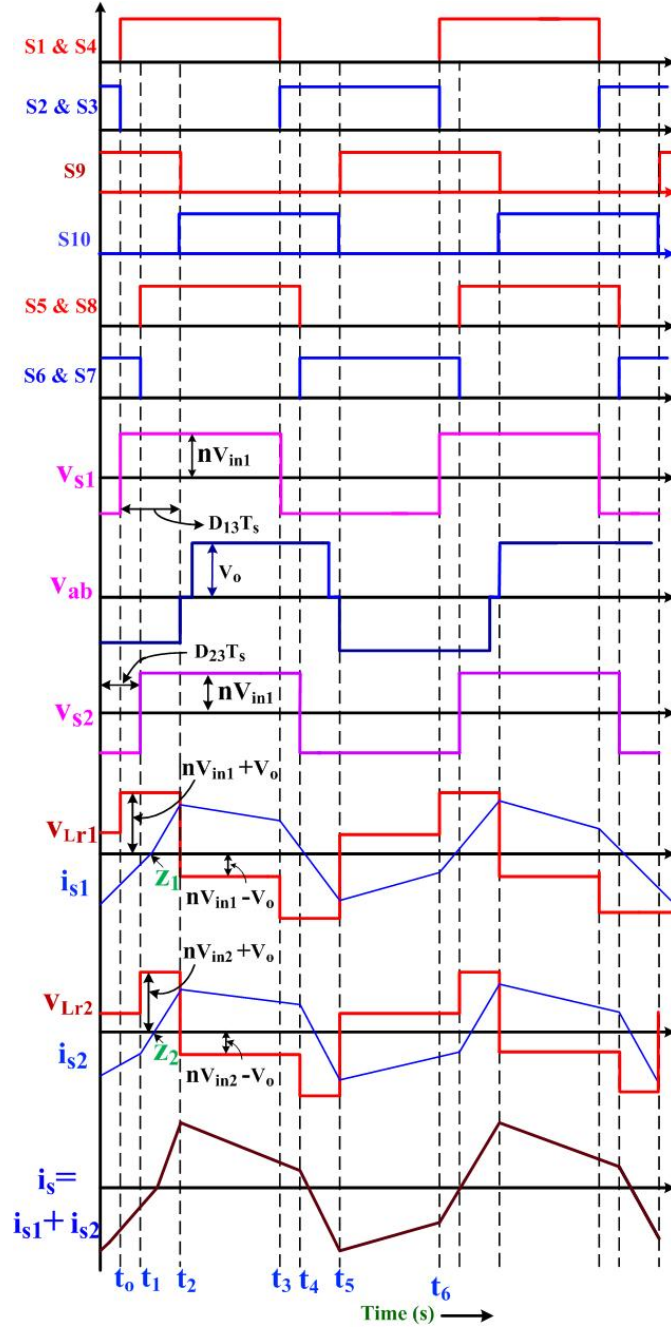


Figure 3.14: Steady state operating waveforms for modified modular dual-input converter configuration

t_0-t_1 can be represented by equation (3.13)-(3.14)

$$i_{s1}(t) = ((nV_{in1}) + V_o/(L_{r1}))(t - t_o) + i_{s1}(t_o) \quad (3.13)$$

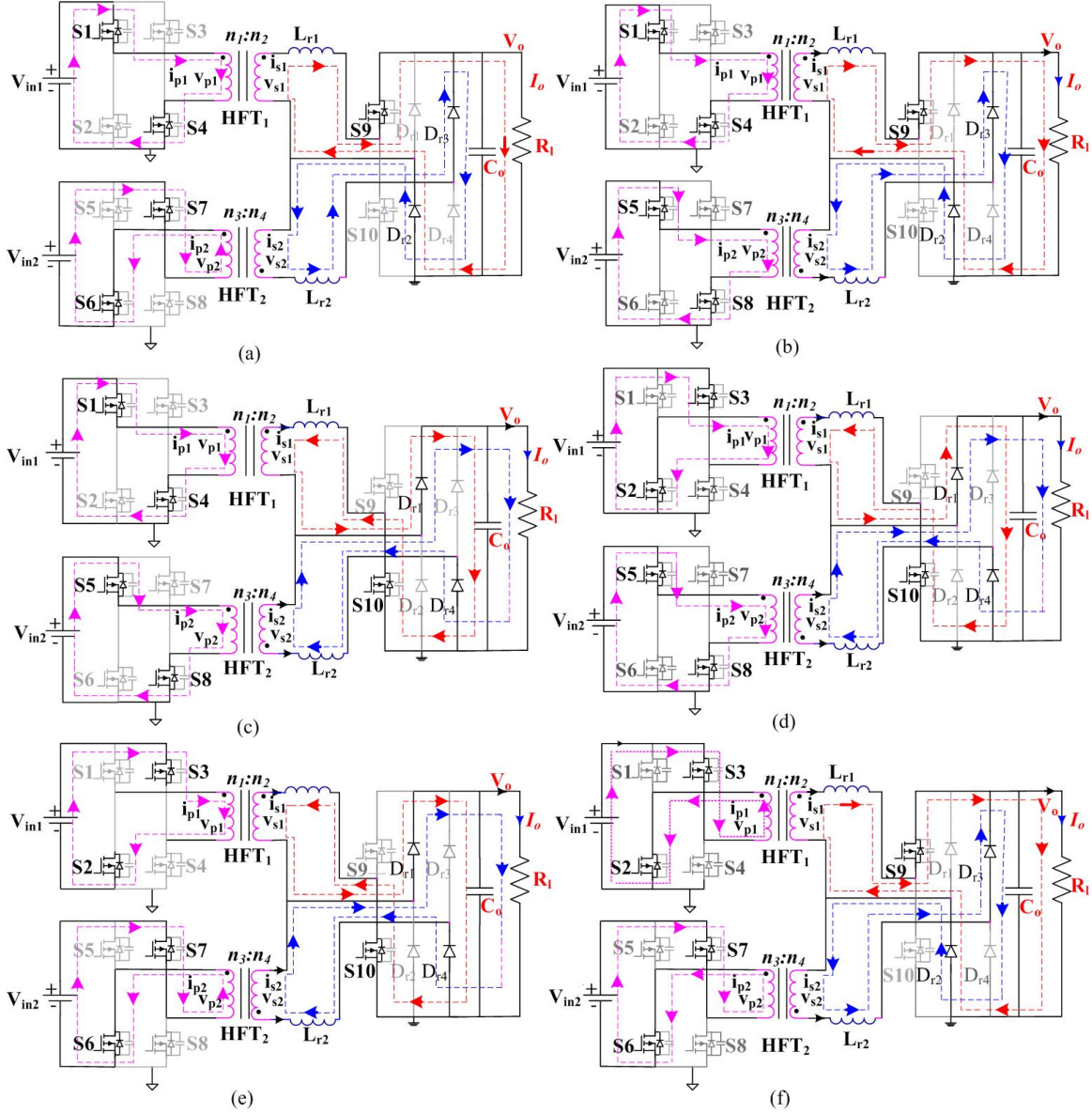


Figure 3.15: Equivalent circuits depicting the closed loop current paths for the primary and secondary of HFTs during different intervals of operation of the modified modular dual-input converter (a) interval ($t_0 < t < t_1$) (b) interval ($t_1 < t < t_2$) (c) interval ($t_2 < t < t_3$) (d) interval ($t_3 < t < t_4$) (e) interval ($t_4 < t < t_5$) (f) interval ($t_5 < t < t_6$)

$$i_{s2}(t) = ((-nV_{in2}) + V_o/(L_{r2}))(t - t_o) + i_{s2}(t_o) \quad (3.14)$$

Where i_{s1} , i_{s2} are secondary current of HFT₁ and HFT₂ respectively. V_{in1} and V_{in2} are input voltages of each module, n is HFT ratio ($n = n_2/n_1$), L_{r1} and L_{r2} equivalent

leakage Inductance value, V_o is the output voltage and $i_{s1}(t_0)$ is the initial current that will be present before starting of this interval.

Interval 2 ($t_1 < t < t_2$)

As shown in Fig. 3.14, at instant t_1 , S6 and S7 are turned OFF and secondary voltage v_{s2} changes its polarity from negative to positive. The closed loop path of input current i_{p2} changes from S6, S7 to D5 and D8 respectively. The switches S5, S8 are turned ON at zero voltage once i_{s2} becomes zero. The closed loop current path for primary and secondary winding for this interval is shown in Figure 3.15 (b). The secondary current expression for the interval can be obtained from steady state analysis and can be represented as

$$i_{s1}(t) = ((nV_{in1}) + V_o/(L_{r1}))(t - t_2) + i_{s1}(t_1) \quad (3.15)$$

$$i_{s2}(t) = ((nV_{in2}) + V_o/(L_{r2}))(t - t_2) + i_{s2}(t_1) \quad (3.16)$$

Interval 3 ($t_2 < t < t_3$)

This interval begins at instant at t_2 when switch S9 is OFF and the secondary voltage V_{ab} shifts from negative to positive polarity. The path for secondary current i_{s1} changes from S9 to D10. When current i_{s2} comes to zero, switch S10 gets turned ON. Figure 3.15 (c) shows the closed loop current path for primary and secondary winding of HFT during this interval. The expression for secondary current for this interval can be represented as

$$i_{s1}(t) = ((nV_{in1}) - V_o/(L_{r1}))(t - t_1) + i_{s1}(t_2) \quad (3.17)$$

$$i_{s2}(t) = ((nV_{in2}) - V_o/(L_{r2}))(t - t_1) + i_{s2}(t_2) \quad (3.18)$$

Interval 4 ($t_3 < t < t_4$)

During this interval at the instant at t_3 , S1 and S4 are turned OFF and secondary voltage v_{s1} changes its polarity from positive to negative. The path of input current i_{p1} changes from S1, S4 to D2 and D3 respectively. Thus, it leads switches S2 and S3 to turn ON at zero voltage once i_{s1} becomes zero. The paths for the primary

and secondary currents of HFT in closed loop condition during these intervals are shown in Figure 3.15 (d). The secondary current expression for the interval can be represented as

$$i_{s1}(t) = ((nV_{in1}) + V_o/(L_{r1}))(t - t_3) + i_{s1}(t_3) \quad (3.19)$$

$$i_{s2}(t) = ((nV_{in2}) - V_o/(L_{r2}))(t - t_3) + i_{s2}(t_3) \quad (3.20)$$

Interval 5 ($t_4 < t < t_5$)

During this interval S2, S3 and S6 and S7 will be ON and the power will flow to load via S10, Dr1 and D_{r4} . The current path of i_{p2} changes from positive to negative polarity. The closed loop paths for the primary and secondary currents of HFT during these interval is shown in Figure 3.15 (e). The secondary current expression can be represented as

$$i_{s1}(t) = ((nV_{in1}) + V_o/(L_{r1}))(t - t_4) + i_{s1}(t_4) \quad (3.21)$$

$$i_{s2}(t) = ((nV_{in2}) + V_o/(L_{r2}))(t - t_4) + i_{s2}(t_4) \quad (3.22)$$

Interval 6 ($t_5 < t < t_6$)

Similarly, at this instant at t_5 switch S10 is OFF and voltage V_{ab} shifts from positive to negative. The path for secondary current i_{s2} changes from S10 to D9. When current i_{s2} comes to zero at zero voltage, switch S9 turns ON. Fig. 3.15 (f) shows the closed loop path for current flow for this interval. The expression for secondary current for this interval is represented as

$$i_{s1}(t) = ((nV_{in1}) - V_o/(L_{r1}))(t - t_5) + i_{s1}(t_5) \quad (3.23)$$

$$i_{s2}(t) = ((nV_{in2}) - V_o/(L_{r2}))(t - t_5) + i_{s2}(t_5) \quad (3.24)$$

3.3.2 Power and Voltage Relation of the Developed Converter

The simplified equivalent circuit with HFT secondary winding voltages is shown in Fig. 3.16 in which, v_s and v_{os} signifies the secondary voltage of HFT and the AC voltage of the secondary side semi active full-bridge rectifier. L_r represent the transformer leakage inductance of HFT.

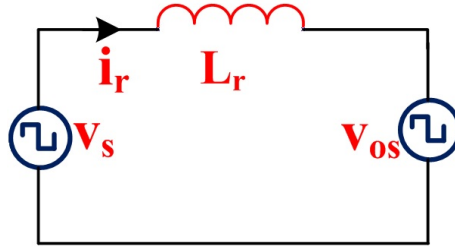


Figure 3.16: Equivalent circuit diagram for secondary winding voltage

The relation between voltage v_s and v_{os} and current is can be obtained by applying KVL as

$$L_r \frac{\partial i_r}{\partial t} = v_s - v_{os} \quad (3.25)$$

By simplifying equation (3.25) and applying volt-second balance principle, the approximated average current I_{avg} of secondary current is can be obtained as

$$I_{avg} = \frac{1}{2f_s L_r} D(1 - D)V_o \quad (3.26)$$

where D is the phase shift ratio for input modules and V_o is output voltage, f_s is switching frequency and L_r is leakage inductance. By using equation (3.26) and substituting I_{avg} , Power can be calculated as

$$P_o = V_o I_o \quad (3.27)$$

Where,

$$\frac{V_o}{V_{in}} = \frac{n_2}{n_1} = n \quad (3.28)$$

$$V_o = nV_{in} \quad (3.29)$$

Substituting V_o in equation (3.27) we get

$$P_o = nV_{in}I_{avg} \quad (3.30)$$

Where I_{avg} is secondary current of HFT, substituting I_{avg} in equation (3.30) output power expression can be represented as

$$P_o = (nV_{in}) \left(\frac{1}{2f_s L_r} \right) D(1-D)V_o \quad (3.31)$$

Where P_o is output power and D is phase shift ratio, f_s is switching frequency, V_{in} is input voltage. If a resistive load R_L is considered as load then, we have

$$P_o = \frac{V_o^2}{R_L} \quad (3.32)$$

By equating equation (3.31) and (3.32) we get output voltage given by

$$V_o = \frac{nV_{in}R_L}{2f_s L_r} D(1-D) \quad (3.33)$$

It can be witnessed from equation (3.33) that the output voltage can be restrained by regulating the phase shift ratio D between the AC voltages of its full-bridge converters. Average current for both the modules can be derived from equations (3.13)-(3.24). By considering modified modular based dual-input converter configuration the average current equation for each module can be represented by equations (3.34) and (3.35)

$$I_{avg1} = \frac{n}{2f_s L_{r1}} D_{13}(1-D_{13}) \quad (3.34)$$

$$I_{avg2} = \frac{n}{2f_s L_{r2}} D_{23}(1-D_{23}) \quad (3.35)$$

Where D_{13} and D_{23} are the phase shift ratio between each modules and L_{r1} , L_{r2} are leakage inductance of respective modules. By avoiding the losses of active devices and HFTs, the total supplied power by both the energy sources at the output module

can be illustrated as

$$P_1 = nV_{in1}I_{avg1} \quad (3.36)$$

and

$$P_2 = nV_{in2}I_{avg2} \quad (3.37)$$

By substituting equation (3.34) and (3.35) the power for each module can be represented by

$$P_1 = \frac{nV_{in1}V_o}{2f_s L_{r1}} D_{13}(1 - D_{13}) \quad (3.38)$$

$$P_2 = \frac{nV_{in2}V_o}{2f_s L_{r2}} D_{23}(1 - D_{23}) \quad (3.39)$$

The total power consumed by each module can be represented by equation (3.40)

$$P_o = P_1 + P_2 \quad (3.40)$$

$$P_o = \frac{V_o}{2f_s} \left[\frac{nV_{in1}D_{13}(1 - D_{13})}{L_{r1}} + \frac{nV_{in2}D_{23}(1 - D_{23})}{L_{r2}} \right] \quad (3.41)$$

By considering two input, output voltage can be obtained by equating equations (3.31) and (3.41) considering resistive load as R_L

$$V_o = \frac{nR_L}{2f_s} (V_{in1} + V_{in2}) \quad (3.42)$$

$$V_o = \frac{R_L}{2f_s} \left[\frac{nV_{in1}D_{13}(1 - D_{13})}{L_{r1}} + \frac{nV_{in2}D_{23}(1 - D_{23})}{L_{r2}} \right] \quad (3.43)$$

Where n is turns ratio where $n = n_2/n_1$, D_{13} and D_{23} are phase shift ratio between each module, L_{r1} and L_{r2} is leakage inductance of HFT₁ and HFT₂ respectively. It can be observed from equation (3.43) that the output voltage variation is with respect to the phase shift ratios (D_{13} and D_{23}) for different source voltages and load resistance.

3.3.3 Soft Switching Operation for the Developed Converter

Fig. 3.14 shows the key waveforms for steady-state voltage and current waveform for zero voltage switching. Considering before turn ON of switch S1 the primary input current i_{p1} will be negative as shown in Fig. 3.17. Once S2 is turned OFF, C1 the parasitic capacitance of switch S1 that will be present across switch will discharges from V_{in1} to zero. At the same time C2 the parasitic capacitance across S2 will start charging from zero to V_{in1} . As input current i_{p1} is negative, it freewheels through an antiparallel diode D1 of switch S1 once the process of charging and discharge is finished. As, S1 is accommodated with turn ON gate signal from the controller it

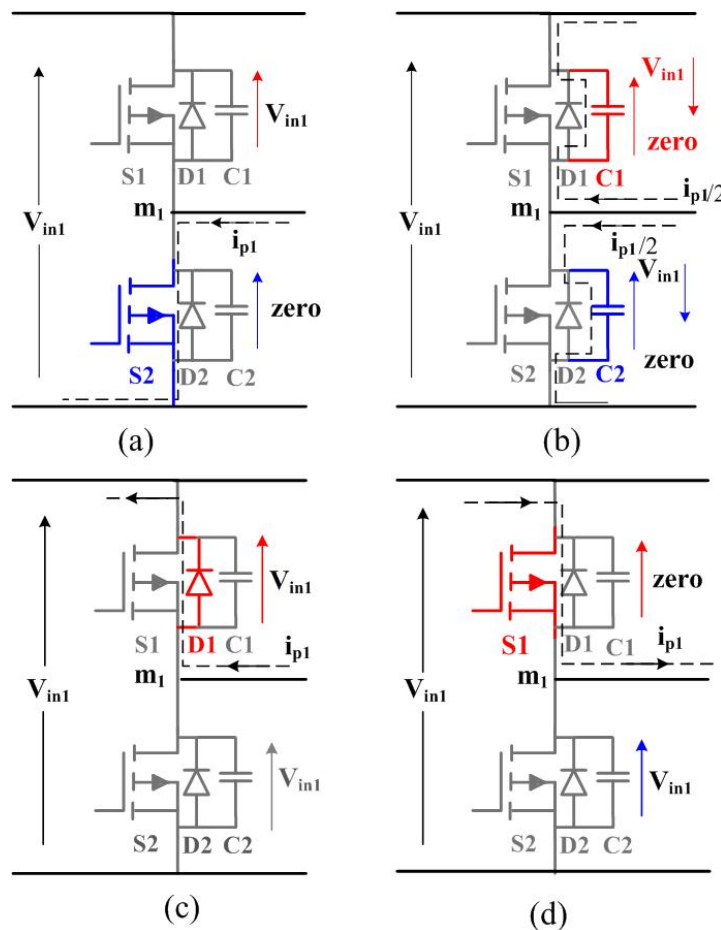


Figure 3.17: ZVS operation of S1 (a) Instant before turn on of switch (b) Charging and discharging process of C1 and C2 (c) Freewheeling of diode (d) Current changing path and conduction of switch S1.

starts conducting at zero voltage as soon as i_{p1} alternates its polarity. In the same

way all other switches also turn ON with ZVS. The conditions needed for switches of modified converter configuration for ZVS is listed in Table 3.2.

Table 3.2: Conditions for ZVS operation of switches

Input Module	Switches	Conditions
V_{in1}	S1,S2,S3,S4	$i_{s1}(t_o) < 0, i_{s1}(t_3) < 0$
V_{in2}	S5,S6,S7,S8	$i_{s2}(t_1) < 0, i_{s2}(t_4) < 0$
Semi active Rectifier	S9,S10	$i_{s1}(t_2) < 0, i_{s2}(t_5) < 0$

It can be observed that from the steady state waveforms that ZVS for input converter switches S1-S4 can be achieved only when $i_{s1}(t_o)$ and $i_{s2}(t_3)$ is less than zero. Similarly, for the other module converters ZVS can be achieved at conditions listed in Table 3.2. For proper understanding of ZVS operation we have considered both the input full-bridge converters are in phase and are fed from identical sources then the following expression can be achieved by evaluating the steady state waveform as,

$$i_{s1}(t_o) = i_{s2}(t_1), i_{s1}(t_1) = i_{s2}(t_2) = I_2 \quad (3.44)$$

and the expression for I_1 and I_2 can be derived. Where I_1 and I_2 are average currents for each module. Hence, I_1, I_2 can be expressed as

$$I_1 = \frac{1}{4\pi f_s L_r} (1 - 2D)V_o - nV_{in} \quad (3.45)$$

$$I_2 = \frac{1}{4\pi f_s L_r} (2D - 1)nV_{in} + V_o \quad (3.46)$$

Where D is phase shift ratio, I_1, I_2 are average currents of module1 and module 2 respectively. Then by substituting equation (3.45)-(3.46) in output voltage equation and constrained listed in Table 3.2, we get following relation

$$M \leq \frac{1}{1 - 2D}, M \geq (1 - 2) \quad (3.47)$$

Where, M represent the voltage gain that is given by

$$M = \frac{V_o}{nV_{in}} \quad (3.48)$$

3.3.4 Design of the Modified Modular Dual-Input Full-Bridge DC-DC Boost Converter

Here, the design for modified dual-input converter configuration is illustrated with the following specifications:

- Input Voltage $V_{in1} = 48$ V
- $V_{in2} = 230$ V,
- Output voltage $V_o = 300$ V,
- Power $P_{in1} = 2$ kW, $P_{in2} = 1$ kW,
- Total Power $P_o = 3$ kW,
- switching frequency $f_s = 20$ kHz.

The design equations are represented to decide the component rating. It benefits in proper selection of components as well as forecast the performance of the modified converter analytically.

1. Average input current of module 1 is P_o/V_{in1} , considering the efficiency to be 90%, $I_{in1} = 46.2$ A. Similarly, for the second module $I_{in2} = 4.83$ A. output current is $I_o = 10$ A for 3 kW power.
2. Average input secondary current of module 1 and module 2 can be found by equation (3.34) and (3.35) for each modules, $I_{avg1} = 6.64$ A considering D_{13} is 0.4 and leakage inductance is 14.5μ H. Similarly, for the second module $I_{avg2} = 3.33$ A considering $D_{23} = 0.4$ and leakage iductance $L_{r2} = 30 \mu$ H.
3. Design of HFT: The design of HFT includes the selection of frequency, core and turns ratio. Therefore, switching frequency of $f_s = 20$ kHz is selected for the operation of the converter. Primary inductance of HFT is calculated as $L_{p1} = 205.2 \mu$ H and $L_{p2} = 14.8$ m H. Similarly, secondary inductance of HFT is calculated as $L_{s1} = 20.52$ mH and $L_{s2} = 20.52$ mH by considering the Al value from core specification. Number of primary and secondary turns are $n_1 = 6$ turns, $n_2 = 51$ turns and $n_3 = n_4 = 60$ turns respectively, which is required for the modified modular dual-input converter to step down voltage.
4. Leakage inductance L_{r1} and L_{r2} of HFT can be calculated using equaion (3.49)

$$L_r = L_{r1} = L_{r2} = \frac{nR_l}{2f_s V_o} D(1 - D) \quad (3.49)$$

Where n is turns ratio found to be 0.16, R_l is load, D is phase shift ratio. So, L_{r1} is found to be $14.5 \mu\text{ H}$ and L_{r2} is found to be $30 \mu\text{ H}$. D is considered as 0.4.

5. Parasitic Capacitance (C_r): Parasitic resonance is caused by parasitic components present in the circuit i.e the capacitor connected across each switch. Condition of zero voltage switching is given by

$$2\pi\sqrt{(L_r C_r)} = (1 - D)T_s \quad (3.50)$$

The value of capacitor across the switch can be obtained by equation (3.51)

$$C_r = \frac{1}{L_r} \left(\frac{(1 - D)T_s}{2\pi} \right)^2 \quad (3.51)$$

Where, L_r is leakage inductance and C_r is capacitance across each switch.

3.3.5 Control Scheme for Modified Modular Dual-Input Boost Converter

To regulate the desired output voltage and to sustain the powers flowing from the source to load, a closed loop control strategy for modular dual-input converter configuration is presented in this section. Fig. 3.18 shows the schematic for the control strategy of modular dual-input converter. It can be perceived from equation (3.41) and (3.43) that phase shift ratios D_{13} and D_{23} plays a vital role in regulating output voltage V_o . Consequently, the powers supplied from the different energy sources and the output voltage can be regulated by varying D_{13} and D_{23} . An appropriate control strategy is required for proper voltage regulation of the modified modular dual-input converter configuration. The implementation of digital control is a viable option that gives robust and precise control performance. The voltage control algorithm has been implemented using FPGA board. The control scheme consist of sensor gain, 12 bit A/D converter, two current compensator, one voltage compensator and has two phase shift driver circuit and modulator (VCO). I_{p1} , I_{p2} are actual input currents from both the sources, I_{ref1} and I_{ref2} are reference currents and V_o is rated output voltage and V_{ref} is the reference voltage. Error signal that is fed to current compensators are

generated by comparing actual currents with reference currents. Phase shift control signal D_{13} is addition of voltage control signal v_c and current control signal i_{c1} similarly D_{23} is addition of voltage control signal v_c and current control signal i_{c2} . The phase shift percentage gate signal for each input can be determined by D_{13} and D_{23} that are given to phase shift drivers. By proper fine tuning of phase shift percentage with suitable current control signals the output voltage regulation can be obtained and balanced power flow from source to load can be achieved.

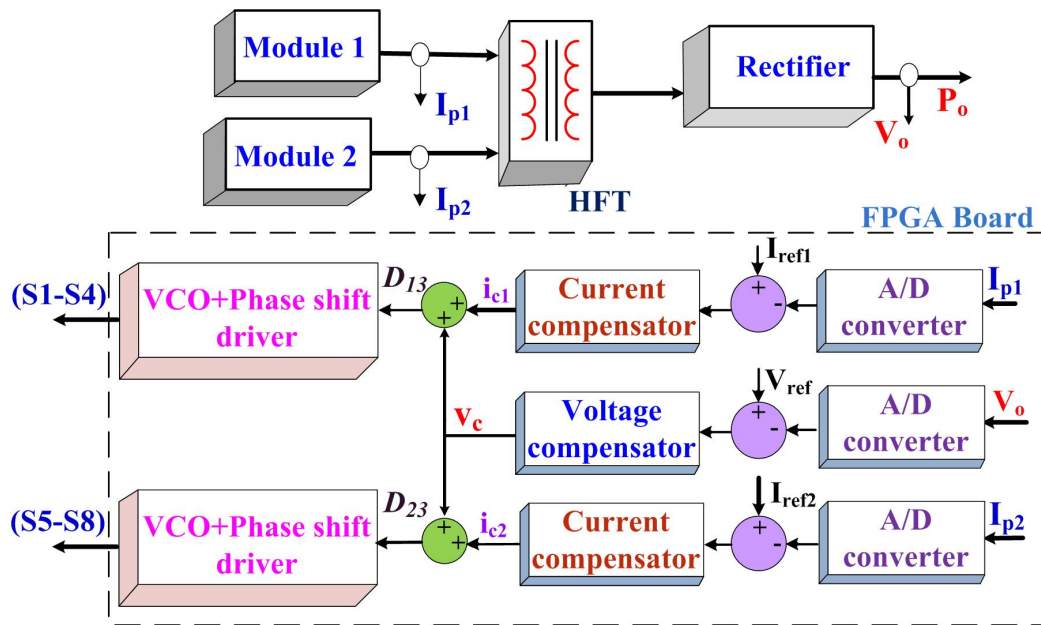


Figure 3.18: Control strategy for the developed modified dual-input DC-DC converter.

3.3.6 Results and Discussion

The modified modular dual-input converter configuration is designed for 300 V and 3 kW power. The battery is charged for 48 V. The simulation of the modified modular based converter topology has been done in MATLAB environment. Fig. 3.19 - 3.24 illustrates the simulated waveforms of the proposed modified dual-input converter configuration. Fig. 3.19 shows the waveforms of primary and secondary voltages of both HFTs. Voltage v_{p1} and v_{s1} are voltage waveform of HFT₁ and voltage v_{p2} and v_{s2} are voltage waveforms of HFT₂ respectively. The resulted waveform shows that input primary voltages of both the HFTs are different and secondary waveforms shows

that the voltage is stepped up to 300 V. Fig. 3.20 shows the gate signals V_{gs1} applied to switch S1 and voltages across these switch V_{DS1} . From figure it can be observed that during the turn-on instants of switch S1 that satisfy the ZVS conditions. Fig. 3.21 shows the input and output current waveform of HFT₁.

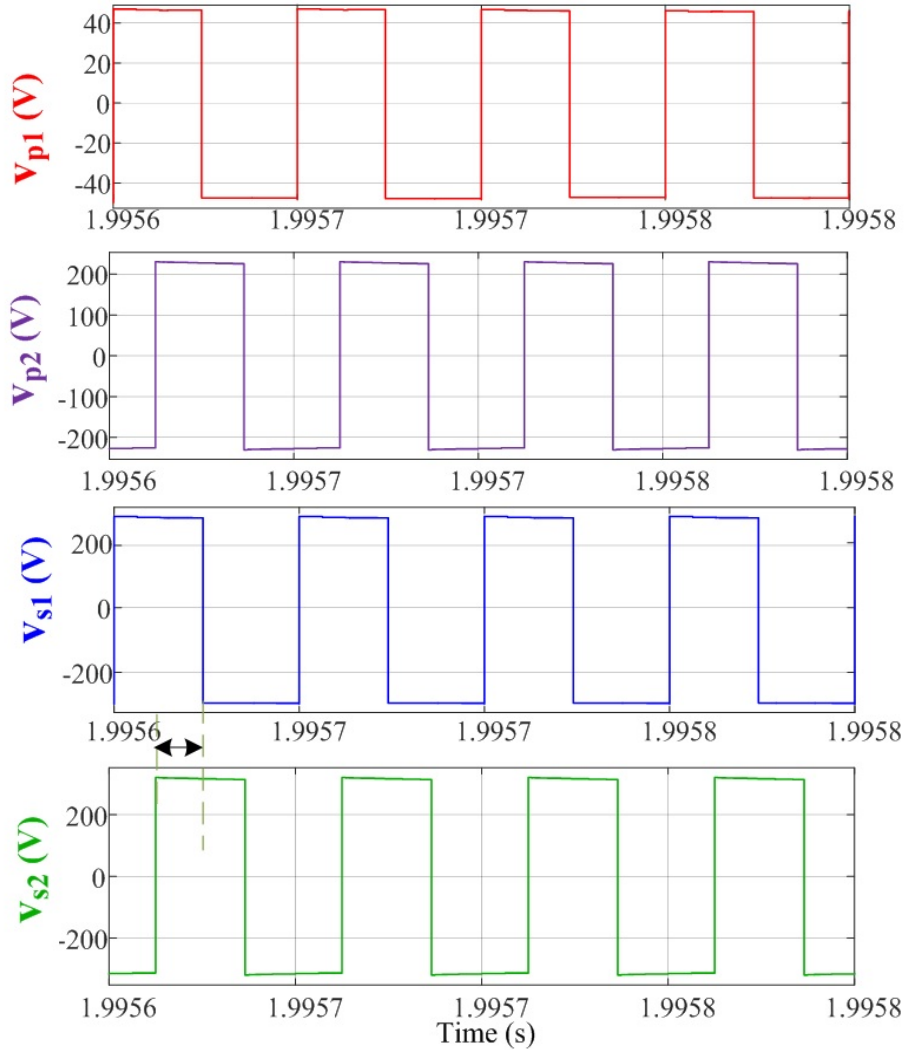


Figure 3.19: Simulated waveform of Voltage of HFTs (V_{p1} , V_{p2}) primary voltages and (V_{s1} , V_{s2}) secondary voltages of HFT₁ and HFT₂ respectively.

Fig. 3.22 (a) shows the secondary voltage of HFT₁ and voltage across one bridge of semi active bridge rectifier. Fig. 3.22 (b) shows the voltage across inductor L_{r1} . It can be observed that voltage across inductor is $nV_{in1}+V_o$ as shown in Fig. 3.22. The dynamic behaviour of the modified modular dual-input converter configuration has

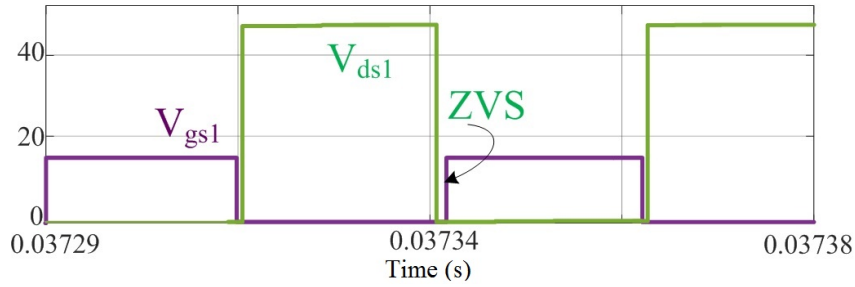


Figure 3.20: Simulated waveform of ZVS turn on operation of Switch S1 and gate pulse of S1.

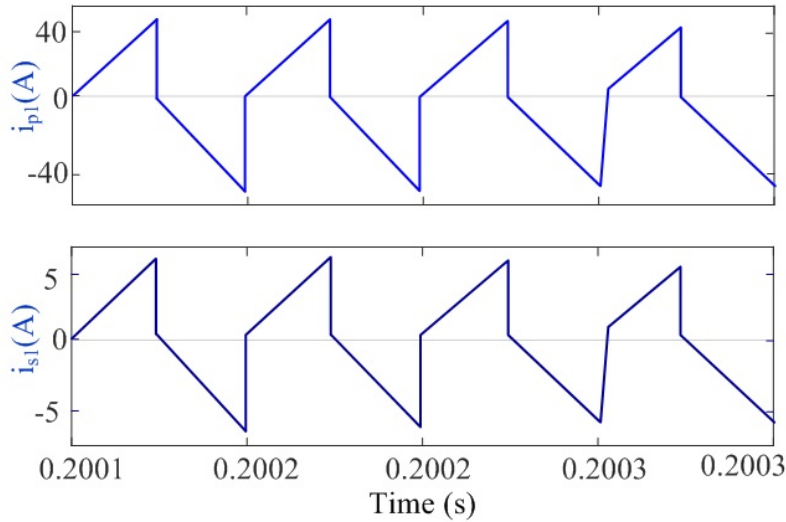


Figure 3.21: Simulated waveform of input i_{p1} and output current i_{s1} waveform of HFT₁

been deliberate by switching the load from steady state condition. Fig. 3.23 shows the rectified DC voltage V_o and current I_o . The resulted waveform shows ripple free constant voltage of 300 V remains to be constant irrespective load change. It shows the dynamic behavior under step load condition from half to full load condition with proper voltage regulation. Fig. 3.23 shows the ripple free output voltage and current waveform of modified converter. Fig. 3.24 shows the simulated waveform of power sharing between each module. It clearly shows that the power is properly shared between each modules and 3 KW power is provided to load.

To examine and justify the feasible operation of modified modular dual-input converter configuration a laboratory prototype is developed for 1 kW power. The test is conducted for both load and charging the battery FPGA board is used to

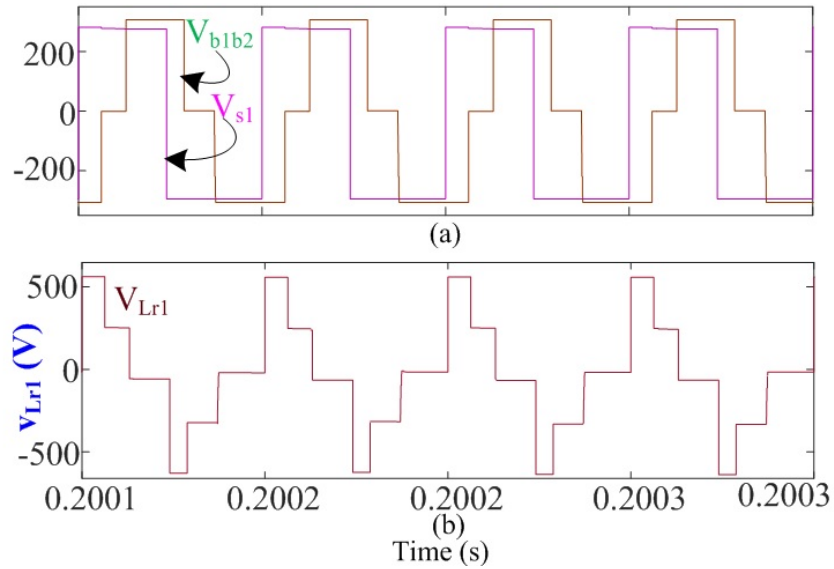


Figure 3.22: Simulated waveform of output voltage of full-bridge rectifier at HFT₁ with voltage across one full-bridge rectifier.

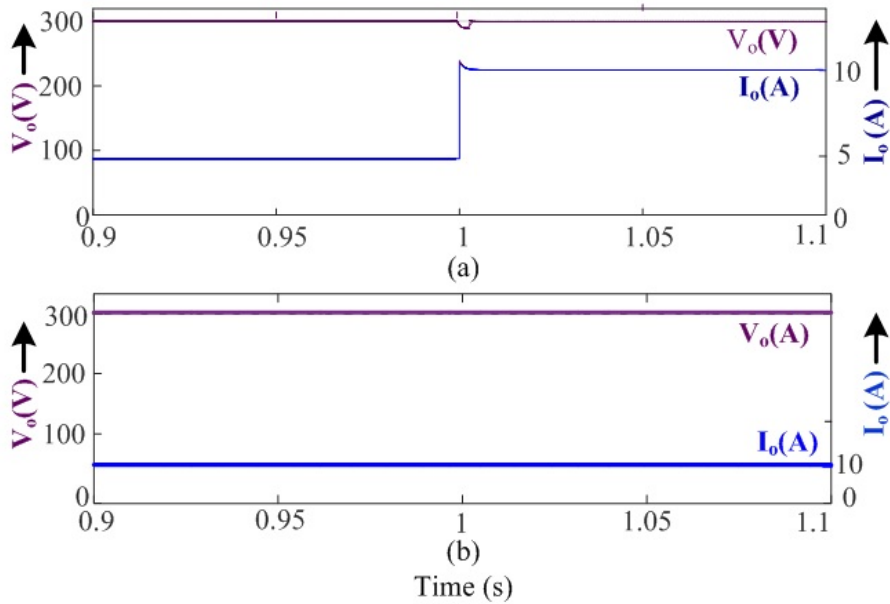


Figure 3.23: Simulated waveform of (a) dynamic behavior under step load condition (b) Output voltage and current for 3 kW load.

implement the control algorithm of the modified modular dual-input converter configuration. One of the converter input is connected to 48 V/5.2 A current and the other converter is connected from 230 V/4.0 A source. Fig. 3.25 (a) shows the in-

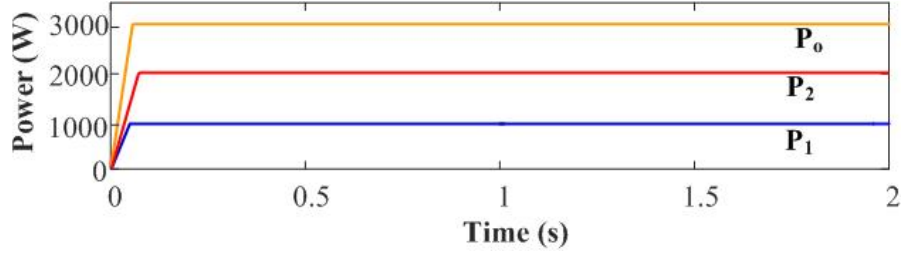


Figure 3.24: Simulation waveform of power sharing of the presented converter

put voltage/current waveform of input source1 and Fig. 3.25 (b) shows the input voltage/current waveform of source 2. Fig. 3.26 (a) and (b) shows the experimental voltage waveform of both the HFTs. The resulted waveform shows that both HFTs secondary are stepped up to 300 V.

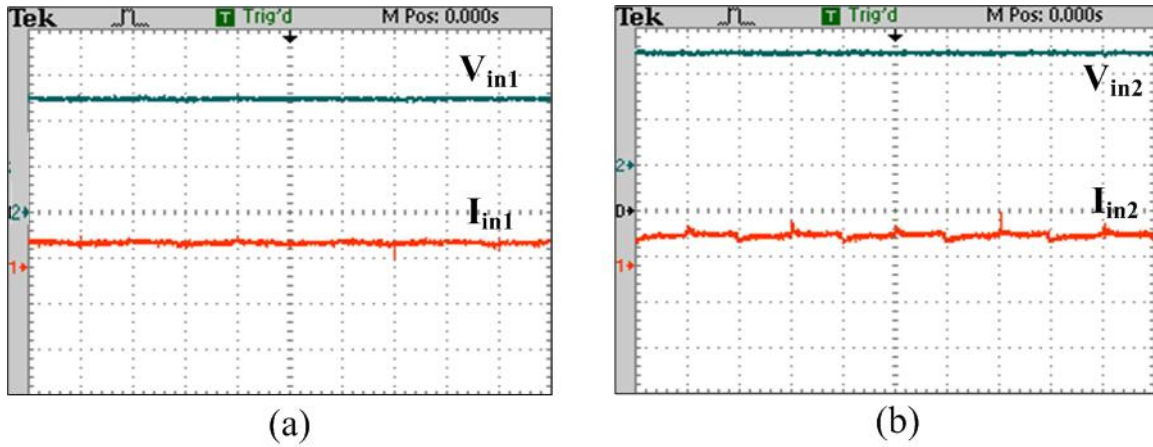


Figure 3.25: Experimental waveforms of (a) Input voltage (20 V/div) and current (10 A/div) of source 1. (b) Input voltage (100 V/div) and current (5 A/div) of source 2.

It can be seen that voltage v_{s1} and v_{s2} are lagging by input voltage v_{p1} and v_{p2} respectively. It indicates the power flow between input ports to output port. Fig. 3.27 shows experimental waveforms of voltage and current of HFTs.

Fig. 3.27 (a) shows the current waveforms of both the modules. It justifies that the power is properly shared between two ports and voltage is regulating appropriately. Fig. 3.27 (b) shows the input waveform of voltage and current of HFT₁. It can be observed that the input voltage is 230 V and current is shared properly. Fig. 3.28 shows the waveform of ZVS operation of switches S1 and S2. The gate signals (V_{GS1} and V_{GS2}) applied to switches S1 and S2, the voltages across these switches (V_{DS1}

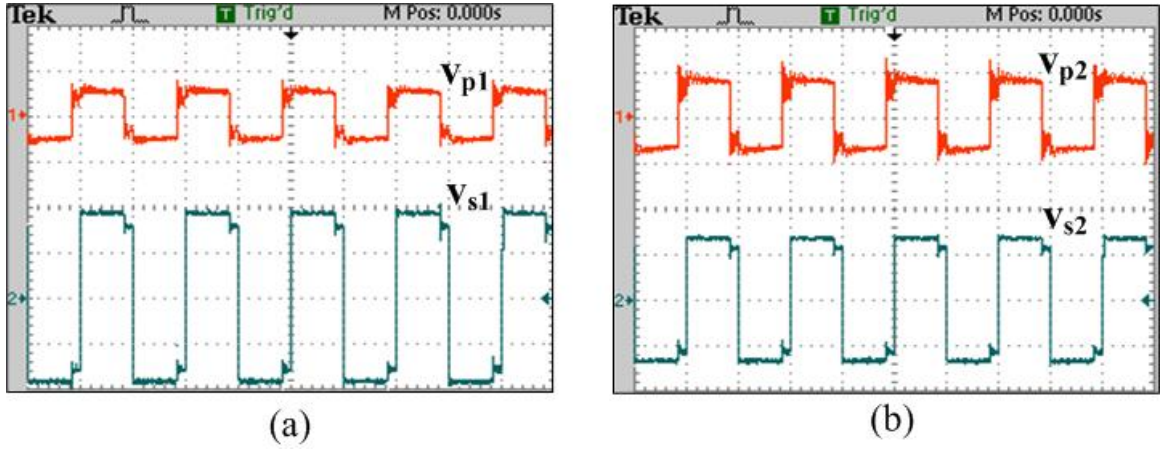


Figure 3.26: Experimental waveforms of (a) Voltage waveforms of HFT1 ($v_{p1}=100\text{V/div}$, $v_{s1}= 100\text{V/div}$) (b) HFT₂ ($v_{p2}=500\text{ V/div}$, $v_{s2}= 200\text{V/div}$).

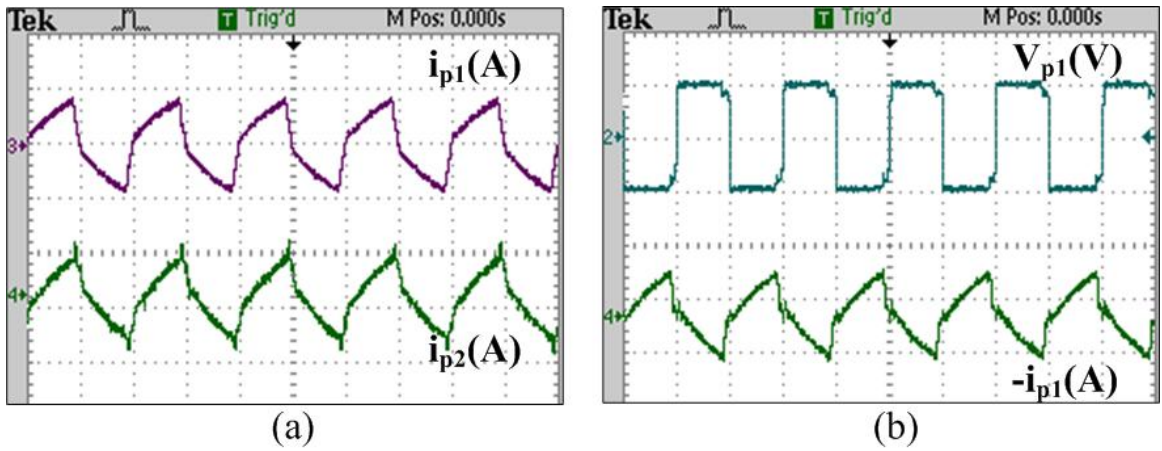


Figure 3.27: Experimental waveforms of (a) input current i_{p1} and i_{p2} . (b) Voltage and current of HFT1 primary ($v_{p1}=50\text{V/div}$).

and V_{DS2}), and input current i_{p1} is shown in Fig. 3.28 (b). It can be observed that, the currents $i_{p1} < 0$, during the turn-on instants of S1 and S2, respectively, which satisfy the ZVS conditions. Similarly, Fig. 3.29 shows the experimental waveform of ZVS operation of S3 and S4. Fig. 3.29 (b) it shows that current $i_{p1} > 0$, during turn of switch S7 that satisfy the ZVS condition. Fig. 3.30 shows the ZVS operation waveform of switches S5 and S7. Fig. 3.31 (a) and (b) shows the waveform of secondary voltage and current i_{s1} and i_{s2} respectively. This justifies the zero circulating of secondary rectifier. Fig. 3.32 (a) shows the experimental waveforms of ripple free DC output voltage and current waveform. It shows that voltage 300 V remains con-

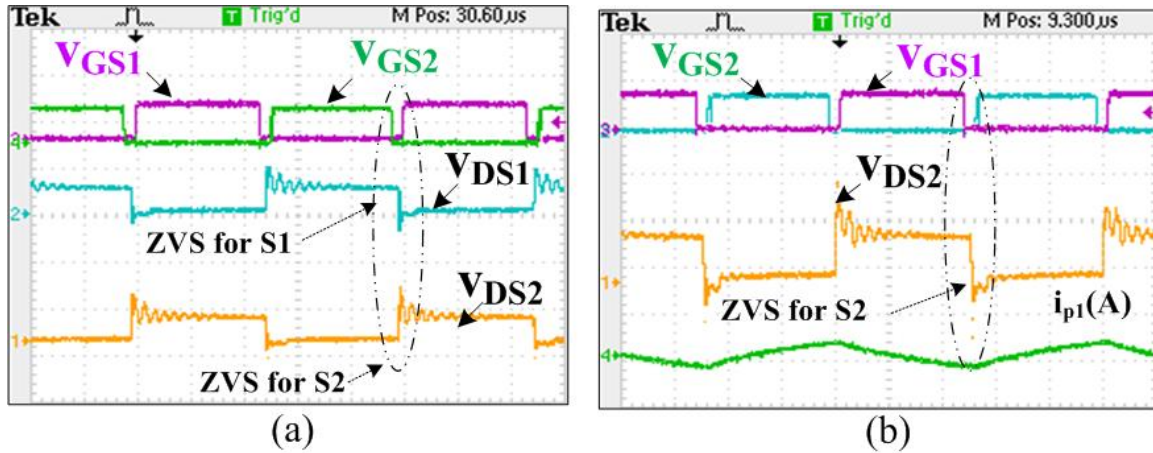


Figure 3.28: ZVS operation of switch S1 and S2 of module 1.

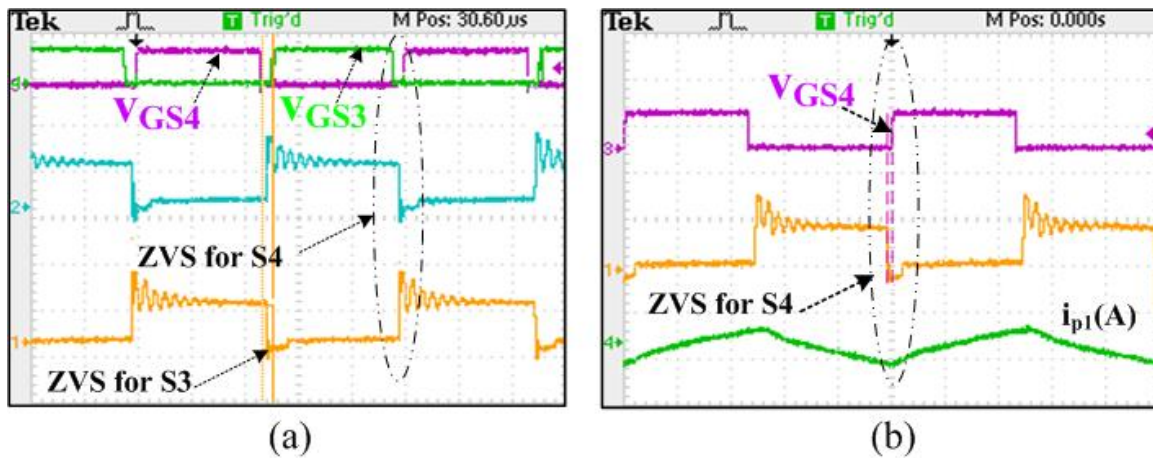


Figure 3.29: ZVS operation of switch S3 and S4 of module 1 with input current waveform.

stant and currents are shared between the load and battery charging. Fig. 3.32 (b) shows the experimental waveforms of dynamic behaviour under step load condition.

The waveform shows that voltage V_o remains to be constant irrespective of load changes and currents are varied accordingly. Fig. 3.33 (a) shows the experimental waveform of output voltage V_o and output current I_o . It shows the dynamic behavior under step load condition. It can be observed that voltage remains to be constant and current is varying accordingly. Fig. 3.33 (b) shows the experimental waveform of output voltage V_o and input current I_{in1} and I_{in2} . It can be observed that the output voltage remains to be constant when both the source currents are varied. It justifies the proper load sharing and power flow of the proposed converter config-

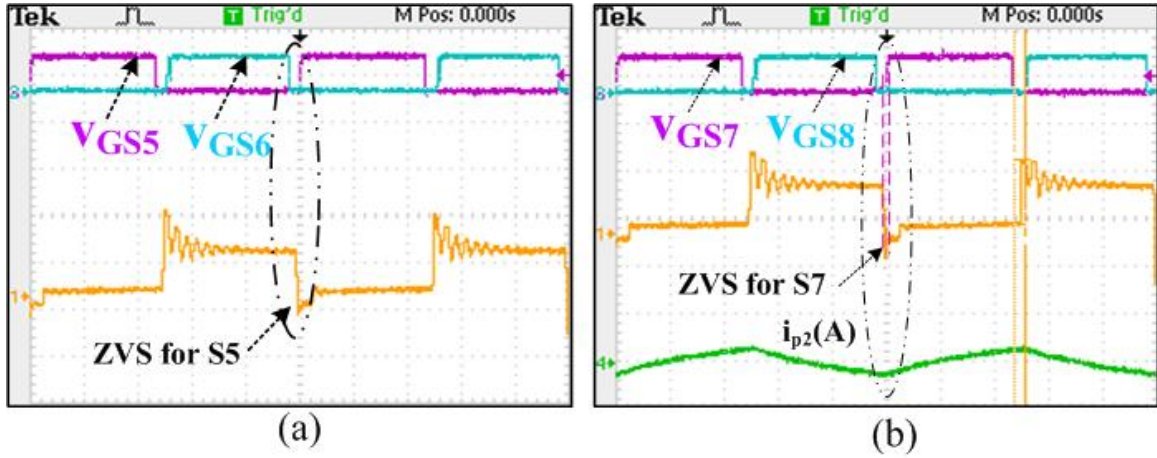


Figure 3.30: ZVS operation of switch S5 and S7 of module 2.

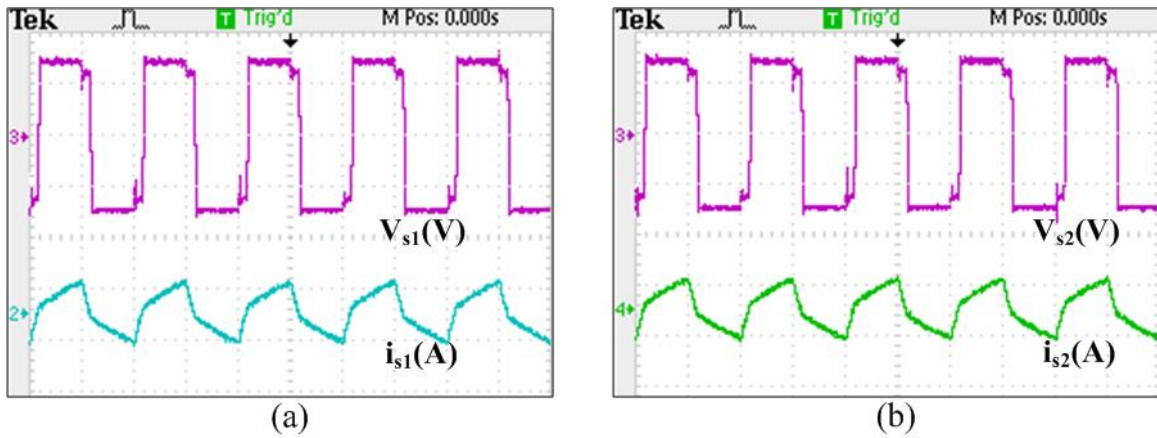


Figure 3.31: Experimental waveforms of (a) secondary voltage/current of HFT₁. (b) Secondary voltage/current of HFT₂.

uration. converter. Fig. 3.34 shows the experimental setup used for validating the proposed modified modular dual input converter with bidirectional DC/DC converter. Similarly, Fig. 3.34 (a) shows the experimental waveform of secondary voltage and current of HFT1 for reduced circulating current at low voltage condition. Similarly, Fig. 3.34 (b) shows the experimental waveform for reduced circulating current at full load condition. It can be observed that at low power rating the circulating current has been reduced significantly by which losses are minimized and aids in improving the efficiency of system. Fig. 3.35 illustrates the experimental set up for modified modular dual-input converter configuration.

It is observed that turn on losses of switches are zero due to ZVS operation. From

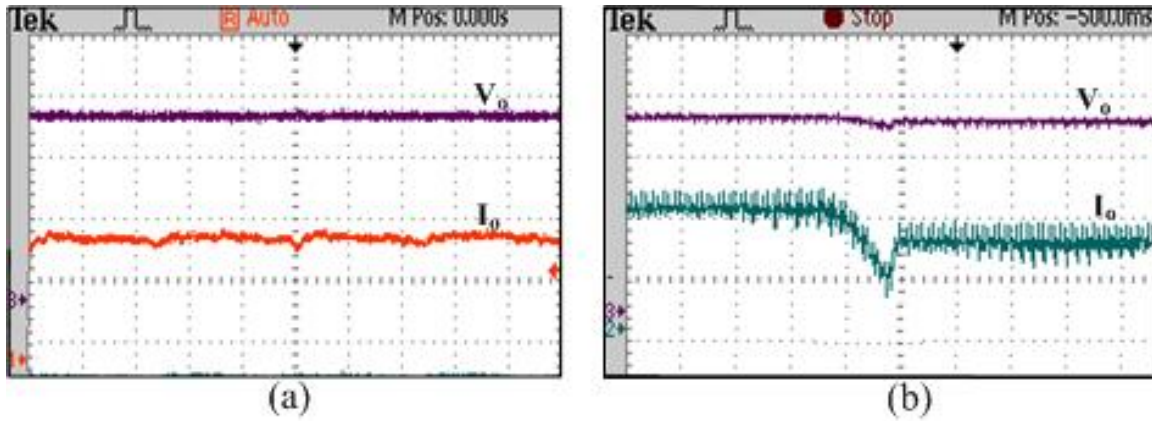


Figure 3.32: Experimental waveforms of (a) output voltage/current. (b) Dynamic behavior under step load conditions.

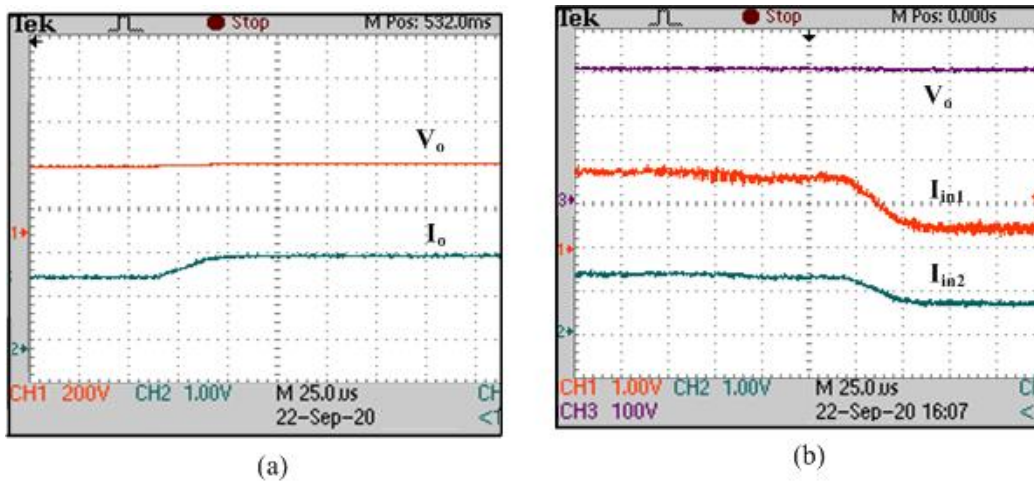


Figure 3.33: Experimental waveforms of (a) output voltage/current under step load condition. (b) Input current (I_{in1}) and (I_{in2}) with output voltage

the simulation and experimental results it is clear that the modified configuration operates smoothly and efficiently with minimum circulating current and proper power sharing of different sources. It is observed that due to semi active rectifier used at secondary rectifier the losses are minimized and achieved efficiency of 92%. Further, it can be reduced by replacing all the diodes with synchronous rectifier.

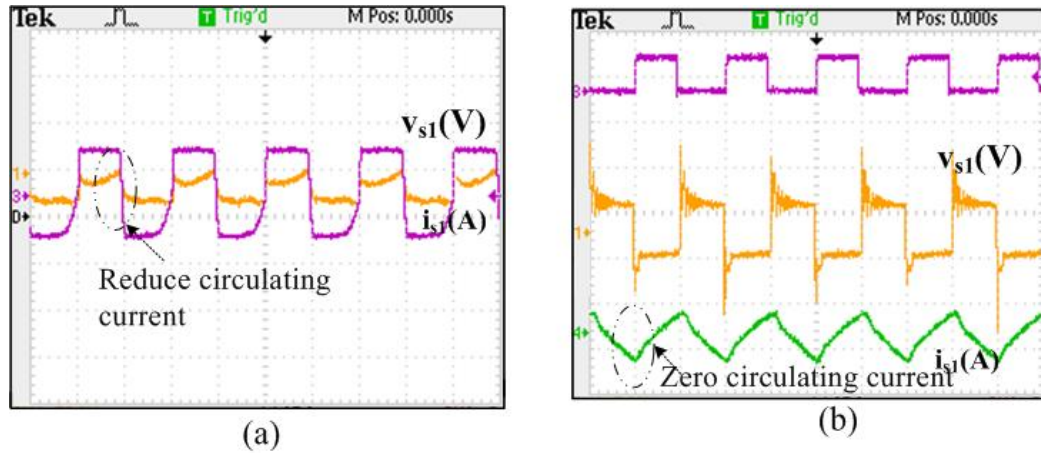


Figure 3.34: Experimental waveforms of (a) voltage and circulating current of HFT₁ at low voltage condition. (b) voltage and circulating current of HFT₁ at full load

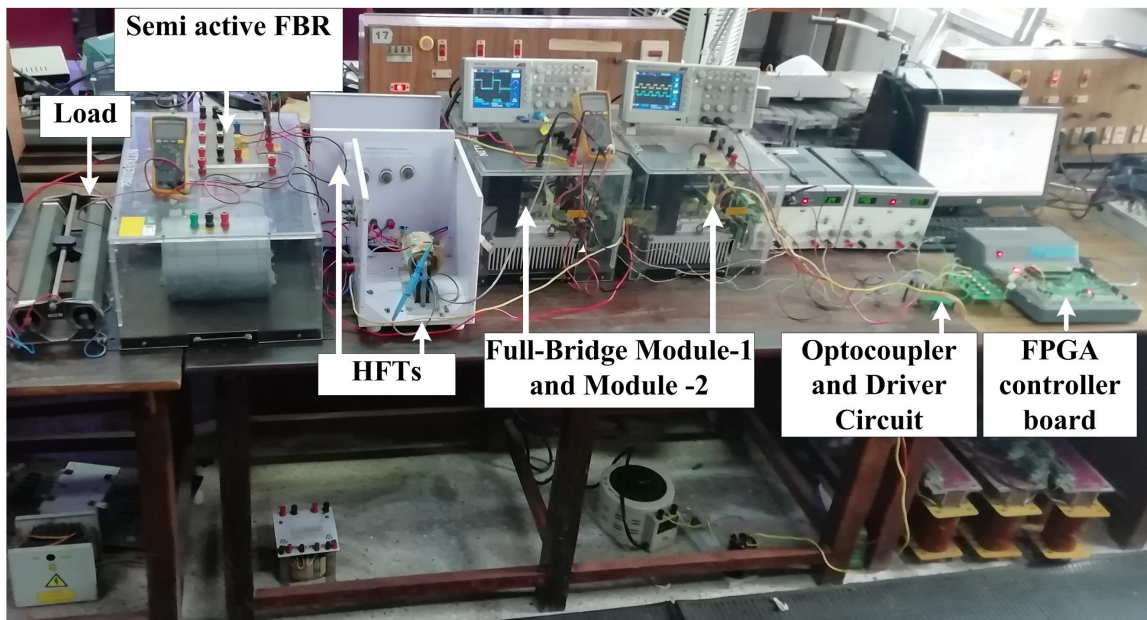


Figure 3.35: Experimental prototype for the modified modular dual input converter

3.3.6.1 Comparison of Developed Topology with Other Dual-Input Topologies

In order to demonstrate the dominance of modified modular dual-input converter configuration over the other presented converter a comparison has been deliberated. Table 3.3 shows the comprehensive comparison of the modified modular dual-input converter configuration topology with other converters. The comparison is made in

terms of component counts, isolation between the circuit, stresses on device with respect to loss consideration for high power application and also the complexity of control strategy has been preferred for the analysis. From the literature it can be observed that all the converter configurations offer dual-input operation, soft-switching, and provides isolation between the source and load.

Table 3.3: Comparison of developed converter with other dual input converters available in the literature

Parameters	Wang et al. 2018	Asa et al. 2015	Lin et al. 2017	Presentedd converter
Input Sources	2	2	2	2
Active devices	12	4	8	10
Passive devices	0	4	12	4
No. of HFTs	1	2	1	2
ZVS	Yes	Yes	Yes	Yes
Isolation between source and load	Yes	Yes	Yes	Yes
Simultaneous power flow	not recommended as $D_{13} \neq D_{23}$	Yes	not recommended	Yes
Isolation between sources	complex	not recommended	complex	simple
Circulating current losses	high	medium	high	low
Controller	complex	complex	complex	moderate

Among these (Asa et al., 2015) configuration structure entails the minimum number of semiconductor devices. However, dual-input operation of this configuration lead to insufficient losses. The three port converter (Wang et al., 2018) needs reduced number of semiconductor components along with less magnetic core and conductor materials as compared to the modified modular dual-input converter configuration and offers most of the requisite features of dual input converters. Conversely, simultaneous power supply from this converter configuration that are connected from two different energy sources leads in considerably higher losses as the windings of HFT gets magnetically short circuited for different values of the phase shift ratios ($D_{13} \neq D_{23}$). This is due to the antiparallel diodes of the accompanying modules that make the conduction paths. Also, due to the presence of leakage inductance considerably higher power circulates between the input-ports. Converter configuration

(Lin et al., 2017) compared to the modified modular dual-input converter configuration offers most of the requisite features of dual-input converters. However, it offers more number of semiconductor devices. Considerably greater losses arise as the windings of HFT are magnetically short circuited for different values of the phase shift ratios. Even though the modified modular dual-input converter configuration consists relatively higher number of semiconductor devices, it permits the input module converters to operate with a wide range of phase delays with respect to the input module converter to achieve wide ranges of the output voltage. Higher power can be achieved with reduced power losses. Further, in the modified modular dual-input converter configuration, isolation between two different sources can be accomplished by applying suitable TURN-OFF and/or TURN-ON gating signals to the particular switches.

3.4 BI-DIRECTIONAL DC-DC CONVERTER FOR BATTERY CHARGING

For charging the battery from 300 V to 48 V and to discharge the battery to meet requirement of load a bidirectional converter is designed with minimum number of switches as shown in Fig. 3.36. It can be observed that it has only two active switches with an inductor to charge the battery and to discharge whenever it's required by load. Here the output voltage is stepped down to charge the battery by using switch

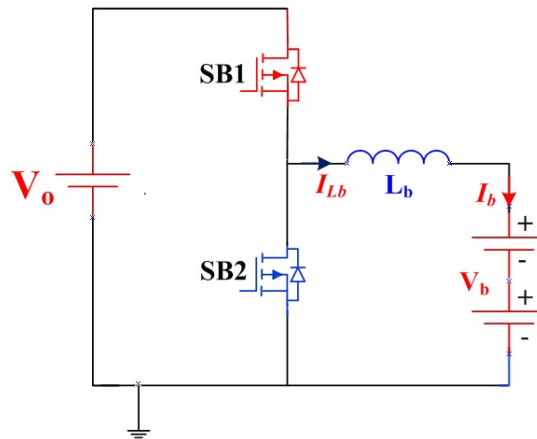


Figure 3.36: Schematic of bidirectional DC-DC Buck-Boost converter.

SB1 and for discharging process of the battery SB2 switch is utilized for the operation.

Here V_o is the output voltage and V_b is the voltage of battery, SB1 and SB2 are two switches used for buck or boosting the voltage.

3.4.1 Operation Principle of Bidirectional Converter

The modes of operation can be divided into two stages that is described in this section. Fig. 3.37 shows the modes of operation during boost and buck operation of the converter.

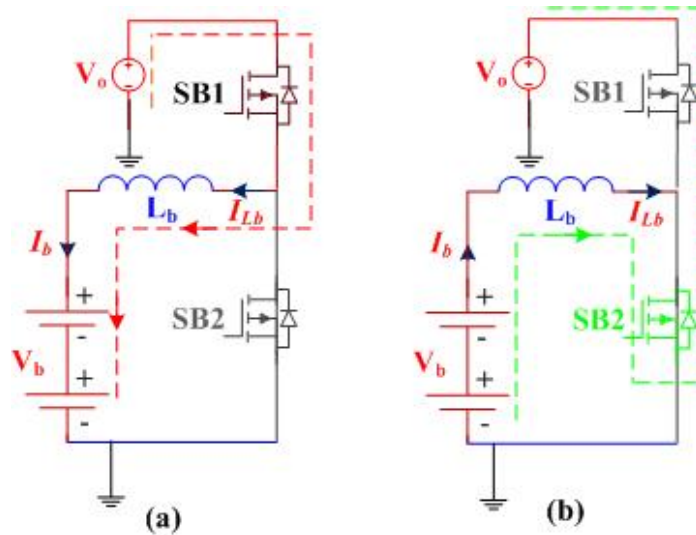


Figure 3.37: Modes of operation of buck-boost converter (a) buck mode (b) boost mode

Charging Mode : At this instant switch SB1 is on and switch SB2 is OFF and the current I_{Lb} flows to battery. The Inductor is designed such that it will avoid maximum current ripple from the output end. The equation of current can be expressed as

$$\frac{di_{lb}}{dt} = \frac{V_o - V_b}{L_b} \quad (3.52)$$

Discharging mode: At this instant SB2 is ON and SB1 is OFF and the current I_{Lb} flows from battery to boost the voltage.

$$\frac{di_{lb}}{dt} = \frac{V_b}{L_b} \quad (3.53)$$

From Fig. 3.37 it's clear that the current through inductor flows in corresponding switching condition. The inductor current can be represented as

$$I_{Lb} = \frac{I_b}{D_{sb}} \quad (3.54)$$

Where I_{Lb} is average current across inductor and D_{sb} is duty ratio for buck converter operation. It can be perceived from equation (3.54) the average current of the inductor is inversely proportional to the duty ratio of upper switch. Contrarily, the average voltage of the inductor V_b is represented by equation

$$V_b = D_{sb}V_0 \quad (3.55)$$

Where V_b is battery voltage and D_{sb} is duty ratio for converter operation. Buck and Boost conversion can be gained by regulating the duty cycles. For example, if $D_{sb1} > D_{sb2}$, buck conversion can be implemented from output voltage V_o to battery and on the same basis if $D_{sb1} < D_{sb2}$ boost voltage can be achieved in an efficient way.

3.4.2 Control Scheme for Bi-directional DC-DC Converter Topology

An appropriate control strategy is required for proper voltage regulation and voltage charging of the battery. A control strategy scheme for closed loop operation of the proposed converter configuration is shown in Fig. 3.38. The implementation of digital control is a viable option that gives robust and precise control performance. Constant current/Constant voltage (CC/CV) mode of control algorithm has been implemented using FPGA board. The controller is composed of a 12 bit analog to digital converter (A/D), low pass filter and isolator gate driver, mode charge selection, a current controller and a voltage controller. Charge of each mode CC/CV requires its own self-governing controller. Mode selection will play a vital role in selecting mode of control according to the mode of charge. The battery voltage determines the mode of charging. The CC mode is activated when the battery voltage is lower than the maximum charge voltage, 48 V In this paper, to charge the battery in the CC mode while the voltage controller is deactivated. Similarly, when battery voltage reaches to its maximum charge voltage, the current controller is automatically gets shut-down and the voltage controller is turned on to charge the battery in CV mode.

The current or voltage controller is composed of a PI controller, a frequency limiter and data processing unit. The CC/CV controller makes the PWM command using the feedback voltage signal from the A/D controller with the resolution of 12 bit. The control signal produced from voltage or current controller will be fed to FPGA controller board where phase shift percentage for each source input modules can be determined and provides to isolated phase shift gate driver. Fig. 3.39 shows the Flow chart of CC/CV mode of control strategy for PWM generation of the proposed converter.

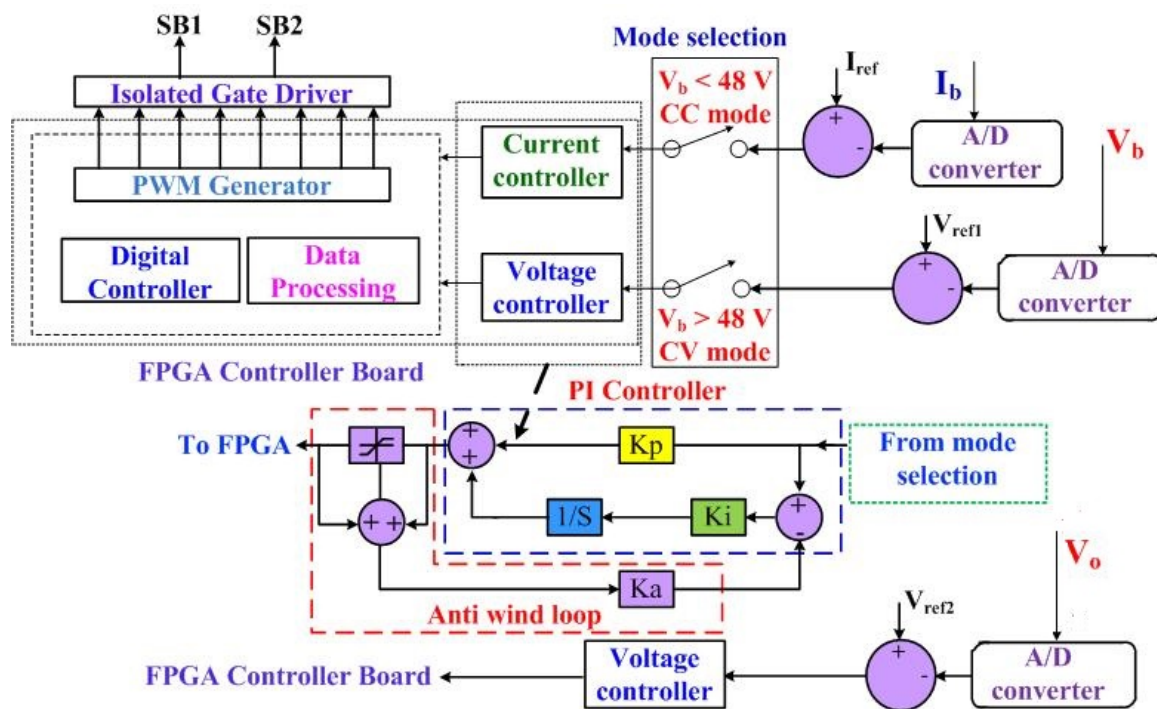


Figure 3.38: Control scheme for bi-directional buck-boost converter using CC/CV mode of operation

3.4.3 Results and Discussions

To verify the CC/CV mode of battery charging using presented bidirectional DC-DC converter and a 4 Ah Lithium cobalt oxide battery is modeled in MATLAB/Simulink platform. The simulation of the proposed converter topology has been done in MATLAB environment.

Fig. 3.40 (a) shows the output voltage of 300 V that is stepped down to 48 V to

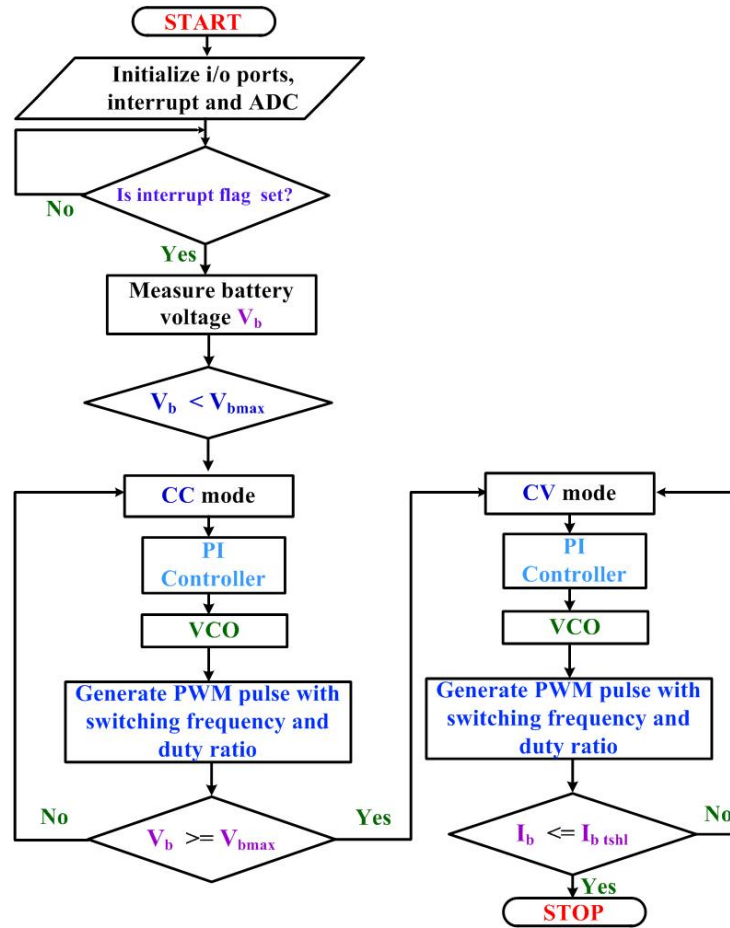


Figure 3.39: Flow chart of CC/CV mode of control strategy for PWM generation of the presented converter

charge the battery. CC/CV mode of charging is used to charge the battery. Fig. 3.40 (b) shows the ripple current of battery. Based on the inductor value ripple can be minimized. Fig. 3.40 shows the waveform of constant battery voltage of 48. Figure 3.41 shows the inductor voltage and current characteristics.

An experimental prototype has been implemented to charge the battery and to discharge for the presented topology. Fig. 3.42 shows the experimental voltage and gating signal during buck and boost operation of the presented converter. Fig. 3.42 (a) shows the switch voltage and gate signals across switch during charging of battery. During this operation voltage is stepped down from 300 V to 48 V. Similarly, Fig. 3.42 (b) shows the switch voltage and gate signals across switch during step-up operation. During this operation voltage is stepped up from 48 V to 300 V. Fig. 3.43 shows

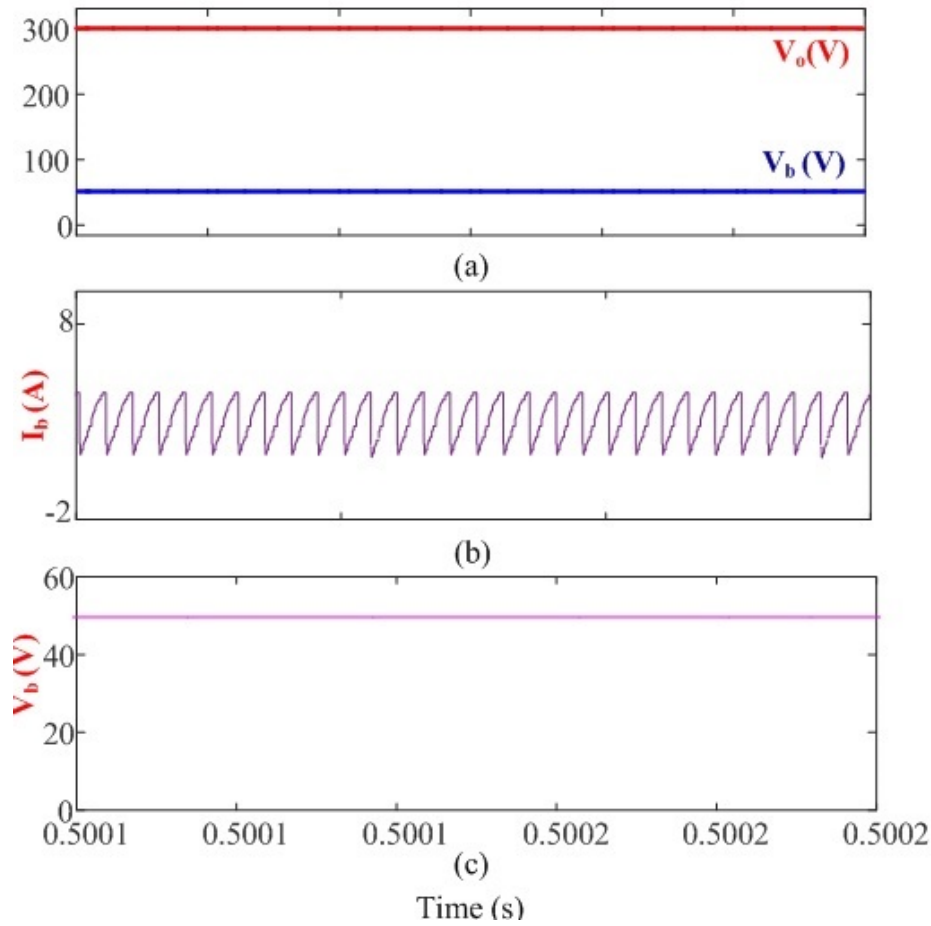


Figure 3.40: Simulated waveform of (a) Output voltage and battery voltage. (b) Battery current (c) Battery Voltage

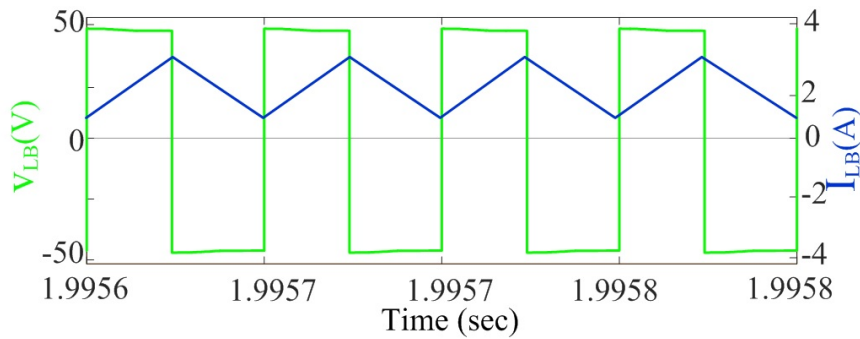


Figure 3.41: Simulated waveform of VI characteristics of inductors L_b during switching

the voltage and inductor current across inductor during buck and boost operation. Fig. 3.43 (a) shows the voltage and inductor current across inductor during buck

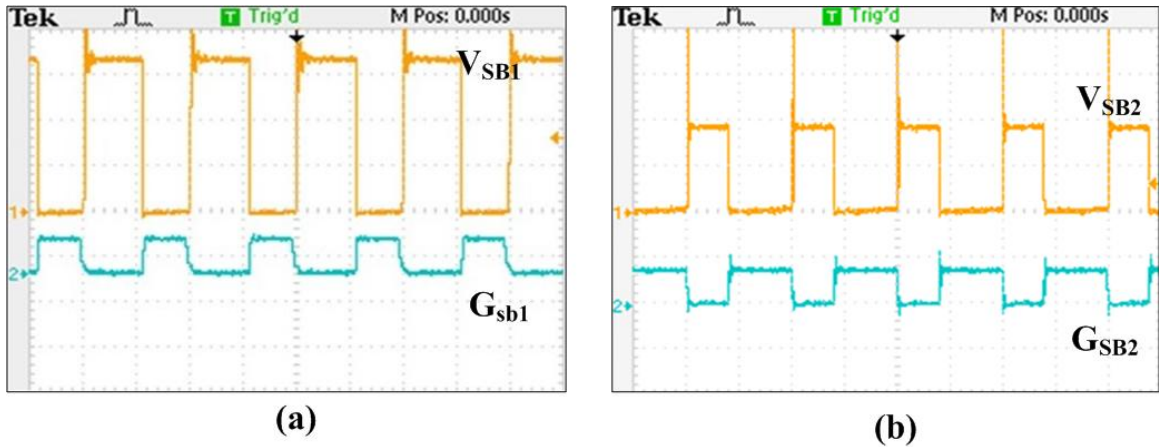


Figure 3.42: Experimental waveform of (a) Voltage and switching gate signal across switch SB1 during buck operation (b) Voltage and switching gate signal across switch SB2 during boost operation

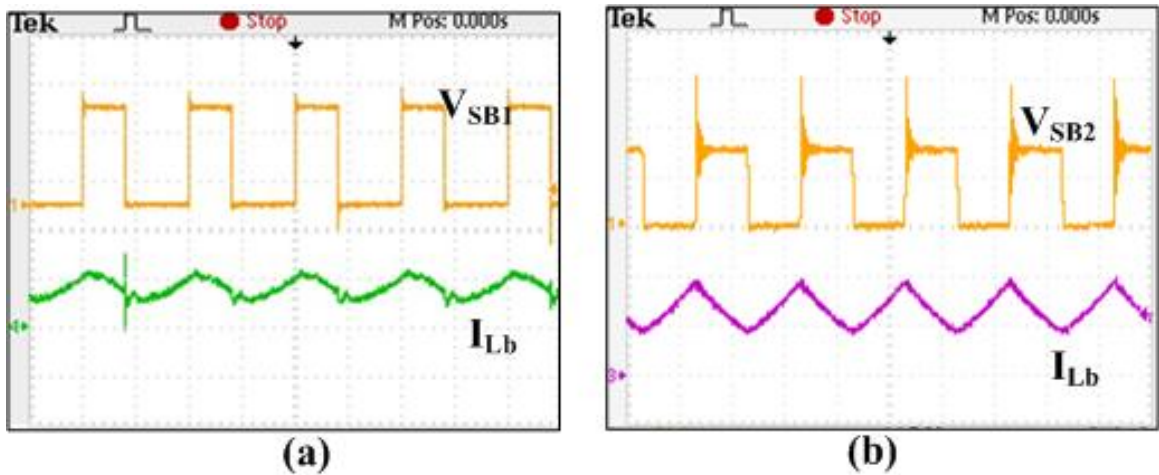


Figure 3.43: Experimental waveform of (a) Voltage across switch SB1 and current across inductor during buck operation (b) Voltage across switch SB2 and current across inductor during boost operation

operation and similarly, Fig. 3.43 (b) shows the voltage waveform across switch SB2 and current waveform across inductor. It can be observed that during both buck and boost operation the current is in continuous conduction mode. Fig. 3.43 shows the experimental waveform of inductor current and voltage waveform across switch. It can be seen that the converter is operating in continuous conduction mode. Figure 3.44 show the voltage and current waveform of battery. Fig. 3.44 (b) shows the voltage and current waveform across inductor during battery charging mode condition. It can

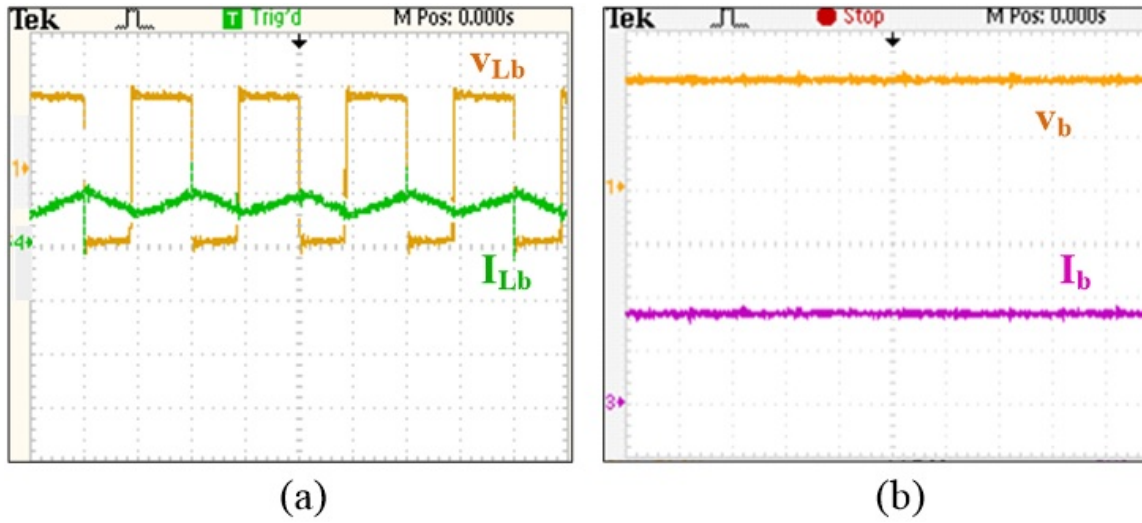


Figure 3.44: Experimental waveform of (a) voltage and current of battery (b) Voltage and current of inductor L_b

be observed that the battery is charging in constant voltage mode of charging. The experimental setup used for validating the proposed topology is shown in Fig. 3.45.

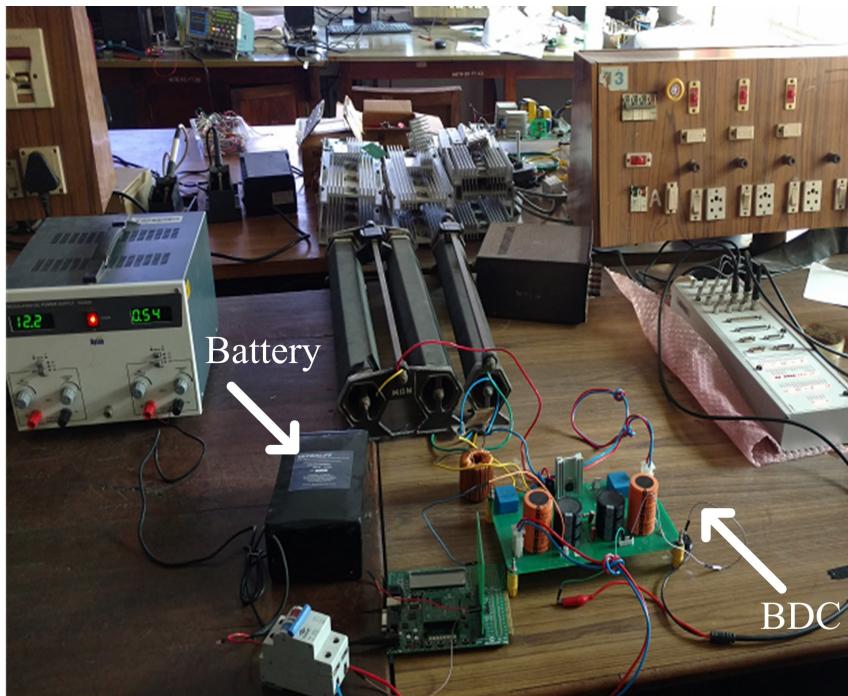


Figure 3.45: Experimental prototype for the presented bidirectional converter.

3.5 SUMMARY

This chapter has presented a detailed design, analysis and implementation of two modular based dual-input DC-DC converter with a bi-directional DC-DC converter for battery charging application. The presented modular based DC-DC step-down converter has the superiority of delivering power from both the sources to load independently and simultaneously.

The results presented shows that the presented modular converter is best suited for high current and low voltage application. A comprehensive comparison of various topologies is done to signify the dominance of the presented converter over other topologies. Further, modified modular dual-input converter configuration is developed, that can be operated over an extended range phase shift ratios between the input source converters to gain the significant ranges of the output power with regulated voltage and proper load sharing. A FPGA based digital control algorithm is preferred and realized for generation of PWM using DSP builder aids an advantage in simple closed loop control. A laboratory prototype has been developed and extensive tests have been conducted to validate the steady state and simulation analysis. It is evident that presented converter configuration has the superiority of delivering power from both the sources to load independently and simultaneously with zero voltage turn on of switches and reduced circulating currents consecutively alleviates the issue of magnetic short circuit condition. These significant characteristics of the presented modified modular dual-input converter configuration can be utilized as a promising multi-input configuration to integrate the different renewable sources and load by achieving regulated output with reduced losses. Further, a bi-directional DC-DC converter is designed and developed for charging the battery.

Chapter 4

DESIGN AND DEVELOPMENT OF MODULAR DUAL-INPUT HALF-BRIDGE DC-DC BOOST CONVERTER

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4.1 GENERAL

In the last chapter, a dual-input full-bridge modular based DC-DC converter in which secondary side rectifiers are connected in parallel structure were presented. So, in order to reduce number of components and minimise circulating power between the ports, a modular dual-input half-bridge DC-DC converter is designed and a laboratory prototype has been presented in this chapter. The chapter is systematized as follows. Section 4.2 gives the details of developed converter topology. 4.3 briefly presents modes of operation and steady state analysis of the converter. Section 4.4 presents ZVS operation of the presented topology. Section 4.5 briefly presents design. Section 4.6 briefly presents the control strategy for proper power sharing of the developed converter. Finally, Section 4.7 presents the results and discussion of the presented converter and summary of the chapter is presented at the end.

4.2 MODULAR DUAL-INPUT HALF-BRIDGE CONVERTER

The schematic of dual-input half-bridge DC-DC step up converter (DI-HBC) configuration is shown in Fig. 4.1. The primary side of DI-HBC has two active half-bridges comprising of four switches S1, S2 and S3, S4 that are connected from two different energy sources. Each active half bridge has two capacitors of equal value. The input voltage will be equally dividing between two capacitors. The output of the two HFTs is connected to a three-leg converter (TLC) at secondary side. It is an active full-bridge converter that consists of three active leg with six switches S5 to S10. The active switches S5, S6 and S7, S8 will build one active full-bridge converter for HFT₁. Whereas, the S7, S8 and S9, S10 builds another full-bridge circuit for HFT₂. The active leg composed of S7 and S8 shares the two-active full-bridge converters. The output of two half-bridge is in parallel to achieve proper voltage regulation with extended voltage range. The inductance L_{r1} and L_{r2} can be either leakage inductance of a transformer or it can be built separately to gain the desired value is a significant element in determining the power handling capacity. The DI-HBC configuration offers two HFTs as presented in Fig. 4.2. Hence, there is no direct leakage inductance between the inputs of the active bridges that aids in minimizing the leakage power between the two sources. Therefore, the DI-HBC benefits in reducing circulat-

ing current between the modules of HFTs as compared to other triple active bridge converter (Wang et al., 2018). DI-HBC configuration offers two HFTs as presented in Figure 4.2 Therefore, the modified configuration benefits in reducing circulating power between the modules of HFTs as compared to other TPC. The AC voltage of full-bridge converter is always a square wave however that of the output converter is an irregular quasi-square waveform whose shape is dependent on phase shift. The DI-HBC configuration can be integrated from various RESs to function with increased phase shift ratio and magnitudes that enhances an improvement in obtaining desired output with considerably low circulating current in HFTs. Further, ZVS is attained over an extended range of output that gains in improving the efficiency of the overall system with reduced losses and efficiency is improved significantly.

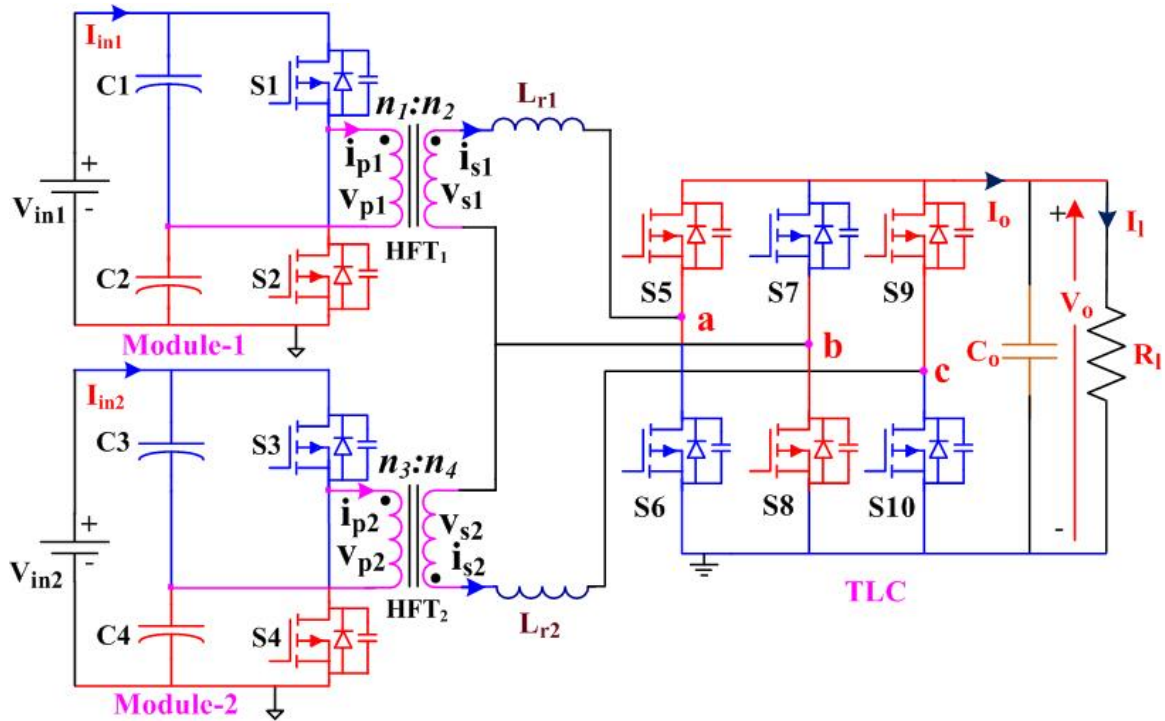


Figure 4.1: Schematic of presented dual-input converter configuration

The assumptions that are made to streamline the examination of the modified modular dual-input converter configuration are:

(a) HFTs are considered to be ideal with insignificant leakage and magnetizing inductance.

(b) All diodes and switching devices are considered to be ideal. Output Capacitor C_o value is large enough to maintain constant output voltage

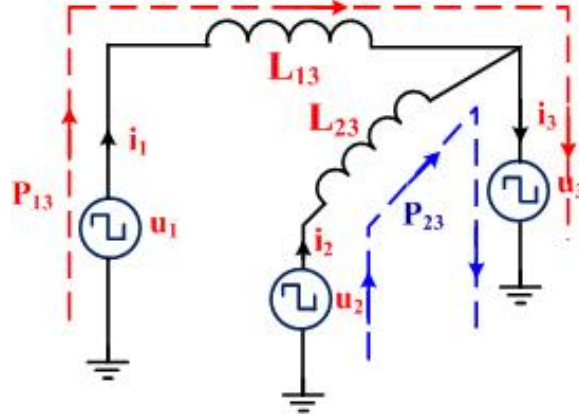


Figure 4.2: HFT equivalent circuit of the presented converter topology.

4.3 MODES OF OPERATION

The DI-HBC configuration may be operated in two different mode as dual-input mode when both the sources are available and single input when one of the sources will be active with load. This section explains the mode of operation for dual-input mode where both the sources are available to feed the load. The steady state operating waveforms for the operation of the DI-HBC configuration is depicted in Fig. 4.3. The operation over a complete switching cycle is divided into six various intervals. The symmetrical circuits of the DI-HBC circuits depicting the conduction status of switches and HFT winding currents in closed loop condition is represented in Fig. 4.4. It is considered that, before starting analysis of a new mode of operation, the secondary currents i_{s1} and i_{s2} are carrying negative currents and the active switches S2, S4 and S6, S7, S10 are turned ON and rest of the switches are in OFF condition.

Interval 1 ($t_o < t < t_1$)

This interval begins when S2 is turned OFF as shown in Fig. 4.3. Here the polarity of secondary voltage v_{s1} switch's from negative to positive. The input current i_{p1} changes from S2 to D1 correspondingly in natural way. Where D1 is antiparallel diode of switches S1. S1 is turned ON once secondary current i_{s1} becomes zero at Z1 as shown in Fig. 4.3. At this instant zero voltage leads to ZVS. Hence, ZVS is achieved. Fig. 4.4 (a) shows the corresponding circuit diagram for direction of current flow in the primary and secondary winding of HFTs during this interval. The secondary current expression from the steady state waveform with respect to interval

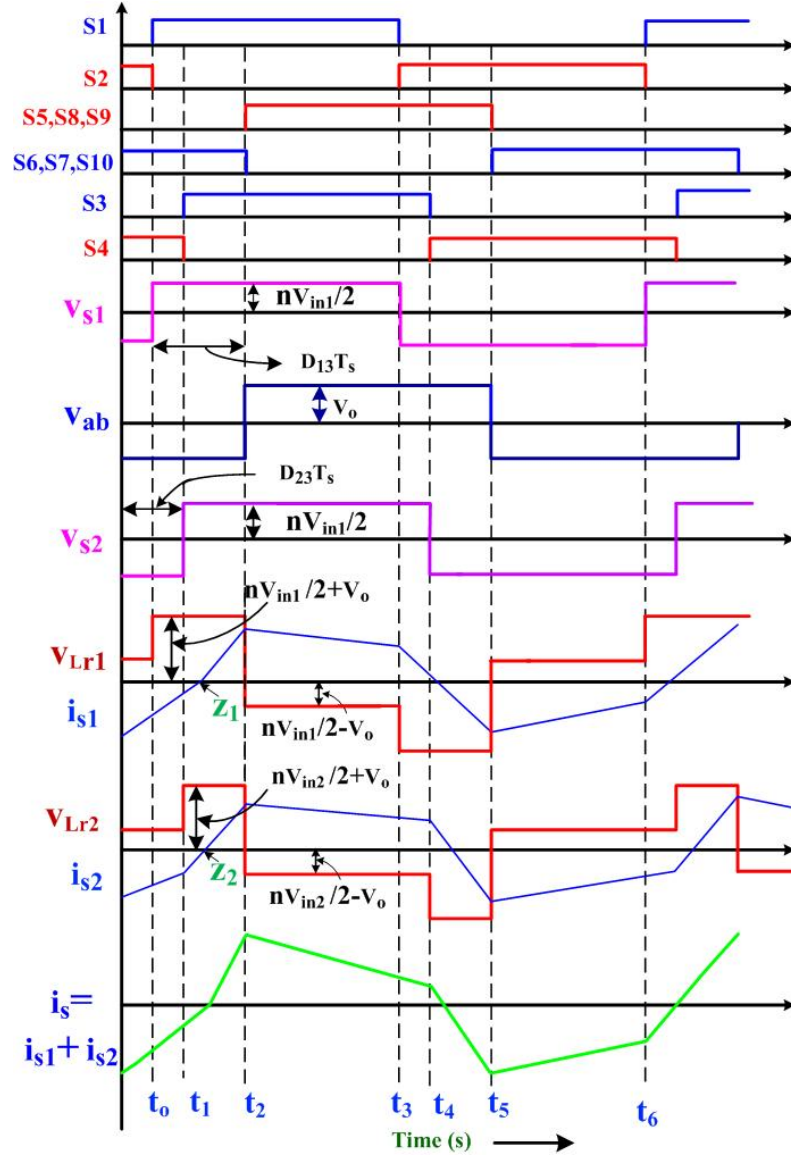


Figure 4.3: Steady state operating waveforms for modular dual-input half-bridge converter configuration

t_0-t_1 can be represented by equations (4.1)-(4.2)

$$i_{s1}(t) = [(nV_{in1}/2 + V_o)/(L_{r1})](t - t_0) + i_{s1}(t_0) \quad (4.1)$$

$$i_{s2}(t) = [(nV_{in2}/2 + V_o)/(L_{r2})](t - t_0) + i_{s2}(t_0) \quad (4.2)$$

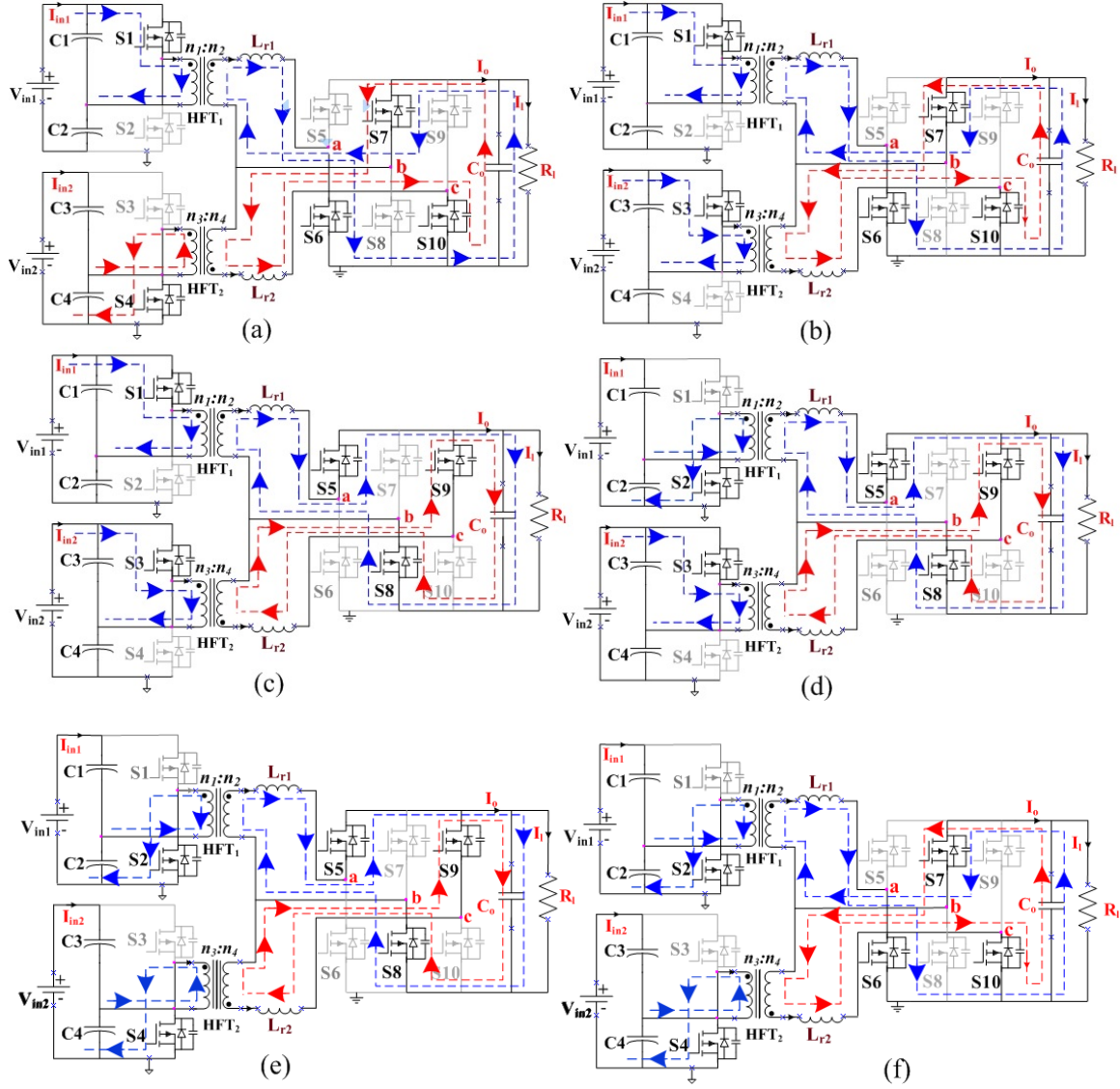


Figure 4.4: Equivalent circuits depicting the closed loop current paths for the primary and secondary of HFTs during different intervals of operation of the modified modular dual-input converter (a) interval ($t_0 < t < t_1$) (b) interval ($t_1 < t < t_2$) (c) interval ($t_2 < t < t_3$) (d) interval ($t_3 < t < t_4$) (e) interval ($t_4 < t < t_5$) (f) interval ($t_5 < t < t_6$)

Where i_{sa1} , i_{s2} are secondary current of HFT₁ and HFT₂ respectively. V_{in1} and V_{in2} are input voltages of each module, n is HFT ratio ($n = n_2/n_1$), L_{r1} and L_{r2} equivalent leakage inductance value, V_o is the output voltage and $i_{s1}(t_0)$ is the initial current that will be present before starting of this interval.

Interval 2 ($t_1 < t < t_2$)

As shown in Fig. 4.3, at instant t_1 , S4 gets turned OFF and secondary voltage v_{s2} switches from negative to positive polarity. The closed loop path of input current i_{p2} changes from S4 to D3. The switches S3 gets turned ON at zero voltage once i_{s2} becomes zero. Fig. 4.4 (b) shows the corresponding equivalent circuit for direction of current flow in primary and secondary winding of HFTs during this interval. The secondary current expression for the interval can be obtained from steady state analysis and can be represented as

$$i_{s1}(t) = [(nV_{in1}/2) - V_o/(L_{r1})](t - t_2) + i_{s1}(t_2) \quad (4.3)$$

$$i_{s2}(t) = [(nV_{in2}/2) - V_o/(L_{r2})](t - t_2) + i_{s2}(t_2) \quad (4.4)$$

Interval 3 ($t_2 < t < t_3$)

This interval begins at instant t_2 when switches S6, S7 and S10 are OFF and the secondary voltage V_{ab} shifts from negative to positive polarity. The path for secondary current i_{s1} changes from S6 to D5, S8 to D7 and current i_{s2} changes S10 to D9, S8 to D7 naturally. When current i_{s1} and i_{s2} comes to zero, switch S5, S8 and S9 gets turned ON. Fig. 4.4 (c) shows the equivalent circuit for direction of current flow in primary and secondary winding of HFTs during this interval. The expression for secondary current for this interval can be represented as

$$i_{s1}(t) = [(nV_{in1}/2) + V_o/L_{r1}](t - t_1) + i_{s1}(t_1) \quad (4.5)$$

$$i_{s2}(t) = [(nV_{in2}/2) + V_o/L_{r2}](t - t_1) + i_{s2}(t_1) \quad (4.6)$$

In the similar way the remaining intervals can be explained by utilizing steady state operating waveform as illustrated Fig. 4.4.

4.3.1 Power and Voltage Relation

The simplified equivalent circuit with HFT secondary winding voltages is shown in Fig. 4.5 in which, v_s and v_{os} signifies the secondary voltage of HFT and the AC voltage of the secondary side semi active full-bridge rectifier. L_r represent the transformer leakage inductance of HFT. The relation between voltage v_s and v_{os} and current i_r

can be obtained by applying KVL as

$$L_r \frac{\partial i_r}{\partial t} = v_s - v_{os} \quad (4.7)$$

By simplifying equation (4.7) and applying volt-second balance principle, the approximated average current I_{avg} of secondary current is can be obtained as

$$I_{avg} = \frac{1}{2f_s L_r} D(1 - D)V_o \quad (4.8)$$

Where D is the phase shift ratio for input modules and V_o is output voltage, f_s

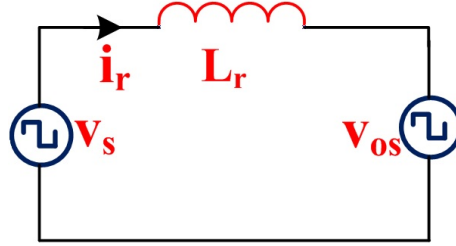


Figure 4.5: Equivalent circuit diagram for secondary winding voltage

is switching frequency and L_r is leakage inductance. By using equation (4.8) and substituting I_{avg} , Power can be calculated as

$$P_o = V_o I_o \quad (4.9)$$

Where,

$$\frac{V_o}{V_{in}} = \frac{n_2}{n_1} = n \quad (4.10)$$

$$V_o = nV_{in} \quad (4.11)$$

Substituting V_o in equation (4.11) we get

$$P_o = nV_{in} I_{avg} \quad (4.12)$$

Where I_{avg} is secondary current of HFT, substituting I_{avg} in equation (4.12) output power expression can be represented as

$$P_o = (nV_{in}) \frac{1}{2f_s L_r} D(1 - D)V_o \quad (4.13)$$

Where P_o is output power and D is phase shift ratio, f_s is switching frequency, V_{in} is input voltage. If a resistive load R_l is considered as load then, we have

$$P_o = \frac{V_o^2}{R_l} \quad (4.14)$$

By equating equation (4.14) and (4.13) we get output voltage given by

$$V_o = \frac{nV_{in}R_l}{2f_s L_r} D(1 - D) \quad (4.15)$$

It can be witnessed from equation (4.15) that the output voltage can be restrained by regulating the phase shift ratio D between the AC voltages of its full-bridge converters. Average current for both the modules can be derived from equations (4.1)-(4.12). By considering modified modular based dual-input converter configuration the average current equation for each module can be represented by equations (4.16) and (4.17)

$$I_{avg1} = \frac{n}{2f_s L_{r1}} D_{13}(1 - D_{13}) \quad (4.16)$$

$$I_{avg2} = \frac{n}{2f_s L_{r2}} D_{23}(1 - D_{23}) \quad (4.17)$$

Where D_{13} and D_{23} are the phase shift ratio between each modules and L_{r1} , L_{r2} are leakage inductance of respective modules. By avoiding the losses of active devices and HFTs, the total supplied power by both the energy sources at the output module can be illustrated as

$$P_1 = nV_{in1}I_{avg1} \quad (4.18)$$

and

$$P_2 = nV_{in2}I_{avg2} \quad (4.19)$$

By substituting equation (4.16) and (4.17) the power for each module can be represented by

$$P_1 = \frac{n(V_{in1}/2)V_o}{2f_s L_{r2}} D_{23}(1 - D_{23}) \quad (4.20)$$

$$P_2 = \frac{n(V_{in2}/2)V_o}{2f_s L_{r2}} D_{23}(1 - D_{23}) \quad (4.21)$$

The total power consumed by each module can be represented by equation (4.23)

$$P_o = P_1 + P_2 \quad (4.22)$$

$$P_o = \frac{V_o}{2f_s} \left[\frac{n(V_{in1}/2)D_{13}(1 - D_{13})}{L_{r1}} + \frac{n(V_{in2}/2)D_{23}(1 - D_{23})}{L_{r2}} \right] \quad (4.23)$$

By considering two input, output voltage can be obtained by equating equations (4.15) and (4.23) considering resistive load as R_L

$$V_o = \frac{nR_L}{2f_s} (V_{in1} + V_{in2}) \quad (4.24)$$

$$V_o = \frac{R_L}{2f_s} \left[\frac{n(V_{in1}/2)D_{13}(1 - D_{13})}{L_{r1}} + \frac{n(V_{in2}/2)D_{23}(1 - D_{23})}{L_{r2}} \right] \quad (4.25)$$

Where n is turns ration where $n = n_2/n_1$, D_{13} and D_{23} are phase shift ration between each module, L_{r1} and L_{r2} is leakage inductance of HFT₁ and HFT₂ respectively. It can be observed from equation (4.25) that the output voltage variation is with respect to the phase shift ratios (D_{13} and D_{23}) for different source voltages and load resistance.

4.3.2 Zero Voltage Switching

Fig. 4.3 shows the key waveforms for steady-state voltage and current waveform for zero voltage switching. Considering before turn ON of switch S1 the primary input current i_{p1} will be negative as shown in Fig. 4.6. Once S2 is turned OFF, C_{r1} the

parasitic capacitance of switch S1 that will be present across switch will discharges from V_{in1} to zero. At the same time C_{r2} the parasitic capacitance across S2 will start charging from zero to V_{in1} . As input current i_{p1} is negative, it freewheels through an antiparallel diode D1 of switch S1 once the process of charging and discharge is finished.

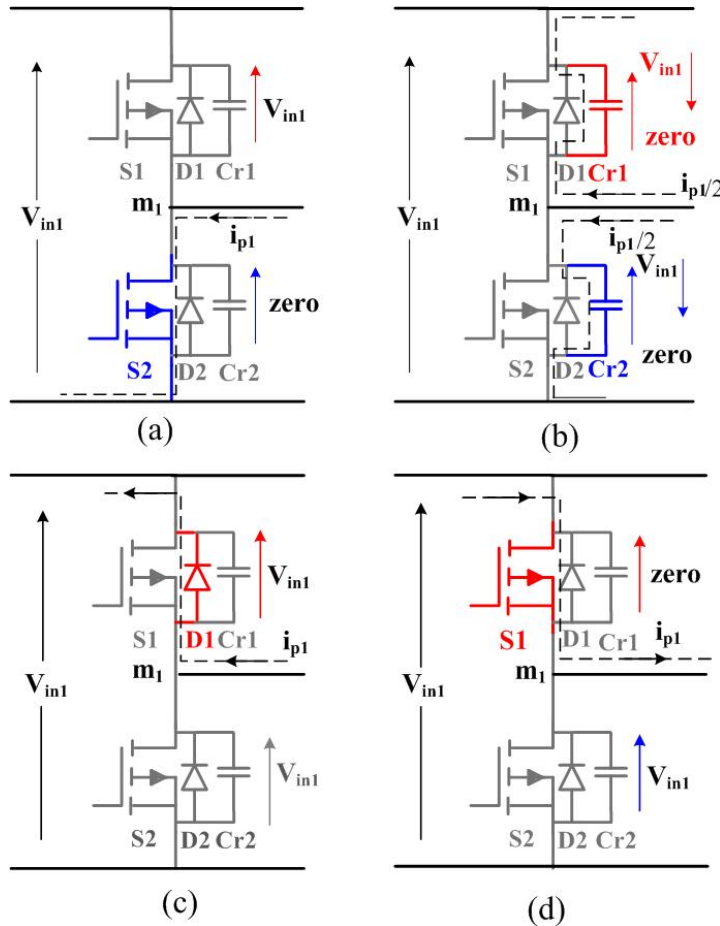


Figure 4.6: ZVS operation of S1 (a) Instant before turn on of switch (b) Charging and discharging process of C_{r1} and C_{r2} (c) Freewheeling of diode (d) Current changing path and conduction of switch S1.

As, S1 is accommodated with turn ON gate signal from the controller it starts conducting at zero voltage as soon as i_{p1} alternates its polarity. In the same way all other switches also turn ON with ZVS. The conditions needed for switches of modified converter configuration for ZVS is listed in Table 4.1. It can be observed that from the steady state waveforms that ZVS for input converter switches S1-S4 can be achieved only when $i_{s1}(t_o)$ and $i_{s2}(t_3)$ is less than zero. Similarly, for the

Table 4.1: Conditions for ZVS operation of switches

Input Module	Switches	Conditions
V_{in1}	S1, S2	$i_{s1}(t_o) < 0, i_{s1}(t_3) < 0$
V_{in2}	S3, S4	$i_{s2}(t_1) < 0, i_{s2}(t_4) < 0$
Three leg Converter	S5,S6	$i_{s1}(t_2) < 0, i_{s2}(t_5) < 0$
	S7,S8	$i_{s1}(t_2) + i_{s2}(t_2) > 0$
	S9,S10	$i_{s1}(t_5) + i_{s2}(t_5) < 0,$
		$i_{s2}(t_2) > 0, i_{s2}(t_5) > 0$

other module converters ZVS can be achieved at conditions listed in Table 4.1. For proper understanding of ZVS operation we have considered both the input full-bridge converters are in phase and are fed from identical sources then the following expression can be achieved by evaluating the steady state waveform as,

$$i_{s1}(t_o) = i_{s2}(t_1), i_{s1}(t_1) = i_{s2}(t_2) = I_2 \quad (4.26)$$

and the expression for I_1 and I_2 can be derived. Where I_1 and I_2 are average currents for each module. Hence, I_1, I_2 can be expressed as

$$I_1 = \frac{1}{4\pi f_s L_r} (1 - 2D)V_o - nV_{in} \quad (4.27)$$

$$I_2 = \frac{1}{4\pi f_s L_r} (2D - 1)nV_{in} + V_o \quad (4.28)$$

Where D is phase shift ratio, I_1, I_2 are average currents of module1 and module 2 respectively. Then by substituting equation (4.26)-(4.28) in output voltage equation and constrained listed in Table 4.1, we get following relation

$$M \leq \frac{1}{1 - 2D}, M \geq (1 - 2) \quad (4.29)$$

Where, M represent the voltage gain that is given by

$$M = \frac{V_o}{nV_{in}/2} \quad (4.30)$$

4.4 DESIGN OF DUAL-INPUT HALF BRIDGE CONVERTER

Here, the design for developed DI-HBC configuration is illustrated with the following specifications:

Input Voltage $V_{in1} = 48$ V

$V_{in2} = 230$ V,

Output voltage $V_o = 300$ V,

Power $P_{in1} = 2$ kW, $P_{in2} = 1$ kW,

Total Power $P_o = 3$ kW,

switching frequency $f_s = 20$ kHz. The voltage ratio V_2/V_1 of HFT_1 is 12.5 and similarly of HFT_2 is 2.6. The design equations are represented to decide the component rating. It benefits in proper selection of components as well as forecast the performance of the modified converter analytically. The design equations are represented to decide the component rating. It benefits in proper selection of components as well as forecast the performance of the modified converter analytically.

1. Design of HFT: The design of HFT includes the selection of frequency, core and turns ratio. The selection of switching frequency plays an important role in designing a HFT for the converter. The power loss is a function of the switching frequency. The switching losses increases with the switching frequency while the magnetic core losses and conduction losses decreases. Since higher switching frequency leads to lower flux swing and less ripple current. Hence, by considering these parameters and power rating of the developed system high switching frequency is selected for implementation of the developed converter. High switching frequency will compact the size and the weight of converter. Therefore, switching frequency of $f_s = 20$ kHz is selected for the operation of the converter

The following steps are followed for designing a HFT

- (a) Specification of the developed converter is defined.

- (b) Absolute duty cycle limit D_{lim} , and tentative normal D_{max} at low input voltage is defined. So for designing of leakage inductance D is defined as 0.4
- (c) Output voltages and secondary IR drops at full load has been selected for the proposed converter.
- (d) Turns ratios (n) for both the HFTs are calculated using equation (4.31) and (4.32). Turns ratio is selected such that choices with low voltage will probably be limited

$$n = \frac{N_1}{N_2} = \frac{V_1}{V_2} \quad (4.31)$$

where N_1 is primary turns of HFT_1 and N_2 is secondary turns of HFT_1 . v_1 is input voltage of HFT_1 and v_2 is secondary output voltage of HFT_1 Similarly,

Where N_3 is primary turns of HFT_2 and N_4 is secondary turns of HFT_2 . v_3 is input voltage of HFT_2 and v_4 is secondary output voltage of HFT_2 . For HFT_1 , input voltage is 48 V and for half bridge converter HFT primary voltage will be 24 V and secondary voltage is 300 V. So,

$$n_1 = \frac{v_1}{v_2} = 0.08 \quad (4.32)$$

Hence, n_1 is found to be 0.08 and selected as 0.1. Similarly for HFT_2 input voltage is 230 V and primary of HFT_2 will be 115 and secondary output voltage will be 300 V. So, n_2 is found to be 0.38. Hence, for practical application 0.5 is selected.

2. Core Selection Core Material: Ferrite, Magnetics Type U Core type, For construction of HFT U101/76/30 is selected. Core specifications: The selected core for modified modular dual-input converter is U101/76/30 (TDK). Area product (A_p) can be calculated from equation (4.33).

$$A_p = A_c A_w = 8.4cm^4 \quad (4.33)$$

where A_c is an effective magnetic cross section, A_w is window area. Inductance of primary and secondary winding of HFT can be obtained by the equation (4.34)

$$L = A_l N^2 \quad (4.34)$$

Number of primary and secondary turns of HFT_1 are $N_1=30$ turns, $N_2=240$ turns. Similarly, primary and secondary turns of HFT_2 $N_3= 150$ and $N_4= 230$ turns respectively, which is required for the proposed dual-input converter to step up voltage. Primary inductance of HFT is calculated using equation (4.34) as, $L_{p1}=5.13 \mu\text{H}$ and $L_{s1}= 328.12 \mu\text{H}$ Similarly, secondary inductance of HFT is calculated as $L_{p2} = 128.25 \mu\text{H}$ and $L_{s2} = 301.53 \mu\text{H}$. A_l value of 5700 nH is selected from datasheet of core specification.

3. Leakage inductance L_{r1} and L_{r2} of HFT can be calculated using equation (4.35)

$$L_r = L_{r1} = L_{r2} = \frac{nR_l}{2f_s v_o} (D(1 - D)) \quad (4.35)$$

n is turns ratio found to be 0.1 and 0.5 respectively, R_l is load, D is phase shift ratio. So, L_{r1} is found to be 18 μH and L_{r2} is found to be 10 μH , D is considered as 0.4.

4. Parasitic Capacitance (C_r): Parasitic resonance is caused by parasitic components present in the circuit i.e the capacitor connected across each switch. Condition of zero voltage switching is given by

$$2\pi\sqrt{(L_r C_r)} = (1 - D)T_s \quad (4.36)$$

The value of capacitor across the switch can be obtained by equation (4.37)

$$C_r = \frac{1}{L_r} \left(\frac{(1 - D)T_s}{2\pi} \right)^2 \quad (4.37)$$

Where, L_r is leakage inductance and C_r is capacitance across each switch.

4.5 CONTROL SCHEME

To maintain the desired output voltage across the load terminals and to supervise the power sharing from source to the load, an appropriate control approach for the developed modular dual-input converter configuration is presented in this section. Fig. 4.7 shows the schematic for the control strategy of modular dual-input converter.

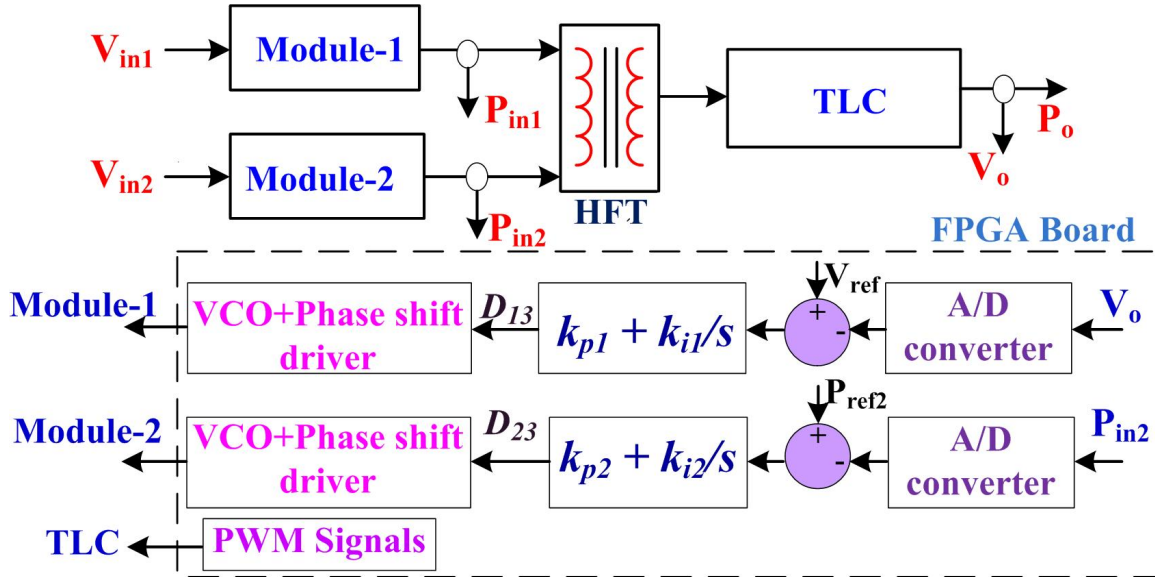


Figure 4.7: Control strategy for the presented dual-input DC-DC converter.

It can be perceived from equation (4.23) and (4.25) that phase shift ration D_{13} and D_{23} plays a vital role in regulating output voltage V_o . Subsequently, output voltage V_o can be controlled by changing D_{13} and D_{23} , and the powers supplied from the various RESs. The module 1 is functioned to sustain the output voltage at anticipated level. Similarly, module 2 is functioned to provide the anticipated power from the RES connected at module 2. Hence, the outstanding power utilised by the output will be provided from the RES connected to module1. Here, D_{13} is achieved by applying a proportional-integral (PI) regulator to the error signal developed by comparing the reference signal with actual output voltage. On the same basis, D_{23} is achieved by implementing a PI controller to the error signal created by the comparing the reference and real powers delivered from the module2. With proper fine tuning of phase shift ratio and providing an appropriate control signals to the switches the output voltage V_o can be regulated in an desired manner and power flow of the sources can be achieved appropriately. Real power flows from the half-bridge with leading

phase angle to the bridge with lagging phase angle, the amount of transferred power is controlled by the phase angle difference and the magnitudes of the DC voltages at the two ends as given by (4.38)

$$P_o = \frac{V_{in2}V_o}{2Lf_s}D_{23}(1 - D_{23}) \quad (4.38)$$

where, V_{in2} is input side voltage, f_s is switching frequency, L is leakage inductance, V_o is output side DC bus voltage referred to input side, and D_{23} is the ratio of time delay between the two bridges to one-half of switching period. For the proposed converter, the phase-shift control is applied to regulate the output DC voltage to the reference 300 V under different load conditions. First the difference between the V_o and the reference voltage is compared. Then, the phase-shift angle is adjusted by the proportional-integral (PI) controller to regulate V_o according to this voltage error. Due to the parameter variation of the high-frequency transformers, such as leakage inductance and turns ratio, the dual active bridge currents can be different, which results in a power unbalance of the developed converter. A power balance control method is developed to regulate the real power transferring through the dual input converter. As shown in Fig. 4.7, the voltage regulator compares the output voltage V_o with the reference V_{ref} and generates the error signal. Then, the power regulator compares the calculated average power of input with P_{ref2} and generates the phase-shift angles D_{23} for developed converter

4.6 RESULTS AND DISCUSSION

The developed dual-input converter configuration is designed for 300 V and 3 kW power. The battery is charged for 48 V.

The simulation of the modified modular based converter topology has been done in MATLAB environment. Fig. 4.8 - 4.13 illustrates the simulated waveforms of the developed dual-input converter configuration. Fig. 4.8 shows the waveforms of primary and secondary voltages of both HFTs. Voltage v_{p1} and v_{s1} are voltage waveform of HFT1 and voltage v_{p2} and v_{s2} are voltage waveforms of HFT_2 respectively. The resulted waveform shows that input primary voltages of both the HFTs are different and secondary waveforms shows that the voltage is stepped up to 300 V. Fig. 4.9

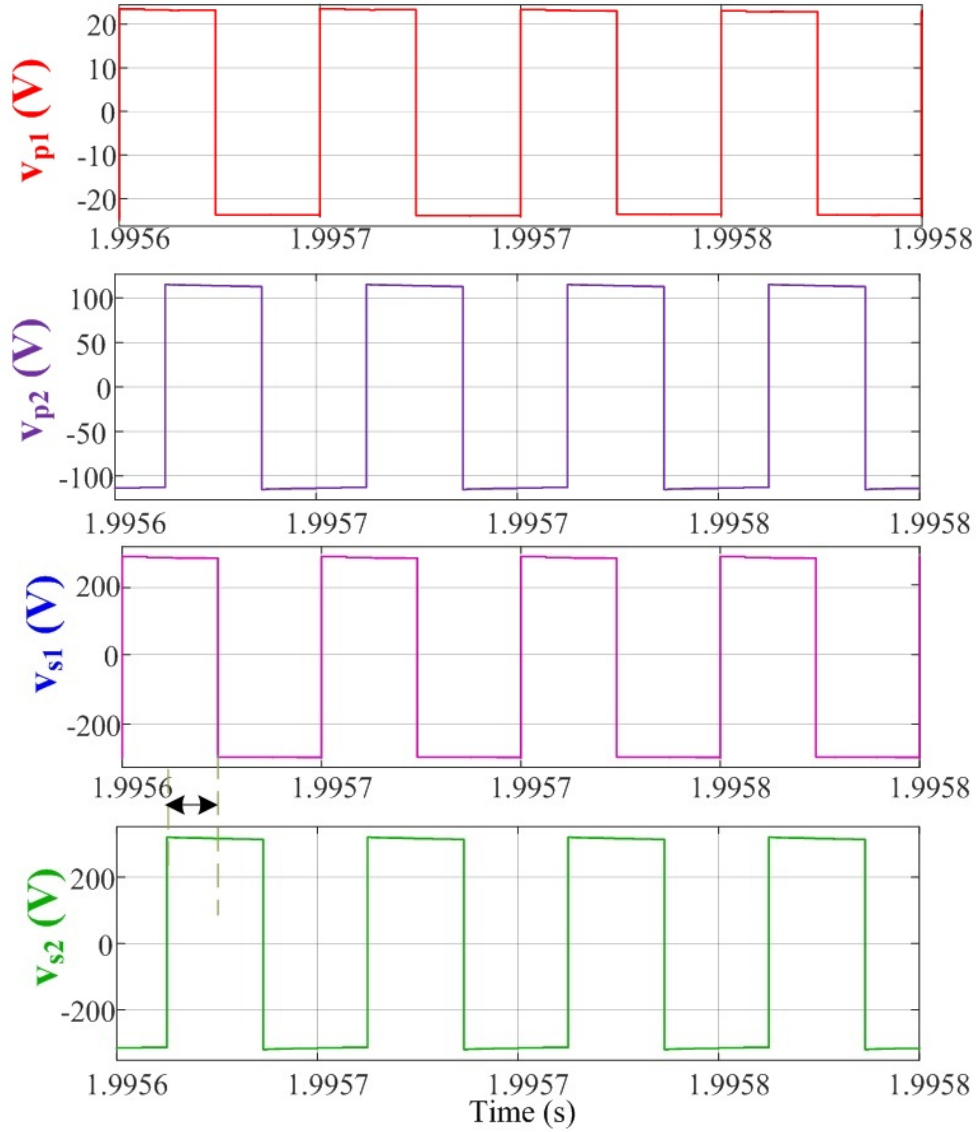


Figure 4.8: Simulated waveform of Voltage of HFTs (v_{p1} , v_{p2}) primary voltages and (v_{s1} , v_{s2}) secondary voltages of HFT_1 and HFT_2 respectively.

shows the gate signals V_{gs1} applied to switch S1 and voltages across these switch V_{DS1} . From Figure it can be observed that during the turn-on instants of switch S1 that satisfy the ZVS conditions. Fig. 4.10 shows the input and output current waveform of HFT1.

Fig. 4.11 shows the secondary voltage of HFT_1 and voltage across one bridge of three leg converter. The dynamic behaviour of the modified modular dual-input converter configuration has been deliberate by switching the load from steady state

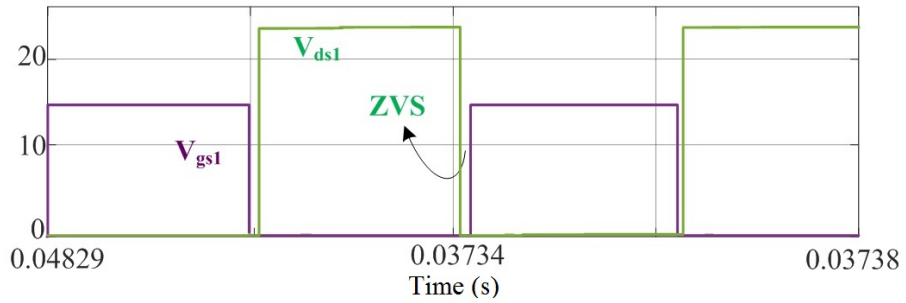


Figure 4.9: ZVS turn on operation of Switch S1 and gate pulse of S1.

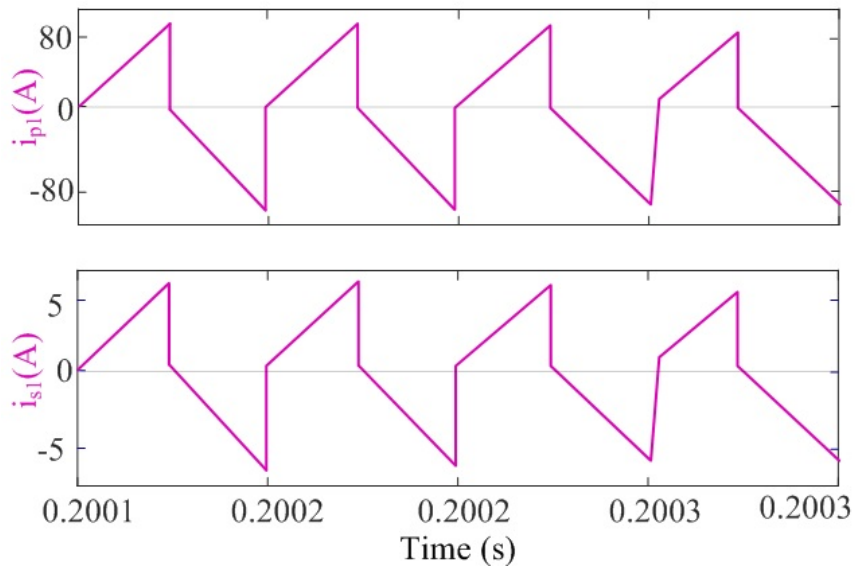


Figure 4.10: (a) Input current waveform of HFT_1 (b) output current waveform of HFT_1

condition. Fig. 4.12 shows the rectified DC voltage V_o and current I_o . The resulted

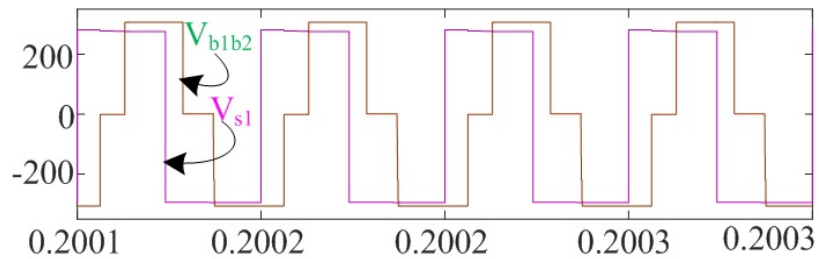


Figure 4.11: Output voltage of full-bridge rectifier at HFT_1 with voltage across one full-bridge rectifier.

waveform shows ripple free constant voltage of 300 V remains to be constant irrespective load change. It shows the dynamic behavior under step load condition from half to full load condition with proper voltage regulation. Fig. 4.12 shows the ripple free output voltage and current waveform of modified converter. Fig. 4.13 shows the simulated waveform of power sharing between each module. It clearly shows that the power is properly shared between each modules and 3 kW power is provided to load.

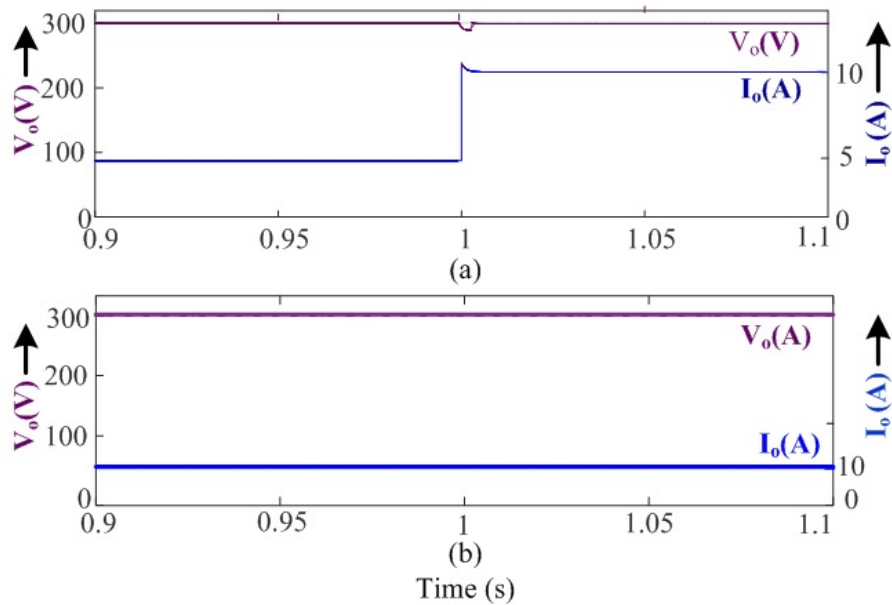


Figure 4.12: Simulated waveform of (a) dynamic behavior under step load condition (b) Output voltage and current for 3 kW load.

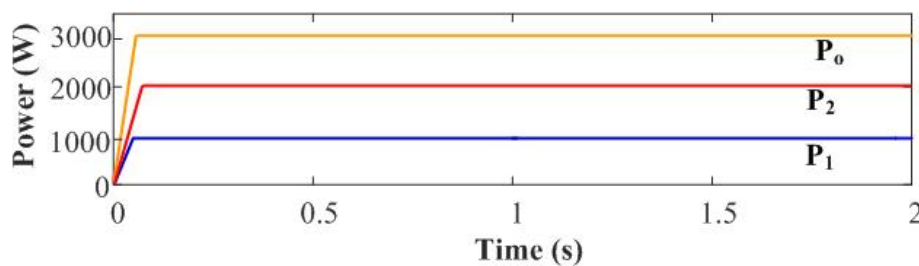


Figure 4.13: Simulation waveform of power sharing of the presented converter

To examine and justify the feasible operation of modified modular dual-input converter configuration a laboratory prototype is developed for 1 kW power. The test is conducted for both load and charging the battery FPGA board is used to implement the control algorithm of the modified modular dual-input converter configuration.

One of the converter input is connected to 48 V/5.2 A current and the other converter is connected from 230 V/4.0 A source.

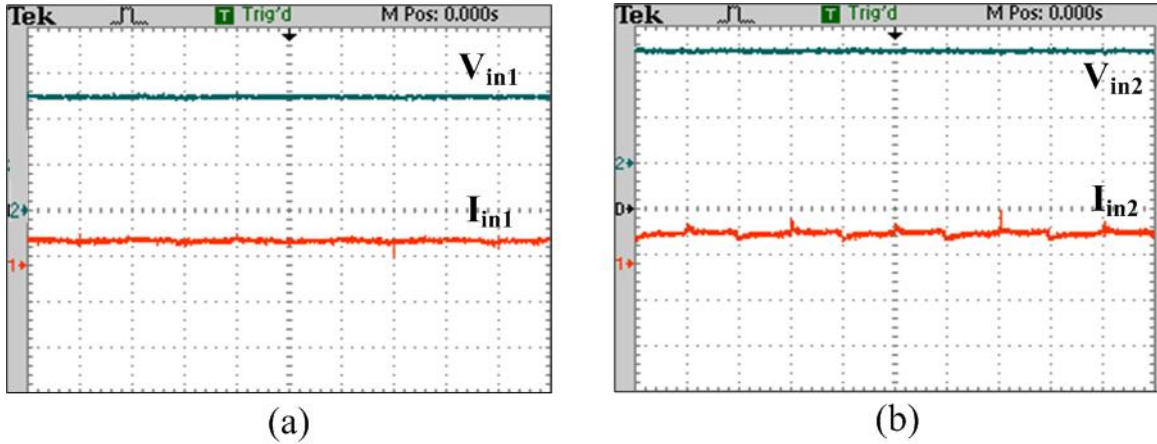


Figure 4.14: Experimental waveforms of (a) Input voltage (20 V/div) and current (10 A/div) of source 1. (b) Input voltage (100 V/div) and current (5 A/div) of source 2.

Fig. 4.14 (a) shows the input voltage/current waveform of input source1 and Fig. 4.14 (b) shows the input voltage/current waveform of source 2. Fig. 4.15 (a) and (b) shows the experimental voltage waveform of both the HFTs. The resulted waveform shows that both HFTs secondary are stepped up to 300 V.

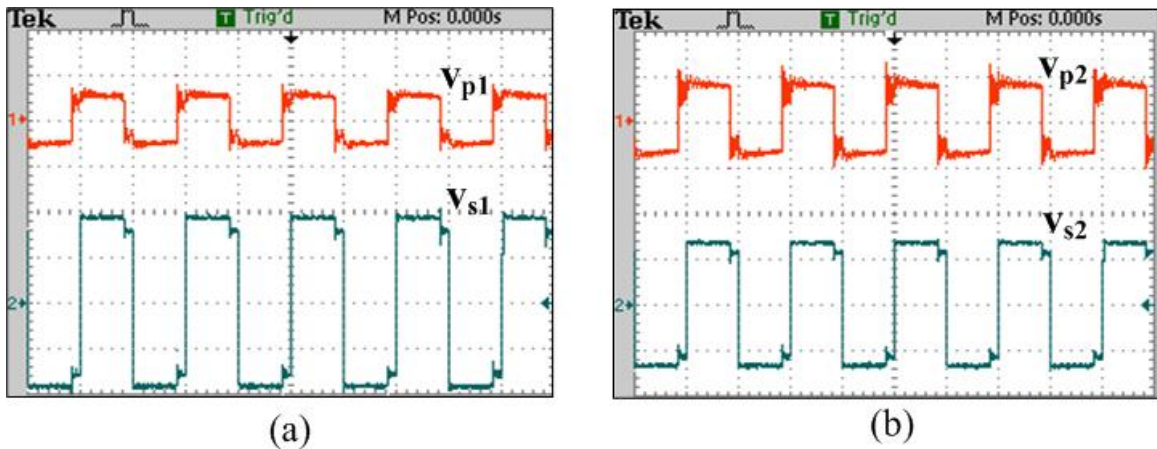


Figure 4.15: Experimental waveforms of (a) Voltage waveforms of HFT₁ ($v_{p1}=50\text{V/div}$, $v_{s1}= 100\text{V/div}$) (b) HFT₂ ($v_{p2}=200\text{ V/div}$, $v_{s2}= 200\text{V/div}$).

It can be seen that voltage v_{s1} and v_{s2} are lagging by input voltage v_{p1} and v_{p2} respectively. It indicates the power flow between input ports to output port. Fig.

4.16 shows experimental waveforms of voltage and current of HFTs.

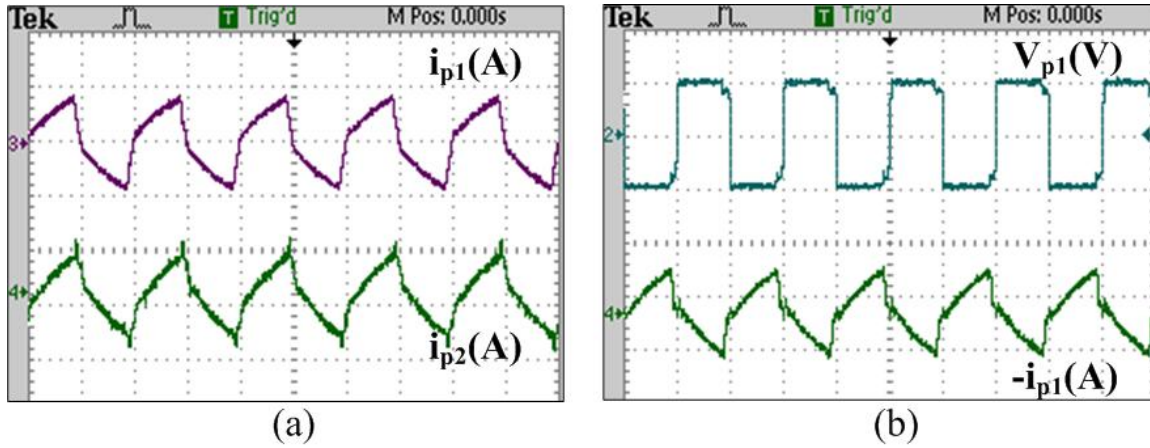


Figure 4.16: Experimental waveforms of (a) input current i_{p1} and i_{p2} . (b) Voltage and current of HFT1 primary ($v_{p1}=50\text{V/div}$).

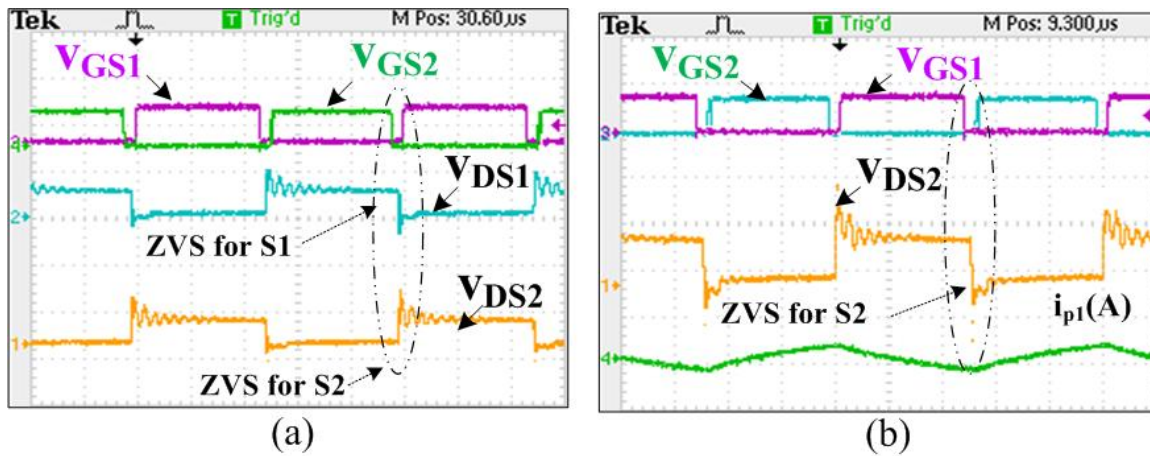


Figure 4.17: Experimental waveforms of ZVS operation of switch S1 and S2 of module 1.

Fig. 4.16 (a) shows the current waveforms of both the modules. It justifies that the power is properly shared between two ports and voltage is regulating appropriately. Fig. 4.16 (b) shows the input waveform of voltage and current of HFT1. It can be observed that the input voltage is 230 V and current is shared properly. Fig. 4.17 shows the waveform of ZVS operation of switches S1 and S2.

The gate signals (V_{GS1} and V_{GS2}) applied to switches S1 and S2, the voltages across these switches (V_{DS1} and V_{DS2}), and input current i_{p1} is shown in Fig. 4.17

(b). It can be observed that, the currents $i_{p1} < 0$, during the turn-on instants of S1 and S2, respectively, which satisfy the ZVS conditions. Similarly, Fig. 4.18 shows

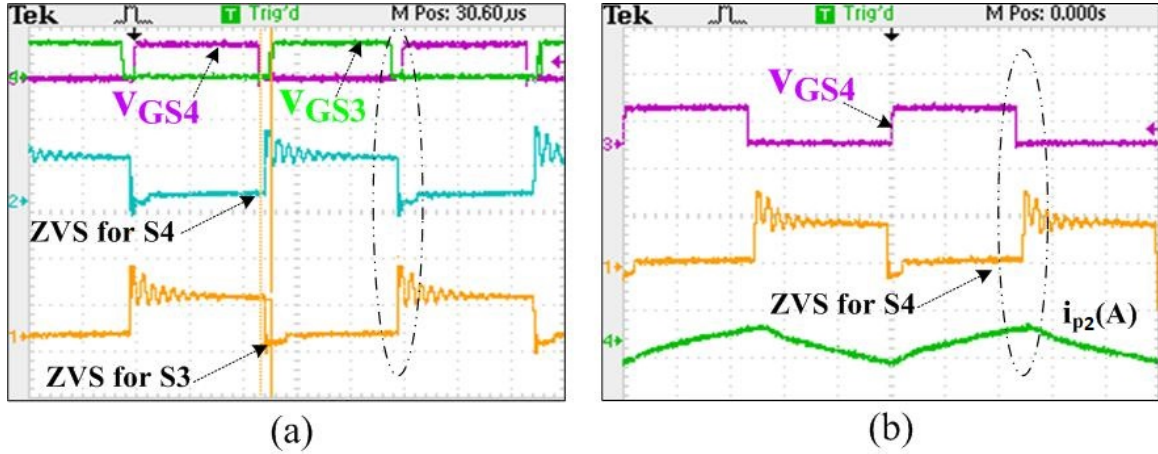


Figure 4.18: Experimental waveforms of ZVS operation of switch S3 and S4 of module 2 with input current waveform.

the experimental waveform of ZVS operation of S3 and S4. Figure 4.18 (b) it shows that current $i_{p2} > 0$, during turn of switch S7 that satisfy the ZVS condition. Fig.

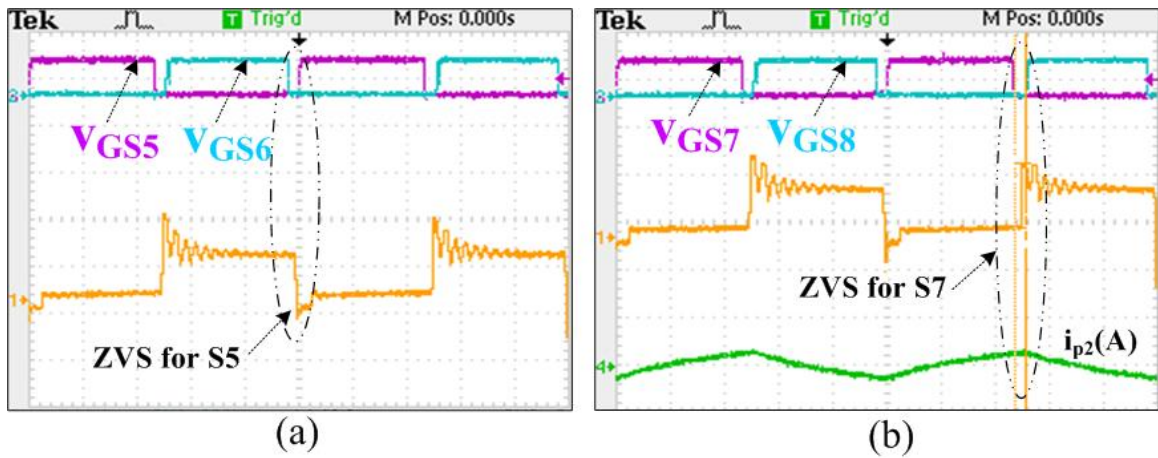


Figure 4.19: Experimental waveforms of ZVS operation of switch S5 and S7 of TLC.

4.19 shows the ZVS operation waveform of switches S5 and S7. Similarly, Fig. 4.20 shows the ZVS operation waveform of switches S6 and S8. Fig. 4.21 shows the ZVS operation waveform of switches S9 and S10. It can be observed from Fig. 4.17 - 4.21 that, ZVS is achieved for all the switches in the presented topology. Fig. 4.22 (a) and (b) shows the waveform of secondary voltage and current i_{s1} and i_{s2} respectively.

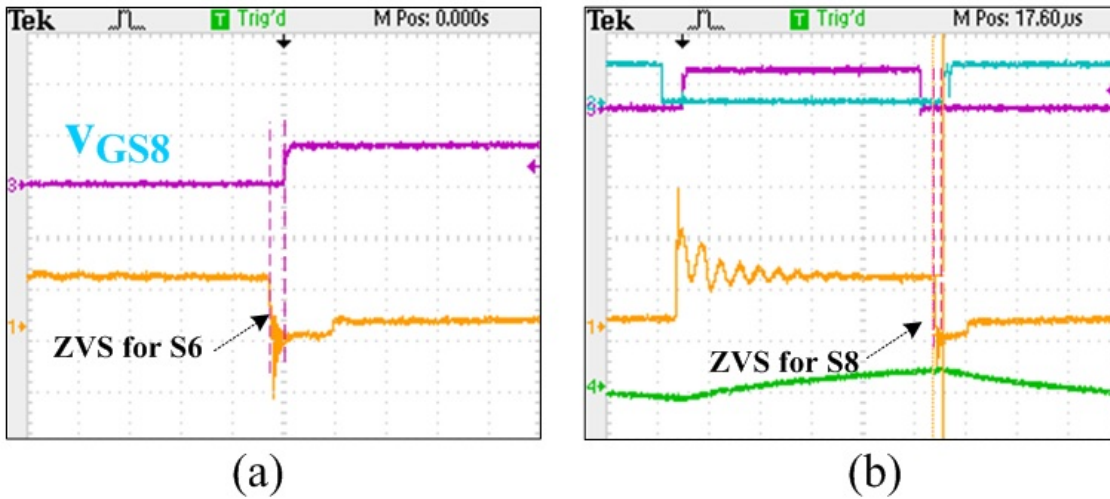


Figure 4.20: Experimental waveforms of ZVS operation of switch S6 and S8 of TLC.

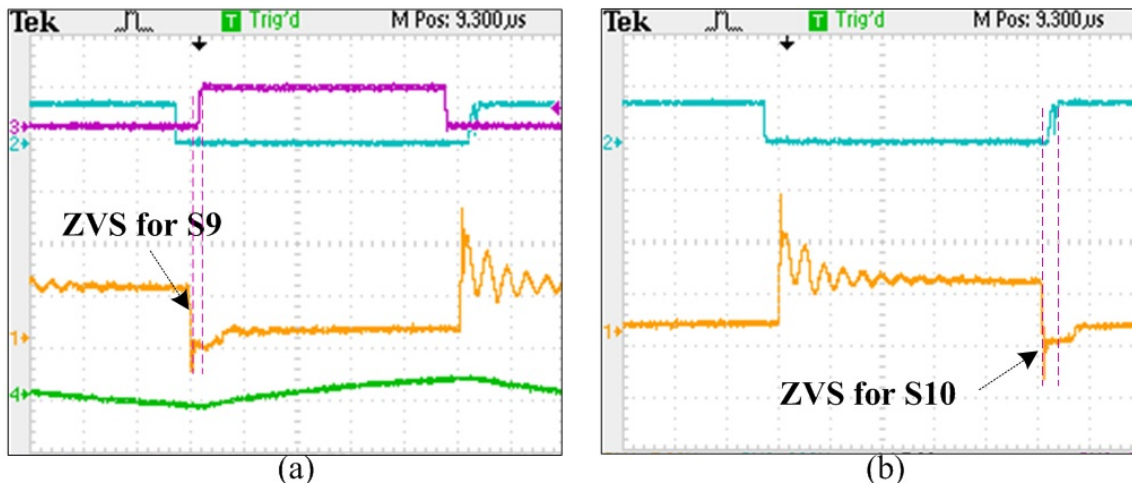


Figure 4.21: Experimental waveforms of ZVS operation of switch S9 and S10 of TLC.

This justifies the zero circulating of secondary rectifier. Fig. 4.23 (a) shows the experimental waveforms of ripple free DC output voltage and current waveform. It shows that voltage 300 V remains constant and currents are shared between the load and battery charging. Fig. 4.23 (b) shows the experimental waveforms of dynamic behaviour under step load condition. The waveform shows that voltage V_o remains to be constant irrespective of load changes and currents are varied accordingly. Fig. 4.24 (a) shows the experimental waveform of output voltage V_o and output current I_o . It shows the dynamic behavior under step load condition. It can be observed

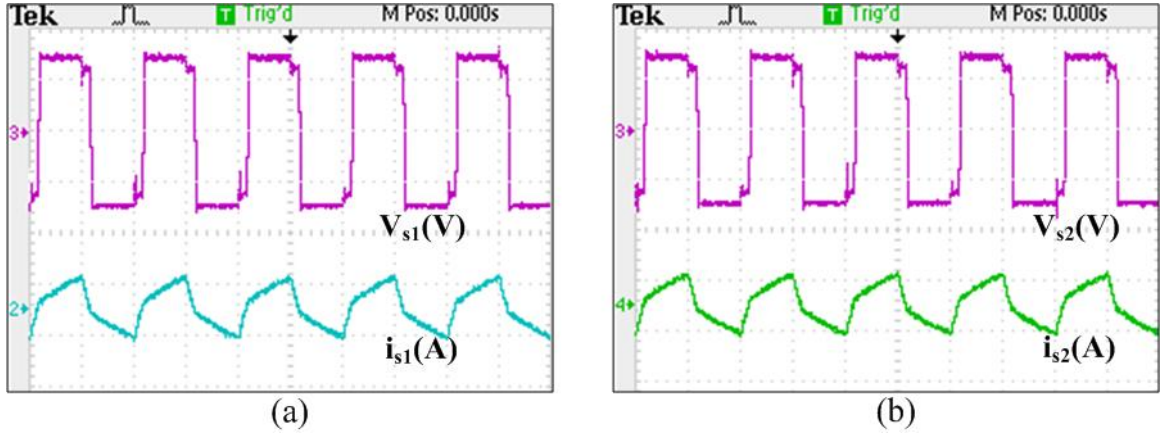


Figure 4.22: Experimental waveforms of (a) secondary voltage/current of HFT₁. (b) Secondary voltage/current of HFT₂.

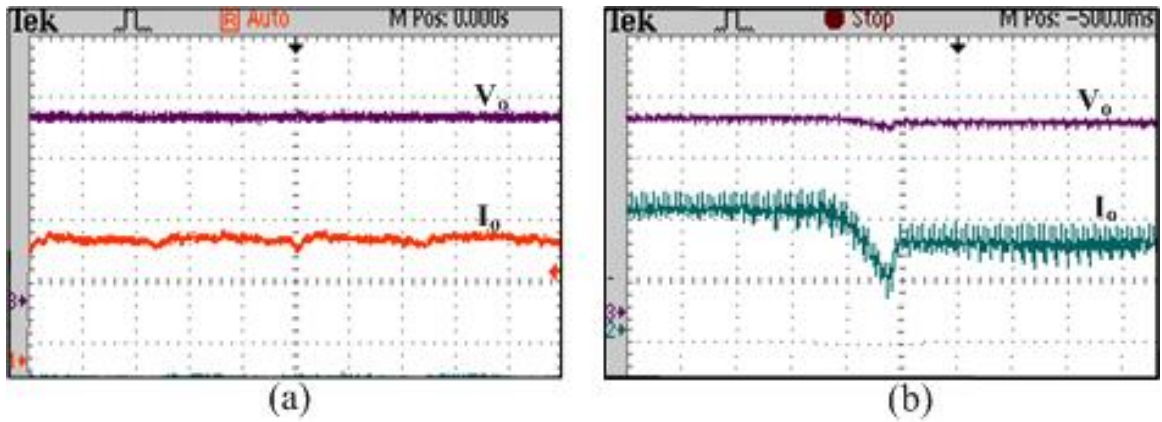


Figure 4.23: Experimental waveforms of (a) output voltage/current. (b) Dynamic behavior under step load conditions.

that voltage remains to be constant and current is varying accordingly. Fig. 4.24 (b) shows the experimental waveform of output voltage V_o and input current I_{in1} and I_{in2} . It can be observed that the output voltage remains to be constant when both the source currents are varied. It justifies the proper load sharing and power flow of the proposed converter configuration. Fig.4.25 (a) shows the experimental waveform of primary voltage and current of HFT₂. It shows the reduced circulating current at low voltage condition. It can be examined that at low voltage condition circulating current is followed by voltage properly without ripples. Similarly, Fig. 4.25 (b) shows the experimental waveform of primary voltage and current of HFT₂ for zero circulating current at full load condition. Fig. 4.26 shows the experimental setup used

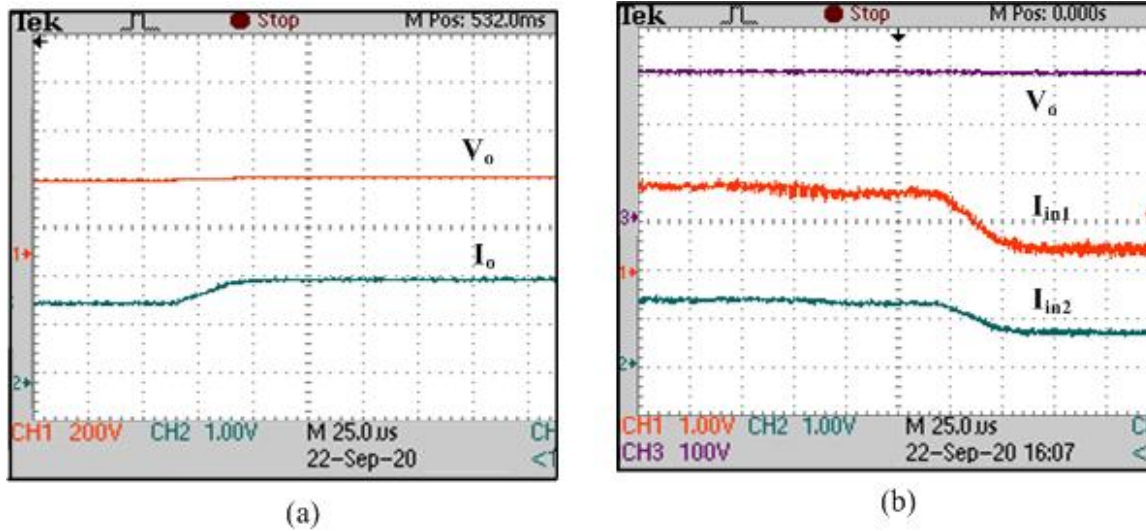


Figure 4.24: Experimental waveforms of (a) output voltage/current under step load condition. (b) Input current (I_{in1}) and (I_{in2}) with output voltage

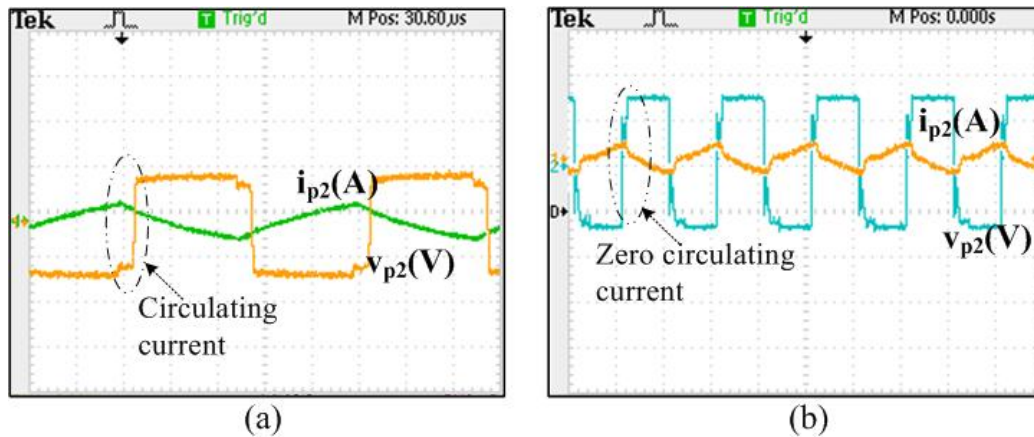


Figure 4.25: Experimental waveforms of (a) voltage/ circulating current of HFT2. (b) Reduced circulating current at 90% load

for validating the developed modified modular dual input converter with bidirectional DC-DC converter. It is observed that turn on losses of switches are zero due to ZVS operation. From the simulation and experimental results it is clear that the modified configuration operates smoothly and efficiently with minimum circulating current and proper power sharing of different sources. It is observed that due to semi active rectifier used at secondary rectifier the losses are minimized and achieved efficiency of 93%. Further, it can be reduced by replacing all the diodes with synchronous rectifier.

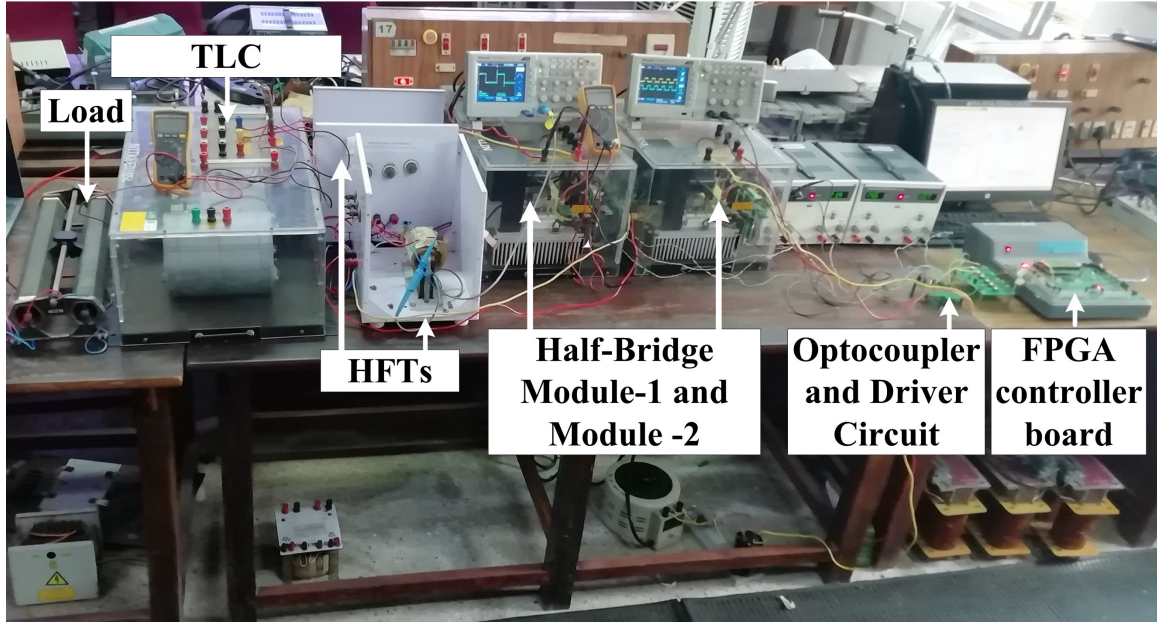


Figure 4.26: Experimental prototype for the developed modular dual input half-bridge converter topology

4.6.1 Comparison Study

To validate the supremacy of DI-HBC configuration over the other topologies a comparative study has been projected in this section. Table 4.2 demonstrates the extensive comparative study of the developed converter topology with various dual-input converter. From the literature it can be observed that all the converter configurations offer dual-input operation, ZVS, and offers galvanic isolation between the RES and the load. Among these (Asa et al., 2015) configuration structure entails the minimum number of semiconductor devices. However, dual-input operation of this configuration lead to insufficient losses. The three-port converter (Tao et al., 2008) needs reduced number of semiconductor components along with less magnetic materials where all the three windings are winded on the same core, with reference to the DI-HBC configuration. It offers most of the requisite features of dual-input converters. Conversely, simultaneous power supply from this converter configuration that are connected from two different energy sources leads in considerably higher losses as the windings of HFT gets short circuited magnetically for contrasting values of the phase shift ratios ($D_{13} \neq D_{23}$). This is due to the diodes that are connected in antiparallel structure of the accompanying modules that creates path for conduction.

Table 4.2: Comparison of developed converter with other dual input converters available in the literature

Parameters	Tao et al., 2008	Asa et al., 2015	Wang et al, 2018	Proposed
Input Sources	2	2	2	2
Active devices	6	4	12	10
Passive devices	0	4	0	0
No. of HFTs	1	2	1	2
ZVS	Yes	Yes	Yes	Yes
Isolation b/n source and load	Yes	Yes	Yes	Yes
simultaneous power flow	not recommended as $D_{13} \neq D_{23}$	Yes	not recommended	Yes
Isolation b/n sources	Complex	not recommended	complex	simple
Circulating current losses	high	medium	high	low
Controller	complex	complex	complex	moderate

Also, due to the presence of leakage inductance considerably higher power circulates between the input-ports. Converter configuration (Wang et al., 2018) compared to the DI-HBC configuration offers most of the requisite features of dual-input converters. However, it offers more number of semiconductor devices. Considerably greater losses arise as the windings of HFT are gets short circuited magnetically for various values of the phase shift ratios. The proposed DI-HBC aids in providing power supply from dual-input to load and circulating current is minimized considerably. Even though the proposed DI-HBC configuration consists relatively greater number of active switches, it permits the input module converters to function with a wide range of phase delays with reference to the input module converter to gain the desired output voltage. Higher power can be accomplished with reduced power losses. Further, in the DI-HBC configuration, isolation between two different sources can be accomplished by applying an appropriate gating signals to the respective switches.

4.6.2 Loss Analysis

The power loss of the proposed converter has been analysed. The losses can be classified as power loss and core losses. Power loss of device includes switching losses and conduction losses. Similarly, HFT losses includes, conduction loss and relative core losses. The proposed topology operates in ZVS turn on mode of operation, switching losses of all the switches are considered to be zero.

1. The switching loss of each MOSFET can be found using equation (4.39)

$$P_{sw} = \frac{1}{2}(V_{ds}I_{ds}t_{on}t_{off}) \quad (4.39)$$

where, V_{DS} and I_{DS} are voltage and current of each module. t_{on} is found to be 50 nsec from datasheet of MOSFET. The calculation is for each switch of half- bridge converter. The conduction losses of the MOSFET can be calculated using equation (4.40)

$$P_{cond} = I_{rms}^2 R_{dson} \quad (4.40)$$

Where P_{cond} is conduction loss and I_{rms} is the current flowing in the circuit during turn on of the circuit and R_{dson} is the on state resistance value of the MOSFET.

2. HFT Losses

The losses of ferrite core is proportional to the area of hysteresis loop in the acquisition. So, the HFT loss can be found from equation (4.41)

$$P_{loss} = P_{hyst} + P_{eddy} + P_{resistance} \quad (4.41)$$

Where P_{hyst} is hysteresis loss, P_{eddy} is eddy current loss and $P_{resistance}$ is resistance loss.

4.7 SUMMARY

This chapter proposes a DI-HBC configuration for proper utilization of renewable energy sources to meet the requirement of load is presented. It provides galvanic isolation between both the source and load, zero voltage turn ON of switches, proper

load sharing, and power flow, reduced circulating currents and alleviates the issue of magnetic short circuit condition, etc. The DI-HBC configuration can be functioned over an extended range phase shift ratio between the input sources. It aids to gain the significant ranges of the output power with regulated output voltage. A FPGA based digital control scheme consequences in simple closed loop control. A laboratory prototype has been developed to validate the steady state waveforms. The experimental results signify that the DI-HBC can be best suited for high voltage application and can be utilized as a promising dual-input configuration to integrate the different RES and load by achieving desired output with reduced losses.

Chapter 5

VOLTAGE REGULATION TECHNIQUE FOR TELECOM LOAD

Contents

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5.1 GENERAL

The DC loads of telecom station (i.e., transceivers) operates in pulsed power mode, and also the power consumption of these loads depends on signal traffic. (Liu et al., 2005) have modeled the transceivers in BTS station operates in a pulsed-power mode intermittently also the power telecom load profile based on the assumptions that the transceiver operates for 200s out of every 250s. During the on state condition, load draws the high amount of power for 10s and for the next 10s it draws low power as shown in Fig. 5.1. The DC loads in BTS stations requires the constant DC voltage (i.e., 48V or 24V) (Energy, 2012). However, due to pulsed power consumption of DC loads voltage will have fluctuations. Therefore, for safe operation voltage across DC loads has to be maintained constant. Therefore, in this chapter a Type II compensator is designed to regulate the voltage at the terminals of DC loads.

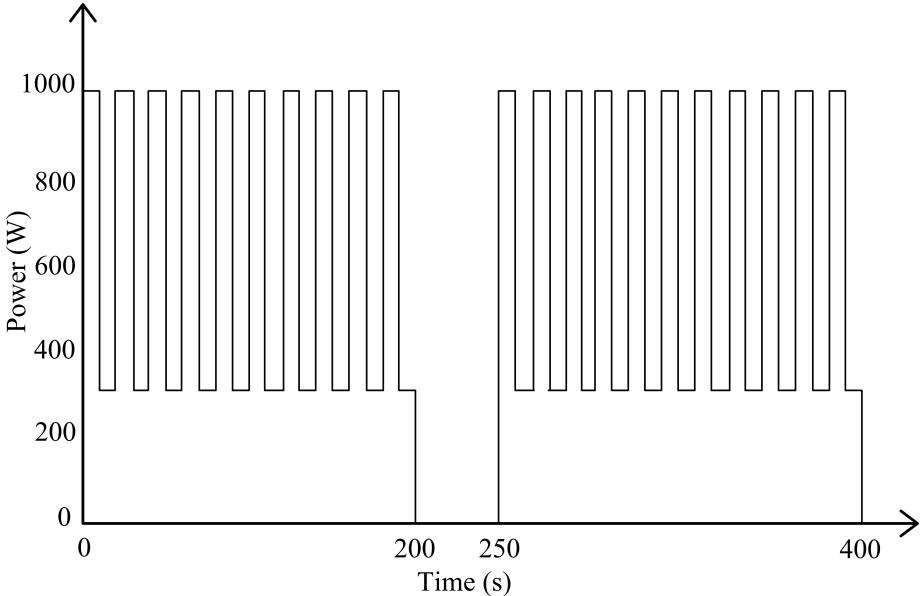


Figure 5.1: Load profile of Telecom Tower

5.2 DESIGN OF THE TYPE II COMPENSATOR FOR TIGHT VOLTAGE REGULATION

Type II compensators are popularly being used in controlling the output voltage of switching power electronic converters. Type II compensator has two poles and one

zero, which provides the required phase and gain to the total control loop of the switching converter. In this research work, to step down the voltage to 48V from DC link voltage of 300 V, a buck converter is used (ref. Fig. 2.4 in Chapter 2). In general, it is significant to have adequate phase margin and gain margin to work the control loop properly in all conditions. The schematic of the Type II compensator is shown in Fig. 5.2. To implement the Type II compensator to the buck converter, it is required to have the control to output voltage transfer function considering the parasitic elements of energy storage components of the buck converter. Equivalent series resistance (ESR) of the output capacitor in buck converter is a very critical parameter, since it introduces a zero in the converter transfer function. The buck converter control to output voltage transfer function is given in equation (5.1). From the control point of view, it is important to derive the transfer function of all the blocks shown in Fig. 5.3. The transfer function of Type II compensator is derived from the Fig. 5.2 and it is given in equation (5.2). The transfer function of PWM is generally described as $1/V_{PWM}$, where V_{PWM} is the peak to peak voltage of the carrier wave used.

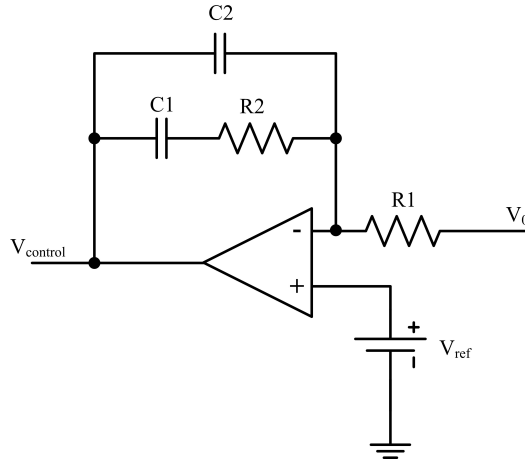


Figure 5.2: Schematic of the Type II compensator

To design the compensator with required loop characteristics, it is required to evaluate the Bode plot of the open loop system (i.e., Buck converter with PWM).

$$\frac{V_o}{d} s = \frac{V_{dlink} R_{load} (s(C_o ESR) + 1)}{L_o C_o s^2 (R_{load} C_o ESR) + R_{load}} \quad (5.1)$$

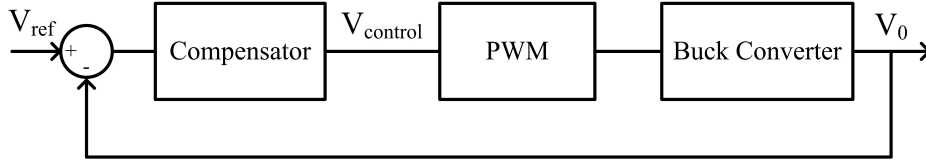


Figure 5.3: Complete control diagram of a buck converter with the Type II compensator

Buck converter parameters considered for deriving the open loop transfer function is listed in Table. 5.1.

Table 5.1: Parameters Used for Type II Compensator Design

Parameter	Value
PWM oscillator peak voltage	6.6 V
Buck regulator lter capacitor ESR	0.5 ohm
Inductor (L) and Capacitor (C) value of buck regulator	100uF, 100uH

The open loop transfer function of buck converter with PWM voltage is given in equation (5.3) and the bode plot for the same is shown in Fig. 5.4. The rest of the design steps are explained as follows,

$$\left(\frac{V_{control}}{V_o}\right)_s = \frac{V_{dclink}R_{load}[s(C_oESR) + 1]}{L_oC_o s^2(R_{load}C_oESR) + R_{load}} \quad (5.2)$$

$$\left(\frac{V_o}{d}\right)_s = \left(\frac{1056 + 0.0696s}{5.745 \times 10^{-7}s^2 + 8.768 \times 10^{-4}s + 4.8}\right) \left(\frac{1}{6.6}\right) \quad (5.3)$$

Step 1 Selecting the crossover frequency (F_0) plays an important role in any compensator design. For the desired loop characteristics, typically (F_0) is selected to be in the range of 10% to 20% of switching frequency (F_s). Moreover, selecting the higher (F_0) results in the faster dynamic response during the load change. Therefore, in this study, (F_0) is selected as 7.2 kHz.

Step 2 Determine the phase and gain of the open loop transfer function at the selected crossover frequency using the bode plot shown in Fig. 5.4. The gain and phase values of open loop buck converter with PWM at (F_0) is found to be -2:98 dB and -133 °.

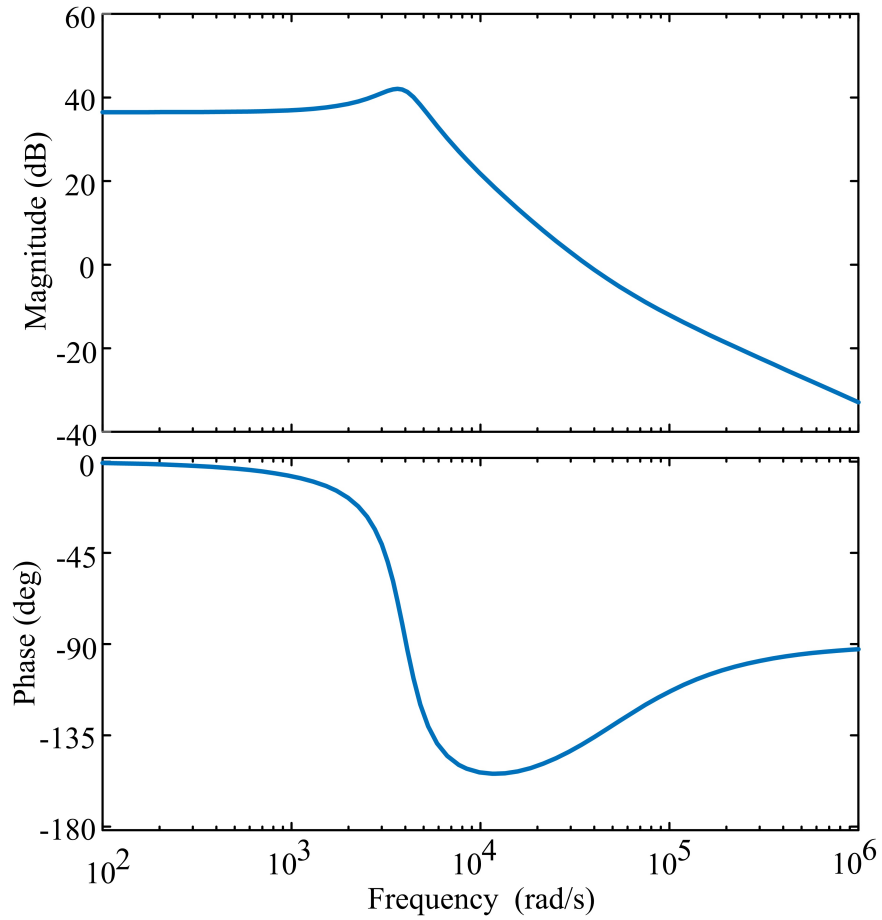


Figure 5.4: Bode diagram of open loop buck regulator

Step 3 Determining the ratio of R_2/R_1 of compensator (ref. Fig. (5.2)) using the calculated gain value in the previous step as follows,

$$\frac{R_2}{R_1} = 10 \left(\frac{Gain F_o}{20} \right) \quad (5.4)$$

Step 4 From the calculated phase at crossover frequency from bode plot of open loop transfer function, determine the required poles and zeros of compensator to provide required phase margin using the K factor technique as follows (Basso, 2008),

$$\theta_{compensator} = \theta_{phasemargin} - \theta_{F_o} \quad (5.5)$$

where, $\theta_{phasemargin}$ is the required phase margin of the closed loop system, which is selected to be 45° and F_0 is found to be 133° . From equation (5.5), K factor is calculated as follows,

$$K = \tan\left(\frac{\theta_{compensator}}{2}\right) \quad (5.6)$$

The feedback capacitors of compensator is calculated using the K value as follows

$$C1 = \frac{K}{2\pi F_0 R2} \quad (5.7)$$

$$C2 = \frac{K}{2\pi F_0 K R2} \quad (5.8)$$

From the design equations, the value of compensator elements are found to be $R1=10 \text{ k}\Omega$, $R2=7.09 \text{ k}\Omega$, $C1= 175 \text{ nF}$ and $C2= 53 \text{ pF}$. From the calculated values, transfer function of compensator is expressed as follows, From the equations (5.3) and (5.9), loop transfer function is calculated and the bode characteristics of loop transfer function is plotted and shown in Fig. 5.5.

$$G(s)_{compensator} = \frac{-(s + 805.28)}{5.3 \times 10^{-7}s^2 + 1.409s} \quad (5.9)$$

From the loop characteristics, it is clear that the phase of the loop is around 45.5° at the crossover frequency. Moreover, gain of the loop is crossing the 0dB at the low frequency (i.e., less than F_s). Therefore, this ensures the stability of the overall closed loop system. Voltage regulation for the variation in DC link voltage and load is discussed in the following section.

5.2.1 Results and Discussion

The developed Type II compensator for buck regulator at the DC loads of BTS is tested for 50% load change condition i.e., BTS draws the load current of 20 A for the duration of 3s and for the next 3 s it draws 10 A. Load current and load voltage characteristics for this case is shown in Fig. 5.6.

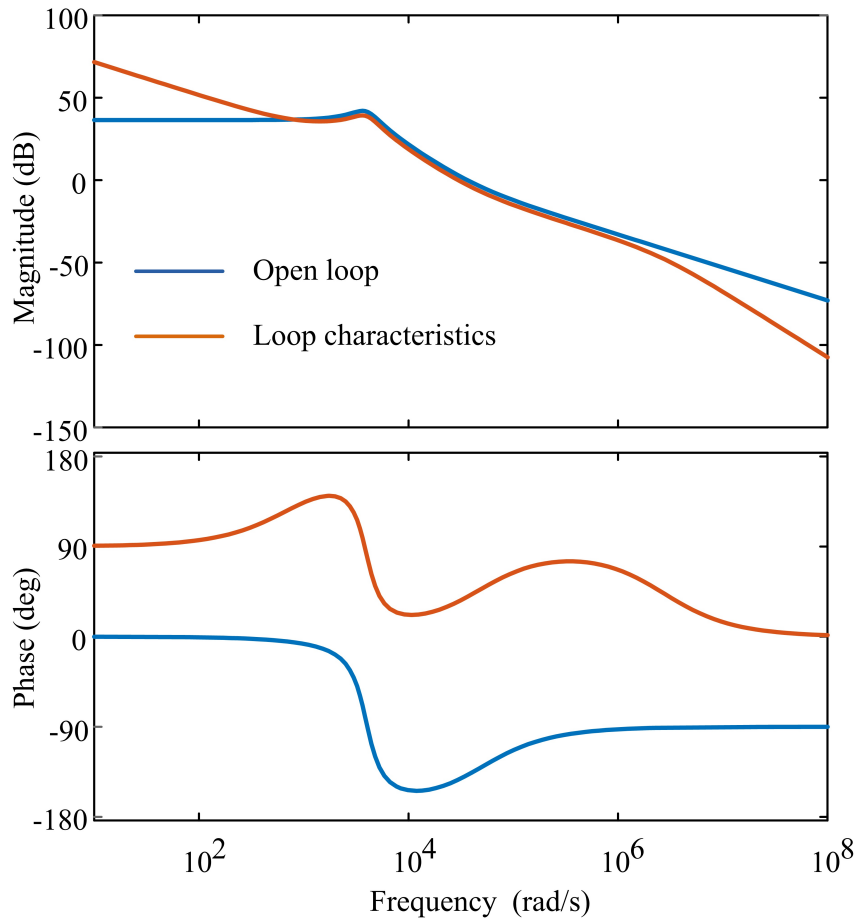


Figure 5.5: Bode diagram of open loop buck regulator

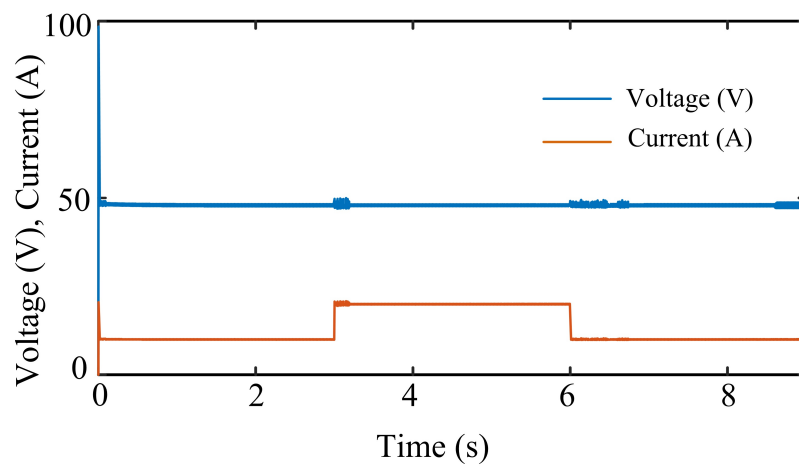


Figure 5.6: Load voltage characteristics during change in load current

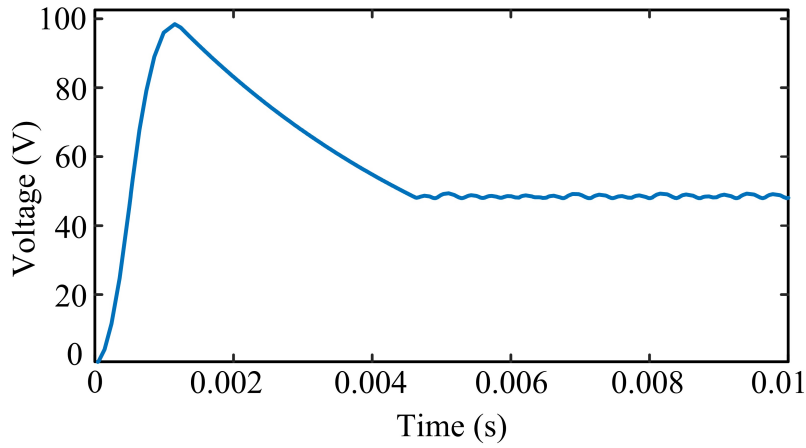


Figure 5.7: Initial response and settling time characteristics of designed compensator

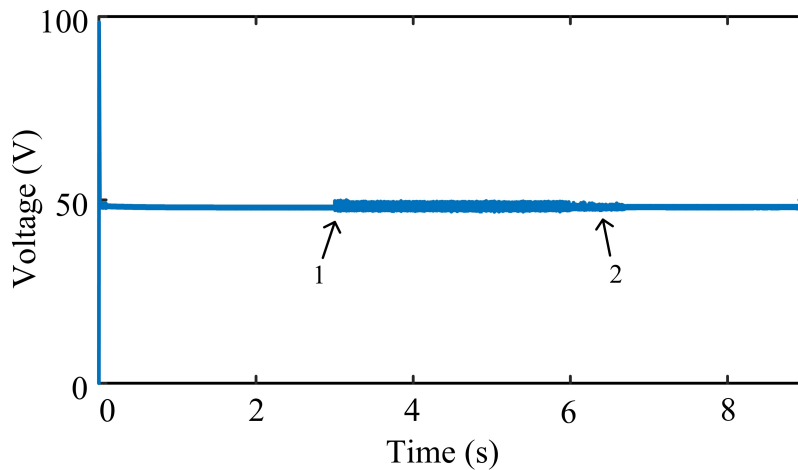


Figure 5.8: Load voltage regulation characteristics for change in DC link voltage

From the load regulation characteristics, it is evident that, response time of the compensator is very fast and it has a settling time of less than 5ms which is shown in Fig. 5.7. Therefore, for the pulsed power operation of BTS, the designed compensator regulates the load voltage actively. The designed compensator is tested for the input voltage (i.e., DC link voltage) variation. The voltage regulation characteristics using the designed compensator is shown in the Fig. 5.8. In Fig. 5.8, at two instants DC link voltage is varied manually for the testing purpose. Initially, the DC link voltage was 300 V, after 3 s (i.e., at instant 1), the voltage is dropped to 250 V and after 6 s (i.e., at instant 2), the voltage again dropped to 220 V. At both the instants the developed compensator maintained the output voltage constant at 48 V. Generally,

the DC link voltage does not vary, however, for testing the designed compensator change in DC link voltage is considered. From the test results shown, it is clear that closed loop system is always stable for load and input voltage variations and response time of compensator is very fast.

5.3 SUMMARY

In this chapter, a type II compensator is designed and developed to regulate the voltage at the DC loads of BTS. To design the compensator with required loop characteristics, buck converter transfer function is derived and frequency response is plotted. To design the compensator parameters, K factor method is used. Moreover, for the fast response time, higher (F_0) is selected to design the compensator. The designed closed loop system is tested for the 50% load variation and 10% dc link voltage variation. From the results, it is clear that the system is always stable and the response time is around 5ms, which is less than the typical BTS load variation time. The designed compensator is tested in MATLAB/Simulink platform.

Chapter 6

CONCLUSIONS AND FUTURE SCOPE

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6.1 GENERAL

The main objective of this investigation has been to design and develop a high efficient dual-input DC-DC converter topologies for telecom load applications. At the same time it is aimed to explore novel configurations and power sharing control schemes for proper utilization of renewable energy sources. Further, it is aimed to design and develop a bidirectional DC-DC converter topology for charging the battery and discharge whenever required by the load. A brief summary pertaining to different aspects of work are presented at the end of each chapter. A summary of main conclusion from each chapter is presented in this chapter, which is followed by suggestion for further work in this research area.

6.2 CONCLUSIONS

This report is mainly focusing on the design and development of different dual-input converter topologies for telecom load. The main conclusive remarks, and the future works of this thesis are presented as follows:

Chapter 1 presents the background of the thesis, conventional and PV based power supply configurations of telecom station. A brief description of PV array, characteristics of the PV array, biomass power, and multi-input converter topology with different Li-Ion battery technologies is presented.

In chapter 2, compressive review related to multi-input converter topology, bidirectional DC-DC converter topology and telecom load profile is presented. Furthermore, identified research gaps and research objectives of this study is presented.

Chapter 3 presents two modular dual-input converter topologies with a bidirectional DC-DC converter for battery charging. The presented modular based DC-DC step down converter has the superiority of delivering power from both the sources to load independently and simultaneously. A FPGA based digital control algorithm is preferred for generation of PWM using DSP builder aids an advantage in simple closed loop control. The results presented shows that the proposed modular converter is best suited for high current and low voltage application. A comprehensive comparison of various topologies is done to signify the dominance of the proposed converter over other topologies. Further, a modified modular dual-input based full-bridge DC/DC converter is presented. The developed converter configuration can be operated over

an extended range phase shift ratios between the input source converters to gain the significant ranges of the output power with regulated voltage and proper load sharing. A prototype has been developed and extensive tests have been conducted to validate the steady state and simulation analysis. It is evident that proposed converter configuration has the superiority of delivering power from both the sources to load independently and simultaneously with zero voltage turn on of switches and reduced circulating currents consecutively alleviates the issue of magnetic short circuit condition. These significant characteristics of the proposed modified modular dual-input converter configuration can be utilized as a promising multi-input configuration to integrate the different renewable sources and load by achieving regulated output with reduced losses. Further, For charging the battery from 300 V to 48 V and to discharge the battery to meet requirement of load a bidirectional converter is designed and developed with minimum number of switches. CC/CV mode of control algorithm has been implemented for charging of battery for achieving higher efficiency and protection of battery. The current of battery charging is controlled by the output current control loop and has low output voltage ripple that leads to high efficiency of system.

Chapter 4 presents modular dual-input half bridge DC-DC converter topology is presented. The presented converter configuration has the superiority of delivering power from both the sources to load independently and simultaneously. It provides galvanic isolation between both the source and load, zero voltage turn on of switches, proper load sharing and power flow, reduced circulating currents and alleviates the issue of magnetic short circuit condition, etc. The presented dual-input converter configuration can be operated over an extended range phase shift ratios between the input sources converters to gain the significant ranges of the output power with regulated voltage.

Chapter 5 presents the Type II compensator to regulate the voltage of DC loads of BTS. To develop the Type II compensator, frequency response of open loop regulator (i.e., Buck DC-DC converter) is plotted and based on the gain and phase characteristics, the control loop with required loop characteristics is developed. The developed closed loop system is tested in MATLAB/Simulink platform for different load and input voltage variation conditions and the results show that the system is always stable and having a fast response time.

6.3 FUTURE SCOPE

Based on the research carried out in this report, the recommendations for the future research are presented.

1. Efficiency of the modular dual-input DC-DC converter can be further improved by improvising the controller and phase shift modulation technique.
2. Circulating power between the port has been minimised by proper power sharing control strategy. Further, an appropriate control scheme for power sharing controller can be developed.
3. Bidirectional DC-DC converter can be achieved with ZVS/ZCS mode of operation, thereby improves the complete system efficiency.
4. Experimental validation of type II compensator for tight voltage regulation can be realized using digital controller.

Appendix A

EXPERIMENTAL SETUP FOR MODULAR DUAL-INPUT CONVERTER

In this section description of experimental setup used for validating the modified modular dual-input converter is presented. The experimental prototype formed by a DC-DC two full-bridge converters, a battery bank of 7.5Ah 48 V (Assumed to be constant DC linkvoltage), FPGA controller board (EP4CE30F2C7) and HFT. The specifications of the FPGA board and VHDL coding is presented in Appendix B. The switching frequency of converter is 20kHz. For measuring the Idc link, an accurate Hall effect based sensor (LA-25P) is used. An optocoupler (MCT2E) is used to provide isolation between the FPGA and switch gate driver (MIC4452). Fig. 1 shows the experimental prototype used for validating the modular dual-input converter .

Specification of IGBT Modules	
Specifications	Rating
Stack type Number	MD B6CI600/415-40F
DC Voltage	$V_{dc} = 600$ V
Output AC Voltage	$V_{ac} = 415$ V
Output Current	$I_{ac} = 40$ A
Output frequency	$F_{ac} = 50$ Hz
Switching frequency	$F_{sw} = 50$ kHz
Ambient Temperature	$T_{amb} = 50$ deg C
Colling method	Forced Air Cooled

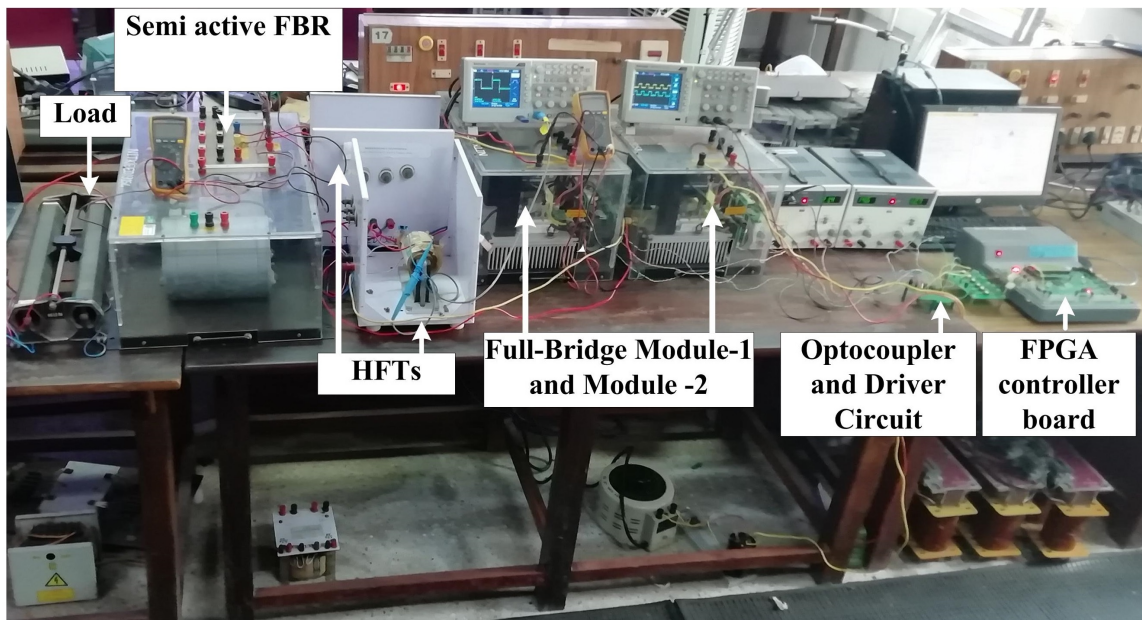


Figure A.1: Experimental prototype for the developed modular dual input converter.

Appendix B

FPGA CONTROLLER BOARD

Steps for execution of programme:

1. Write the code for generation of PWM in VHDL/VERILOG programming language.
2. Run the program in Altera Quatrus software to check any errors in the programme.
3. Once the program is ready to work without any error Dump the program in the DSP builder by using HDL import block as shown in Figure 2.
4. Then compile the programme using signal compiler.
5. Once the compilation of the programme is finished. The PWM can be checked in P11 connector in the FPGA board.

Programme for generation of PWM

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
```

– Uncomment the following library declaration if instantiating
– any Xilinx primitives in this code. –library UNISIM;
–use UNISIM.VComponents.all;

```
entity pwmbi is
Port ( CLK : in STD_LOGIC;
PWM1 : out STD_LOGIC;
PWM2 : out STD_LOGIC;
PWM3 : out STD_LOGIC;
PWM4 : out STD_LOGIC);
```

```
end pwmbi;
```

```
architecture Behavioral of pwmbi is Signal cc :integer:=0;
```

```
begin
process(clk)
begin if rising_edge(clk)then
ccj=cc+1;
if(cc=1000)then
cc<=0;
end if;

if(cc>0 and cc<= 400)then
pwm1<='1';
elsif(cc>400 and cc<= 800)then
pwm1j='0';
elsif(cc>800 and cc<= 1000)then
pwm1<='0';
end if;

if(cc>0 and cc<= 450)then
pwm2<='0';
elsif(cc>450 and cc<= 900)then
```

```
pwm2<='1';  
elseif(cc>900 and cc<= 1000)then  
pwm2<='0';  
end if;
```

```
    if(cc>0 and cc<= 400)then  
pwm3<='1';  
elseif(cc>400 and cc<= 800)then  
pwm3<='0';  
elseif(cc>800 and cc<= 1000)then  
pwm3<='0';  
end if;
```

```
    if(cc>0 and cc<= 450)then  
pwm4<='0';  
elseif(cc>450 and cc<= 900)then  
pwm4<='1';  
elseif(cc>900 and cc<= 1000)then  
pwm4<='0';  
end if;  
end if;  
end process;  
end Behavioral;
```

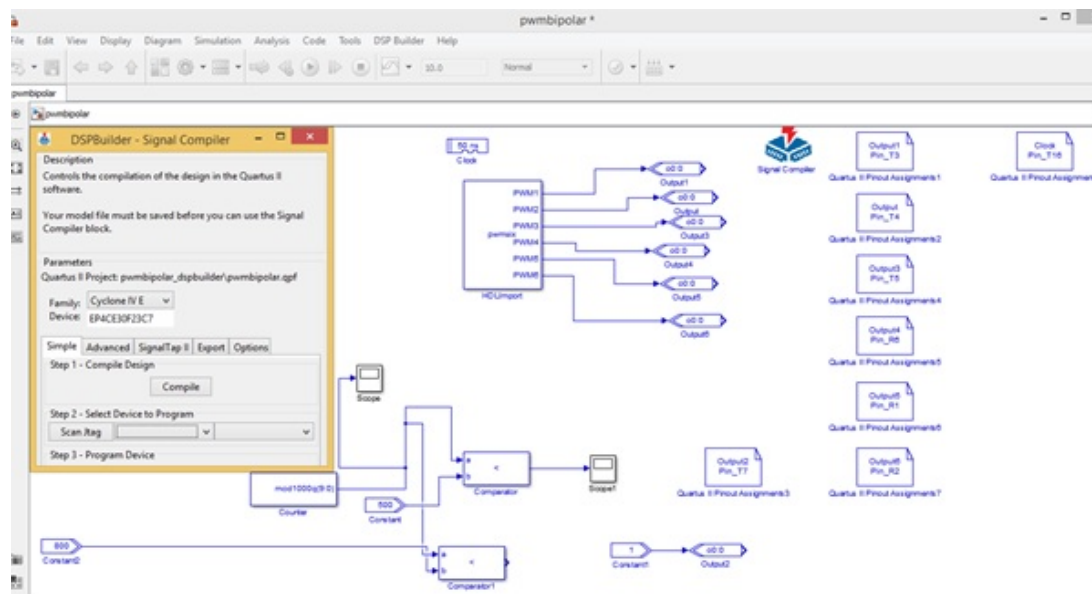


Figure B.1: FPGA closed loop controller design using DSP builder

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PUBLICATIONS BASED ON THE THESIS

Papers in Refereed Journals/Conferences

Papers published

Journals/Transactions

- [1.] Kiran R, R Kalpana, “An Isolated Dual-Input Half-Bridge DC–DC Boost Converter With Reduced Circulating Power Between Input Ports,” *IEEE Canadian Journal of Electrical and Computer Engineering*, vol. 45(1), pp.68-76, 2022.
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Book-Chapter

[1.] R Kalpana and Kiran R, ”Performance Evaluation of Multi-Input Converter Based Battery Charging System for Electric Vehicle Applications” ” *Power Electronics for Electric Vehicles and Energy Storage: Emerging Technologies and Developments-CRC Press, Taylor and Francis group.*

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