2018 31th International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems

Single Inductor Dual Output Buck Converter for Low Power Applications and its Stability Analysis

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***Abstract*—The applications like sensor nodes and wearables, which run on coin/button cell and/or harvested energy source need small form factor and very low power consumption. A single inductor multiple output (SIMO) converter provides saving on inductor count and hence becomes a right choice for such applications. This paper presents a single inductor dual output (SIDO) buck converter targeting light load applications. The architecture uses discontinuous conduction mode (DCM) with pulse frequency modulation (PFM) control and the switching scheme ensures almost zero cross-regulation. The proposed converter is simulated in 180 nm CMOS technology showing zero cross-regulation. An efficiency of above 88% is achieved considering inductor and package losses in load range of micro-amperes to a few milli-amperes. This paper also presents a detailed stability analysis and model for the selected SIMO architecture along with some interesting observations and inferences derived from this analysis.**

***Index Terms*—Low power, DC-DC converter, buck, SIMO, stability, DCM, PFM, IAC**

I. Introduction

Most of the ultra-low power systems, for example sensor nodes and wearable products, running on coin/button cell and/or harvested energy source utilize duty-cycling of the active mode and spend majority of the time in sleep mode. These systems have sleep mode current consumption in few micro-amperes, while in active mode, current consumption can be in few tens of milli-amperes (mostly limited by supply source). Along with low power, due to the small form-factor, it is also desirable to keep component count as low as possible for these systems. Power management for these systems needs to provide high efficiency at such low load currents (micro-amperes to milli-amperes range) with minimal number of board components.

This paper discusses selecting appropriate DC-DC converter architecture for such low load current range and uses it to build a zero cross-regulation SIMO DC-DC buck converter to save on inductor count. This paper also analyses the stability of the selected architecture along with validation of the model through simulations which provide interesting inferences.

II. Background

SIMO buck converters provide a more compact solution for applications which demand small form-factor. Many different control and feedback schemes have been proposed [1]–[3]. Typically for the low power applications, the architecture that fits well is PFM control, DCM operation buck converter. Compared to pulse width modulation (PWM), PFM control-loop architecture provides better efficiency at low load currents. Also the DCM operation allows switching between the SIMO outputs during the zero inductor current period. This ensures no interaction between the multiple outputs and hence near to zero cross-regulation. This architecture, its operation and simulation results are discussed in detail in Section III. Ensuring the stability of SIMO loops is very important to guarantee small ripple and regulation of the output voltage especially during load and line transients. Though there has been literature published on DC-DC stability models, most of them discuss continuous conduction mode (CCM) or PWM control architectures [4]–[6]. There are very few publications on PFM control DCM buck converters [7].

Advancing on the existing work, this paper provides more detailed analysis, specifically for the feed-forward path and also provides more intuitive understanding of the path. For the selected architecture, this paper goes on to develop a stability model, provide stability analysis and verify the model accuracy against SPICE simulation. The stability for a PFM control-loop DCM SISO buck converter is analyzed using the injected absorbed current (IAC) method [8], which is then extended to a SIMO buck converter.

III. Proposed SIMO Architecture

In CCM operation, the inductor current remains above zero throughout the switching period, while in DCM, the inductor current reaches zero and stays zero for a portion of the switching cycle as shown in Fig. 1.

Thus, the average inductor current in a cycle in DCM is generally lower than in CCM, making DCM the preferred mode of operation for light loads. Using PFM control during DCM operation would cause the switching frequency to reduce with the load, especially under light load conditions. This reduces the dynamic power at light loads resulting in higher conversion efficiency.

2380-6923/17 $31.00 © 2017 IEEE
DOI 10.1109/VLSID.2018.88

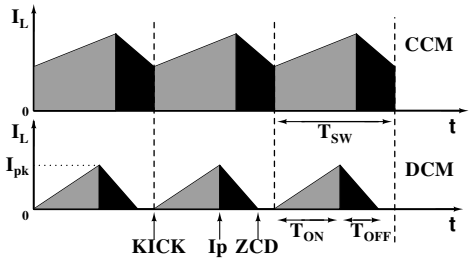

Fig. 1: SISO buck inductor current in CCM and DCM

A. Operation of SISO Buck Converter with Proposed Control Scheme

The block diagram of the sampled loop SISO buck converter operating in DCM with PFM control is shown in Fig. 2. The output voltage V_{out} is compared with the reference voltage $V_{out,ref}$ and sampled at the rising edge of the clock. The charge cycle is initiated only if the output voltage falls below the reference $V_{out,ref}$. Hence it is a need-based charging scheme and the converter does not initiate a charge cycle unless the output demands it. The converter operates in DCM for the entire range of loads and uses PFM control as the charge cycles come at variable intervals of time, depending on the load current. The detailed working is as follows:

By sensing the output voltage and inductor current, we get the signals KICK, Ip and ZCD at the points indicated in Fig. 1.

- KICK signal goes high when the output voltage V_{out} falls below the desired reference voltage $V_{out,ref}$ and starts the charge cycle.
- Ip signal goes high when the inductor current reaches the set current reference value I_{pk}.
- ZCD (zero crossing detect) signal goes high when the inductor current returns to zero.

These signals control the powerFET (pull-up and pull-down) switches that energize and de-energize the inductor during a charge cycle. The sequence of operations (carried out by the Set-Reset Logic block) during one energize/de-energize cycle is as follows:

- KICK makes PC go low, turning on the pull-up (PFET) switch to energize the inductor.
- Ip makes PC and NC go high, turning off the pull-up switch and turning on the pull-down (NFET) switch, de-energizing the inductor.
- ZCD makes NC go low, turning off the pull-down switch and completing the cycle.

Note that while DC-DC switching frequency varies with the load, sampling clock (Clk) is a free running clock with frequency set as per maximum supported load. In this scheme the switching frequency is the same as the KICK frequency. The peak value of the inductor current is maintained constant (equal to the reference I_{pk}) in the SISO operation and in the stability analysis of the sampled loop SISO buck converter described in Section IV.

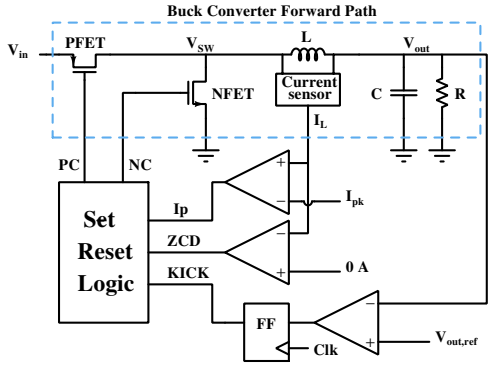

Fig. 2: Block diagram of the SISO buck converter

B. SIMO Buck Converter

SIMO converters can be viewed as circuit extrapolations of corresponding SISO converters [9]. Since all the outputs share one common inductor, variations in one output might affect the others, referred to as cross-regulation. Fig. 3 shows the block diagram of a single inductor dual output (SIDO) buck converter with PFM control.

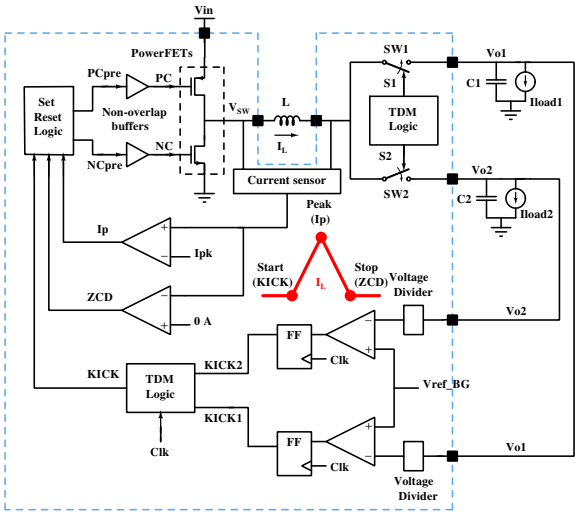

Fig. 3: Block diagram of SIDO buck converter circuit

The SIDO buck converter in Fig. 3 is implemented and verified using SPICE simulator in $180\,\mathrm{nm}$ technology. Since maximum current demands in light load applications are within few tens of milli-amperes, we pick the scheme shown in Fig. 4 to multiplex the inductor current between the outputs. In this scheme, the switching between the two outputs happens only when inductor current is zero. This makes the outputs and their feedback loops independent, with no interaction with each other. As a result, cross-regulation is eliminated and each of the outputs can be treated as two separate SISO converters sharing a common inductor. We refer to this configuration as

time division multiplexed SIDO (TDM SIDO) buck converter. The switching between the two outputs happens on demand basis which means that for equal load on both outputs, they are served in alternate cycles while for unequal loads, the one with the higher load is served more often than the other. This allocation is tracked automatically for varying load current by TDM Logic. SIDO was designed to support a total load current (I_{load1} + I_{load2}) of 50 mA supporting a full range of load combinations i.e. "0 mA+50 mA" to "25 mA+25 mA" to "50 mA+0 mA".

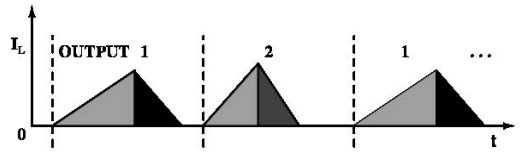

Fig. 4: SIDO buck converter inductor current in DCM

KICK1 and KICK2 signals are combined into a single KICK to control the powerFETs and also generate control signals for output switches SW1 and SW2. As proof of concept, a SIDO buck converter is designed for $V_{in} = 3.6\,\mathrm{V}, V_{o1} = 1.8\,\mathrm{V}, V_{o2} = 1.2\,\mathrm{V}, L = 4.7\,\mu\mathrm{H}, C = 10\,\mu\mathrm{F}, I_{pk} = 130\,\mathrm{mA}$ and Clock (Clk) Frequency = 1 MHz. Fig. 5 shows performance of the converter for V_{in} step with $I_{load1} = I_{load2} = 1\,\mathrm{mA}$. Fig. 6 shows the response when I_{load1} is stepped from 0 to 15 mA and $I_{load2} = 15\,\mathrm{mA}$. Observe that there is no effect of V_{o1} on V_{o2} and vice-versa. This proves that, with the proposed switching scheme, the proposed architecture results in zero cross-regulation.

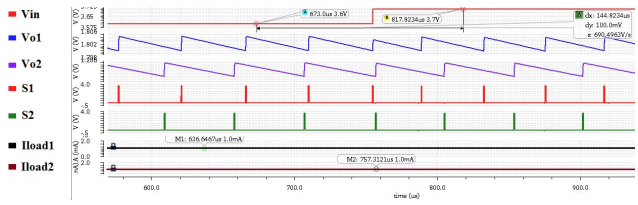

Fig. 5: SIDO buck converter response for V_{in} step

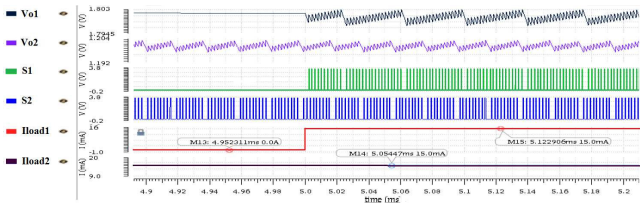

Fig. 6: SIDO buck converter response for load step at one output

Fig. 7 shows efficiency versus total load current ($I_{load1} + I_{load2}$). It includes losses due to inductor and package.

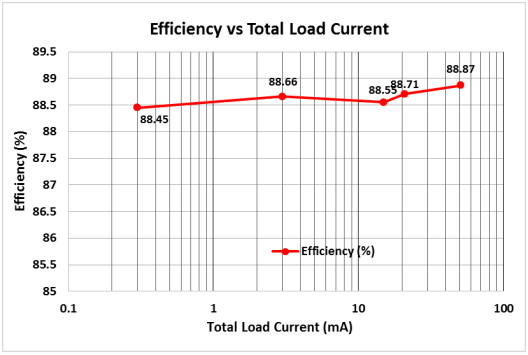

Fig. 7: SIDO efficiency versus total load current

The proposed control scheme can be extended to the design of a SIMO converter with N outputs. In this case, the maximum rate at which charge can be delivered to each output is $\frac{1}{N}$ times the sampling clock frequency. As a result, the voltage ripple at the outputs of the SIMO converter will increase with number of outputs for a given clock frequency. This ripple can be brought down by increasing the clock frequency.

IV. Modeling Of SISO Buck Converter

The stability of the buck converter can be determined from the phase and gain margins of the open loop system. To obtain these margins, a model of the buck converter must be obtained. To obtain a model for the SIMO buck converter, a SISO buck converter is modeled first. The SISO buck converter model can be easily extended to the SIMO buck converter, as will be explained in the following sections.

A. Modeling of Forward Path

There are two popular methods for modeling switched power converters- state space averaging (SSA) [10] and injected absorbed current (IAC) method. For DCM operation, the SSA method requires an additional constraint to account for the discontinuity in the inductor current. Both the methods result in the same transfer function [8]. For ease of algebra, the IAC method is chosen and described in this paper. The SISO PFM buck converter shown in Fig. 2 is modeled as represented in the block diagram shown in Fig. 8. The forward path has two inputs, input voltage V_{in} and KICK frequency F, and a single output V_{out}. The feedback path is modeled with V_{out} as the input and F as its output, thus closing the loop.

V_{in}, F, V_{out} are the nominal values of the operating point over which the circuit is to be linearized. From the geometry of the DCM inductor current waveform shown in Fig. 1 the following steady state equations are obtained:

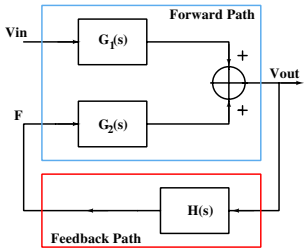

Fig. 8: Block diagram of SISO PFM buck converter

$$I_{L,avg} = \frac{I_{pk}(T_{ON} + T_{OFF})}{2T_{sw}}$$
$$T_{ON} = \frac{I_{pk}L}{V_{in} - V_{out}}$$
$$T_{OFF} = \frac{I_{pk}L}{V_{out}}$$
$$I_{L,avg} = \frac{{I_{pk}}^2 LV_{in}F}{2V_{out}(V_{in} - V_{out})}$$
$$F = \frac{1}{T_{sw}}$$

Taking partial derivatives, linearizing and taking the Laplace transform we get,

$$I_L(s) = \left(\frac{{I_{pk}}^2 LV_{in}}{2V_{out}(V_{in} - V_{out})}\right) F(s) - \left(\frac{{I_{pk}}^2 LF}{2(V_{in} - V_{out})^2}\right) V_{in}(s) - \left(\frac{{I_{pk}}^2 LFV_{in}(V_{in} - 2V_{out})}{2{V_{out}}^2(V_{in} - V_{out})^2}\right) V_{out}(s)$$

For a resistive load, $I_L(s) = V_{out}(s)\left[\frac{1}{R} + sC\right]$ we get,

$$V_{out}(s)\left[\frac{1}{R} + sC\right] = \left(\frac{{I_{pk}}^2 LV_{in}}{2V_{out}(V_{in} - V_{out})}\right) F(s) - \left(\frac{{I_{pk}}^2 LF}{2(V_{in} - V_{out})^2}\right) V_{in}(s) - \left(\frac{{I_{pk}}^2 LFV_{in}(V_{in} - 2V_{out})}{2{V_{out}}^2(V_{in} - V_{out})^2}\right) V_{out}(s)$$

Using the relation $I_{L,avg} = \frac{{I_{pk}}^2 LV_{in}F}{2V_{out}(V_{in} - V_{out})} = \frac{V_{out}}{R}$

$$V_{out}(s)\left[\frac{1}{R}\left(\frac{2V_{in} - 3V_{out}}{V_{in} - V_{out}}\right) + sC\right] = \left(\frac{V_{out}}{RF}\right) F(s) - \left(\frac{{V_{out}}^2}{RV_{in}(V_{in} - V_{out})}\right) V_{in}(s)$$

By setting $F(s) = 0$, we get $\frac{V_{out}(s)}{V_{in}(s)}$ and by setting $V_{in}(s) = 0$ we get $\frac{V_{out}(s)}{F(s)}$.
Thus the transfer functions are:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-\frac{{V_{out}}^2}{V_{in}(2V_{in} - 3V_{out})}}{s\frac{RC(V_{in} - V_{out})}{(2V_{in} - 3V_{out})} + 1} = G_1 \quad (1)$$

$$\frac{V_{out}(s)}{F(s)} = \frac{\frac{V_{out}(V_{in} - V_{out})}{F(2V_{in} - 3V_{out})}}{s\frac{RC(V_{in} - V_{out})}{(2V_{in} - 3V_{out})} + 1} = G_2 \quad (2)$$

It is observed from (1) and (2) that DCM forward path with constant I_{pk} control is a first order system. We also observe a pole at $s = -\frac{(2V_{in} - 3V_{out})}{RC(V_{in} - V_{out})}$. When $V_{out} > \frac{2V_{in}}{3}$, the pole moves to the right half of the s-plane and causes the forward path to become unstable, as mentioned in [7]. The derivation is repeated assuming current source load (I_{load}) instead of a resistor. The transfer function takes the form as given in (3).

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-\frac{{V_{out}}^2}{V_{in}(V_{in} - 2V_{out})}}{\frac{V_{out}C(V_{in} - V_{out})}{I_{load}(V_{in} - 2V_{out})}s + 1} \quad (3)$$

We observe that with current source load, the pole is at $s = \frac{-I_{load}(V_{in} - 2V_{out})}{CV_{out}(V_{in} - V_{out})}$. For this case, the pole moves to the right half of the s-plane when $V_{out} > \frac{V_{in}}{2}$. Following are interesting observations from the forward path transfer functions, followed by the MATLAB simulations of the transfer functions and validation against circuit SPICE simulations.

1) From (1) and (2) we can say that the forward path model resembles a simple first order RC circuit with transfer function of the form $\frac{A}{1 + \frac{s}{\omega_p}}$, where $\omega_p = \frac{1}{R_{eq}C}$. For a resistive load, $R_{eq} = \frac{R(V_{in} - V_{out})}{(2V_{in} - 3V_{out})}$.
2) For the positive equivalent resistance (R_{eq}) i.e. $V_{out} < \frac{2V_{in}}{3}$, the resistance drains charge out of the capacitor and the charge does not build up as can be seen from Fig. 9-12, and the corresponding values are tabulated in TABLE I and TABLE II.
3) For $V_{out} > \frac{2V_{in}}{3}$, R_{eq} is negative. This means that charge is continuously pumped into the capacitor. The voltage across the capacitor rises exponentially to V_{in}, thus leading to instability. The instability indicated by the derived model is verified by setting V_{out} accordingly in SPICE simulations. Due to the inversion in the $\frac{V_{out}(s)}{V_{in}(s)}$ transfer function, when V_{in} is stepped down, V_{out} rises continuously and saturates at V_{in}. This is shown in Fig. 13, where $V_{out} = 2.4\,\text{V} = \frac{2V_{in}}{3}$ and V_{in} is stepped from 3.6 V to 3.55 V. If V_{in} is stepped up, V_{out} decreases and tries to exponentially decay down to zero. Eventually, V_{out} falls below $\frac{2V_{in}}{3}$, hence entering the stable region and settles at the new steady state. This is shown in Fig. 14, where $V_{out} = 3\,\text{V} > \frac{2V_{in}}{3}$ and V_{in} is stepped from 3.6 V to 3.65 V. In both these cases the converter in open loop is unstable since V_{out} is drifting away from its desired level by a large amount due to a small perturbation.
4) Assuming a current source load, $R_{eq} = \frac{V_{out}(V_{in} - V_{out})}{I_{load}(V_{in} - 2V_{out})}$. Negative equivalent resistance (R_{eq}) arises for $V_{out} > \frac{V_{in}}{2}$. Which means, forward path with a resistive load is stable for a wider range of V_{out} than with a current source load. Since it is a first order system, the only source of instability is accumulation (or loss) of charge causing the voltage to rise (or fall) continuously and driving the system to saturation. Current drawn by a

resistive load is a function of V_{out}. For rising V_{out}, current (charge) drawn by the resistive load increases, thus draining charge accumulated on the V_{out} node. In case of current source load, the current (charge) drawn remains constant and so charge accumulation cannot be counteracted. Hence, the range of voltages for stable operation for the two loads is justified.

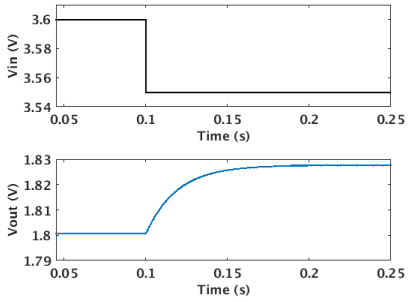

Fig. 9: SPICE simulation of forward path for V_{in} step

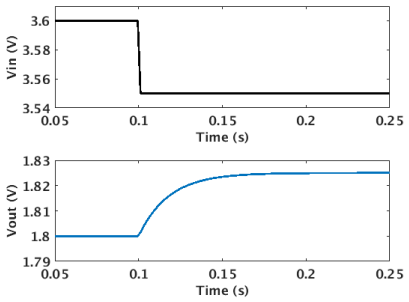

Fig. 10: Response of forward path transfer function in MATLAB for V_{in} step

TABLE I: Observations from transient simulations for V_{in} step in MATLAB and SPICE simulator

$V_{out}(V)$	DCgain		Rise time (ms)	
	MATLAB	SPICE	MATLAB	SPICE
1.2	-0.11	-0.112	17.75	17.2
1.6	-0.29	-0.31	29.3	29.5
1.8	-0.5	-0.53	39.73	42.35

TABLE II: Observations from transient simulations for F step in MATLAB and SPICE simulator

$V_{out}(V)$	DCgain		Fall time (ms)	
	MATLAB	SPICE	MATLAB	SPICE
1.2	3.972×10^{-5}	3.979×10^{-5}	17.6	17.4
1.6	5.972×10^{-5}	5.862×10^{-5}	29.3	29.0
1.8	7.943×10^{-5}	7.384×10^{-5}	39.6	35.3

B. Modeling of Feedback Path

The feedback path (H) consists of a continuous comparator followed by a latch, which sample the output at the rising edge

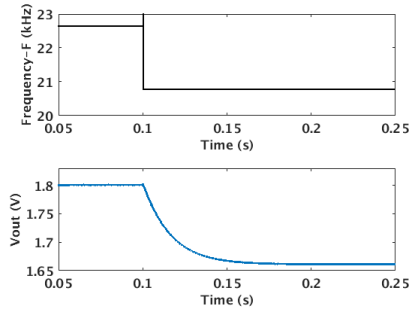

Fig. 11: SPICE simulation of forward path for F step

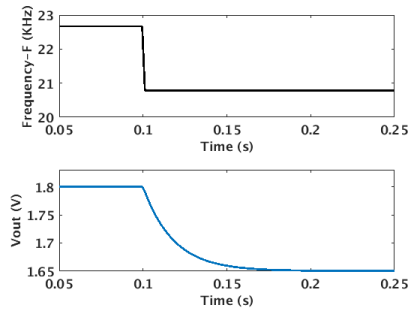

Fig. 12: Response of forward path transfer function in MATLAB for F step

of the clock. The clock frequency is always set much larger than the required powerFET switching frequency. Also the delay (lag) from the comparator and latch are comparatively very small. This means that for any small change in V_{out}, there is an instantaneous and large change in KICK frequency (F). Hence the feedback path can be safely assumed to be continuous, having a very large gain and bandwidth. Therefore the feedback path is modeled as a block with very high gain and no poles. For simulation purposes, the feedback path model is taken as a constant scaling factor $H = 10^{10}$.

The pole-zero plot of the closed loop system is shown in Fig. 15. Due to the large feedback factor, the location of the closed

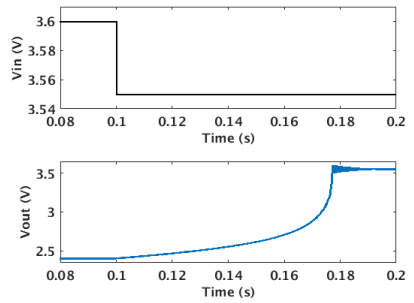

Fig. 13: SPICE simulation of forward path for V_{in} step down at $V_{out} = 2.4\,\mathrm{V}$

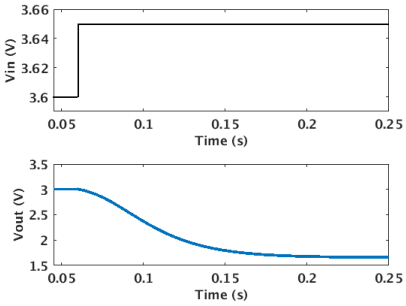

Fig. 14: SPICE simulation of forward path for V_{in} step up at $V_{out} = 3\,\mathrm{V}$

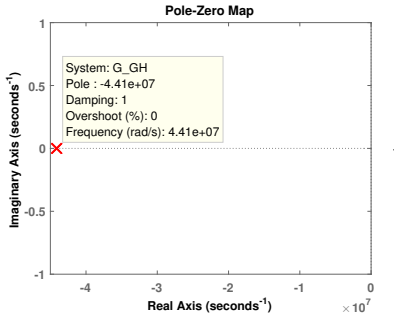

Fig. 15: Pole-zero plot of closed loop buck converter

loop pole is fixed irrespective of the load conditions. From SPICE simulations, we observe that the transient response of the closed loop SISO buck converter with PFM control is the same for all supported load currents.

The SISO buck converter forward path model has a first order transfer function whose gain starts from below $0\,\mathrm{dB}$ and the gain and phase margins are infinite for $V_{out} < \frac{2V_{in}}{3}$. For $V_{out} > \frac{2V_{in}}{3}$, the pole moves to the right half of s-plane, thus making the forward path unstable.
Open loop pole $(\omega_0) = \frac{-(2V_{in}-3V_{out})}{RC(V_{in}-V_{out})}$,
Gain $(A) = \frac{-{V_{out}}^2}{V_{in}(2V_{in}-3V_{out})}$,

When the loop is closed with very large feedback factor ($H = \infty$ ideally), the transfer function reduces to $\frac{G}{1+GH} = \frac{1}{H}$. Setting H to infinity makes the transfer function go to 0. Thus the output remains unaffected by perturbations in the input as can be seen in Fig. 5 and the closed loop SISO buck converter is stable under all operating conditions.

V. SIMO Buck Converter Stability

The SISO buck converter stability model can be extended to the SIDO buck converter architecture described in this paper. The switching between the SIDO's two outputs happens only when inductor current is zero, ensuring non-overlap of output switches. This makes the two outputs and their feedback loops independent, with no interaction with each other. The outputs can be treated as two independent SISO converters sharing a common inductor. Each output is given a charge cycle at a rate proportional to the load it needs to support. Since the SISO buck converter is stable, the discussed SIDO buck converter is also concluded to be stable.

VI. Conclusion

The TDM SIMO approach was chosen to design a SIDO buck converter operating in DCM as this eliminates cross-regulation and enables highly asymmetrical loads to be supported at the outputs. The SIMO buck converter switches between its multiple outputs during the zero inductor current time. So, the SIMO buck converter can be analyzed as multiple SISO buck converters that are independent of each other. A SISO DC-DC buck converter operating in DCM PFM has been modeled. This model is also verified using MATLAB and SPICE simulations by comparing DC gain and rise/fall time. It is proved that closed loop SISO buck converter is stable under all operating conditions. By extension of the SISO buck converter stability derivation, the SIMO buck converter is also concluded to be stable.

Acknowledgments

The authors would like to thank Mahesh Mehendale from Kilby Labs at Texas Instruments for his guidance and crucial feedbacks during the course of this project. The authors would also like to thank the Ministry of Electronics & Information Technology (MeitY), Government of India, for providing EDA tools through SMDP-C2SD Project.

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