The design of an area efficient segmented DAC

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***Abstract*- DAC architectures reported in the literature use segmentation schemes involving more thermometer and less binary bits, in order to guarantee a better dynamic and static performance. In this paper, a novel technique is proposed to minimize the glitch in the binary section of a segmented current steering DAC through the custom design of latches. This enables more bits in the binary section of the segmented DAC than what is reported in the literature. Using the proposed technique, a 12 bit 400MSPS current steering DAC with 8 bit binary section and 4 bit thermometer section is designed using AMI 350 nm n-well CMOS process. A 12 bit segmented DAC with 8 MSB thermometer section and 4 binary section is also designed using the conventional approach. The static and dynamic performance of the above two segmented DACs are obtained through ELDO SPICE simulations. From these, it is found that the INL, DNL and SFDR at 1 MHz for the proposed DAC are 0.7 LSB, 0.65 LSB and 79 dB whereas those of the conventional segmented architecture are 0.63 LSB, 0.04 LSB and 87 dB respectively. With only marginal degradation in the static and dynamic performance, the proposed DAC results in lower silicon area and routing complexity. The reduction in the digital decoder area and the no. of latches required for the proposed DAC enables higher update rate for the DAC. The estimated area of the proposed DAC is about 30% times less than that using the conventional segmentation scheme.**

***Keywords*— Binary, Current Steering DACs, Thermometer decoder, Latch, INL, DNL .**

I. INTRODUCTION

The advancements in the silicon process technology enable the implementation of a complete system consisting of both digital and analog blocks including D/A and A/D converters on a single chip. Single chip solutions for applications such as ultra wideband networks and software defined radio require the individual sub systems such as D/A and A/D to be designed for high speed operation. In view of these, the design of D/A with better update rate becomes important.

Current Steering DACs (CS-DACs) are preferred for high speed applications such as WLAN, WMAN, HDTV and other related applications [1]-[7]. Moreover, they have a no. of other advantages such as lower power dissipation and lower cost than other architectures. However, CS-DACs have a no. of limitations such as poor INL and DNL, poor SFDR and SNR performances. This arises due to device mismatches, mismatch in the speed of current steering between binary and thermometer sections and asymmetry in the settling times of various current sources [8].

Static performance of DACs is quantified by INL and DNL. Their dynamic performance can be inferred from the SFDR (Spurious Free Domain Range) and SNR (Signal to Noise ratio) characteristics. Static and dynamic performances determine the effective number of bits (ENOB).

In general, the segmented DACs use binary bits for the LSBs and thermometer bits for the MSBs. In the literature, a segmented DAC with a greater number of bits in thermometer section than that in the binary section is preferred in order to obtain better dynamic and static performance [6]. However, this is achieved at the cost of more silicon area and complexity in clock synchronization. To overcome this, a novel technique is proposed in this paper to design a segmented CS-DAC with more no. of bits in the binary section without undue degradation in the static and dynamic performance.

The organization of the paper is as follows: Section II presents the design guidelines of the conventional DAC architecture and discusses the limitations of using more number of thermometer bits than binary bits and also the justification for exploring a new scheme of segmentation. Section III discusses the design of the improved DAC architecture- the unit cell structure and the custom design of latches. Section IV explains the integration of the thermometer bits with the 8 bit binary DAC to obtain the proposed DAC. Section VII discusses the simulation results obtained from the ELDO-Spice tool. Section VIII concludes this discussion, capturing the highlights of this suggested architecture.

II. CONVENTIONAL DAC ARCHITECTURES

A segmented N bit CS-DAC typically uses N1 MSB and N2 LSB bits in the thermometer and the binary sections respectively. The thermometer section uses $2^{N1}-1$ unary current sources each of strength $2^{N2} I_{lsb}$, and the binary section uses N2 current sources of binary weighted strengths from I_{lsb} to $2^{(N2-1)} I_{lsb}$. I_{lsb} denotes the current corresponding to the least significant bit of the DAC.
An estimate for the INL [4] is given by

$$\text{INL} = \sqrt{2^{(N-2)}}\,\frac{\sigma(I)}{I}\,\text{LSB} \qquad (1)$$

INL is independent of the segmentation scheme used. However, DNL is dependent on the segmentation adopted and the worst case DNL, occurs at the mid code transition and is given by (2)

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$$\text{DNL} = \sqrt{2^{(N2+1)} - 1}\,\frac{\sigma(I)}{I}\,\text{LSB} \qquad (2)$$

The normalized digital and analog area required for various percentage of segmentation is studied in [6] and is shown in Fig.1. In this figure, 0% segmentation corresponds to the full binary DAC and 100% segmentation corresponds to the full thermometer DAC. The analog area required for an optimum DNL varies from 4096* A_{unit} for the pure binary DAC to A_{unit} for the thermometer DAC. The analog area required for an optimum INL<=0.5 LSB is 1024* A_{unit}, while a more relaxed constraint of INL<=1LSB results in an analog area of 256* A_{unit}. The digital area varies as $2^P A_d$ for P bits in the thermometer section. The cumulative area, assuming the approximate equivalence of A_{unit} and A_d [6], results in a graph where the analog area for optimum DNL dominates for binary DACs, analog area for optimum INL dominates for moderate segmentations, and the digital area dominates for thermometer DACs.

In order to obtain better static performance without undue increase in area, the optimum point for segmentation is chosen such that analog area becomes equal to digital area as shown in fig.1.[6]. This implies more bits in the thermometer section. However, the dynamic performance of DAC degrades with increase in the number of bits in the thermometer section. [9].

Moreover, more bits in thermometer section results in larger digital area, larger output capacitance and larger complexity of the design [9]. These in turn lead to greater timing inaccuracy, synchronisation and matching problems and larger charge feed through to the output . Further, increase in the decoder complexity increases the critical path delay and hence reduces the speed of operation of the DAC. Only if timing accuracy is guaranteed better performances can be obtained from an increased segmentation. At low frequencies the conductance of the DAC is also reduced when more thermometer bits are used.

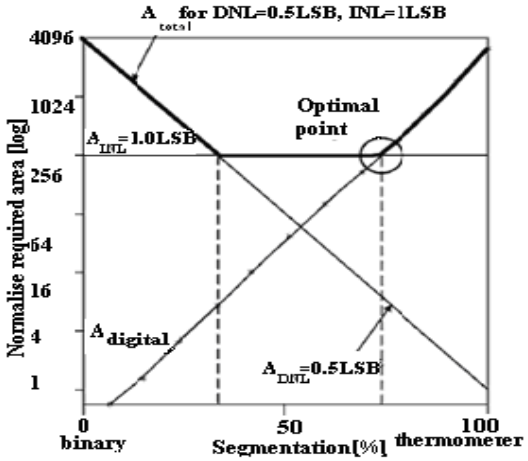

Fig.1. Normalised required area vs % of segmentation

III. DAC IMPLEMENTATION

The segmented DAC block diagram is shown in Fig. 2. The construction of the 8 bit pure binary DAC is discussed in this section. Each of the current source, cascode transistors and their associated switches in Fig. 3 is referred to as a current cell. The major blocks of the 8 bit binary DAC are the bias voltage generation circuitry, the weighted current cell (I_{lsb} to 128*I_{lsb}), and the custom designed latch, whose outputs are fed to the gates of the switching transistors of the weighted current cell. These blocks are discussed in detail in the following sub-sections.

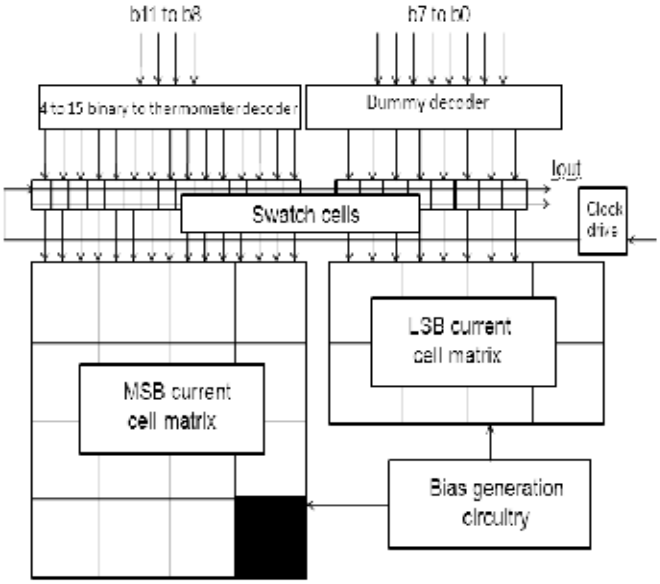

Fig.2. Segmented DAC block diagram

A. Bias Generation Circuitry

The high swing cascode Bias Generation circuitry that produces the required bias voltages V_{b1} and V_{b2}. The bias generation circuitry used is one that allows greater swing at the drain of the cascode transistor of the current source, while generating highly stable bias voltages to be supplied to the gates of the current source transistor and its cascode transistor. The overdrive voltage is set as 0.3 V, which then determines the value of W/L in the square law equation for the drain current.

$$I = \frac{K}{2}\frac{W}{L}V_{od}^{cs2} \qquad (3)$$

B. Unit cell

Fig. 3 shows the schematic of the unit cell. It consists of a cascoded current source section and a differential switch section. The cascoded current sources are used because they inherently provide greater current transfer accuracies and also higher output impedances [10]. The analog area required for guaranteed static performance under statistical variations is given in [4]

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$$W * L = \frac{1}{\frac{2\sigma^2}{I^2}}\left[A_\beta{}^2 + \frac{4A_{VT}{}^2}{\left(V_{GS} - V_T{}^2\right)} \right] \quad (4)$$

This equation that relates the value of area of the current source transistor, to the value of $\frac{\sigma(I)}{I}$, gives the value of WL. This gives us better matching and also less sensitivity to layout sizing errors. On solving (3) and (4) simultaneolusly, the value of W and L can be determined. The minimum voltage required at the drain of the cascoded transistor is 0.6 V, thus allowing for a larger swing at the output nodes.

The differential switch section consists of four transistors- two switches, and two cascodes to the switches. The gates of the switching transistors are given the complementary outputs from the corresponding latches. The gates of the cascodes are always connected to the supply rail, and separate the switching transistors from the output nodes, thereby reducing the clock feed through.

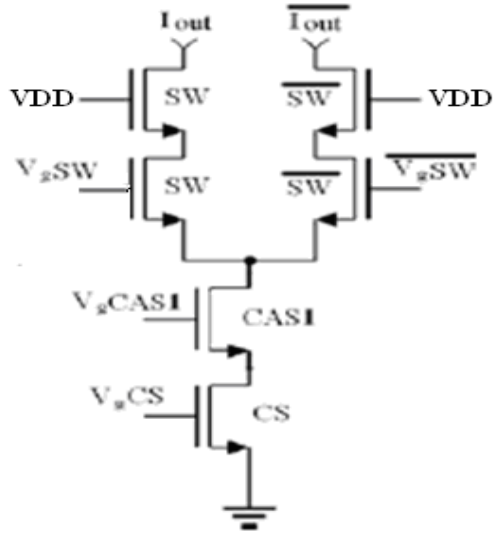

Fig 3. Unit cell schematic

C. Custom design of latches

As seen from the argument presented in [9], it can be concluded that, one can explore a segmentation of lower percentage, involving greater number of binary bits, with some sacrifice in DNL/INL performance, but on less chip area and with better timing accuracy. A segmented DAC involving 4 MSB thermometer and 8 LSB binary bits is constructed, wherein the static performance of the binary section is improved by custom design of latches.

Toward that end, we take into consideration the propagation delay through the latch-switch combination. Approximating the switching transistor with large signal MOS model, we represent it as a parallel combination of R_{eff} and C_{eff}.

As we proceed from the I_{lsb} to 128* I_{lsb} in the binary section of the DAC, it is seen that a greater switch size is required in order to allow the flow of a greater amount of current. In such a situation, the value of the switch width increases, thus increasing the capacitances that need to get charged/discharged. This means the R_{eff} * C_{eff} time constant increases, resulting in an increase in the propagation delay through the switch from I_{lsb} to 128 I_{lsb}.

This implies a custom design of latches has to be done, in such a manner so as to keep the propagation delay through the latch that switches the 128*I_{lsb} current source minimum, and the propagation delay through the latch that switches the I_{lsb} current source maximum.

The latch is essentially a pair of cross-coupled inverters, and as seen from the figure, the propagation through them boils down to the propagation delay analysis as presented in [10]. The equation that relates the T_P is

$$T_P = \frac{1.6C}{\beta V_{DD}} \quad (5)$$

Here, it is seen that, a greater width will result in a lesser propagation delay. The same relation holds for the latch that is viewed only as a pair of cross coupled inverters. Thus, the widths of the transistors in the latches are sized up from I_{lsb} to 128* I_{lsb}. In effect, the propagation delays through the switches increases from I_{lsb} onwards, while the propagation delays through the latches decreases. This helps achieve synchronisation of propagation delays through the latch-switch combinations, thus reducing significantly the number and magnitude of glitches. Hence all timing related errors degrading the static performance are nullified. Table 1 shows the propogation delays of latch – switch combinations for various bit position.

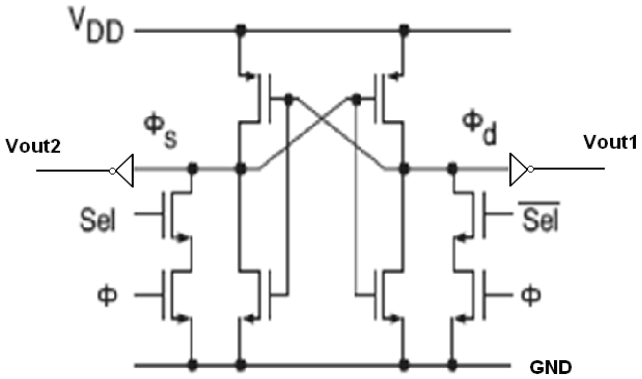

Fig. 4. Latch schematic

TABLE 1. Latch – Switch Propagation Delays

Bit position	Latch (ps)	Switch (ps)	Overall (ps)
0	157.1	174.4	245.8
1	157.1	162.3	236.9
2	157.1	156.1	231.9
3	167.4	165.2	254.3
4	175.7	165.4	254.3
5	163.6	168	244.2
6	160.9	174.8	248.7
7	158	190.7	255.1

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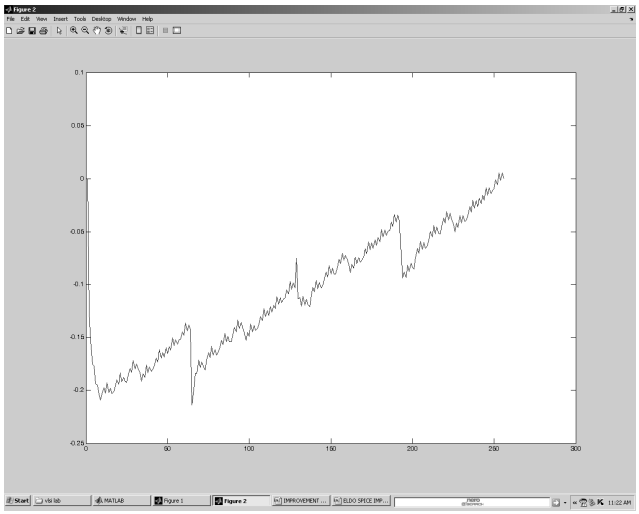


Fig. 5. An 8 bit binary INL

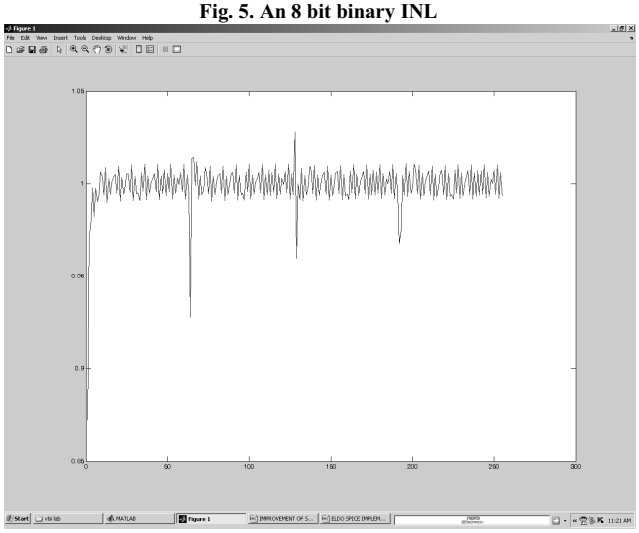


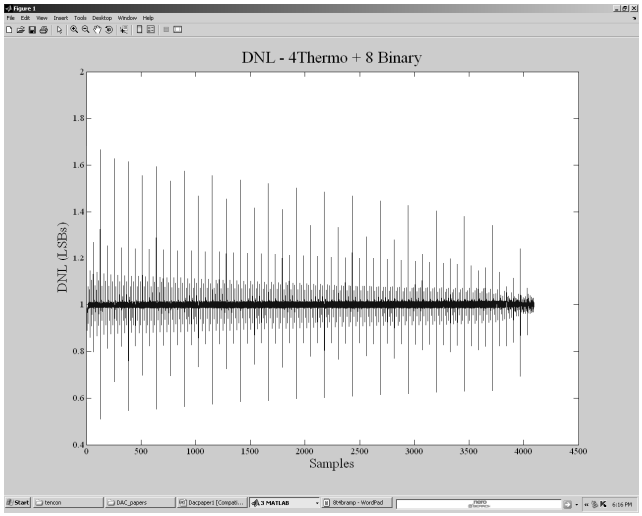
Fig. 6. An 8 bit binary DNL

IV. INTEGRATION WITH THERMOMETER SECTION – THE 12 BIT DAC

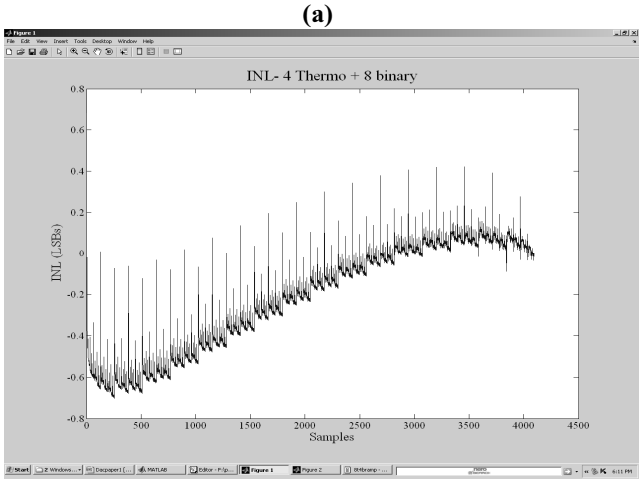
Having generated the 8 bit binary DAC, its integration with the 4 bit thermometer section is considered, to obtain the 12 bit segmented DAC. b_{11} and b_{10} are passed through a 2 binary to 3 thermometer row decoder and b_9 and b_8 are passed through another 2 binary to 3 thermometer column decoder, to obtain 6 signals in all. These signals are further passed through a row column decoder in order to activate 15 thermometer current sources, each of value 256 I_{lsb}. However, since the critical path length is longer for the thermometer bits, a dummy decoder is used for the binary bits, to help equalize the path delays for the thermometer and the binary bits.

V. SIMULATION RESULTS

The 12 bit DAC is powered by a 3.3V supply, resulting in a maximum output current of 40mA to the 50 ohm termination resistor. Thus a differential analog output voltage range of -1V to +1V is obtained. As shown in Fig.5 and Fig.6, the DNL and INL as seen from ELDO simulations of the 8 bit binary DAC are within ±0.22LSB and ±0.07LSB, respectively. The INL of the proposed DAC (4 thermometer and 8 binary bits) and that of the scheme normally implemented (8 thermometer and 4 binary bits) are less than ±0.6LSB and ±0.4LSB respectively. Similarly, the DNLs of the same are less than ±0.5LSB and ±0.1LSB which are shown in Fig.7. The Spurious Free Domain Range (SFDR) at 1MHz input signal for both the schemes are shown in Fig.8. yielding 78dB and 87dB respectively. Further, Fig 9 shows the variation of the SFDR across several frequencies of input signals, for the 4bit thermometer-8 bit binary; 8bit thermometer-4 bit binary architectures. The simulation results of both the schemes are listed in Table 2. The power consumed by the proposed DAC, as seen from ELDO-SPICE simulations is 15% lesser than the conventional one. The DAC, given its binary dominant segmentation also enjoys significant area advantages as it occupies an area of 0.0725mm^2 as compared to an area of 0.105mm^2 occupied by the conventional architecture.



(a)



(b)

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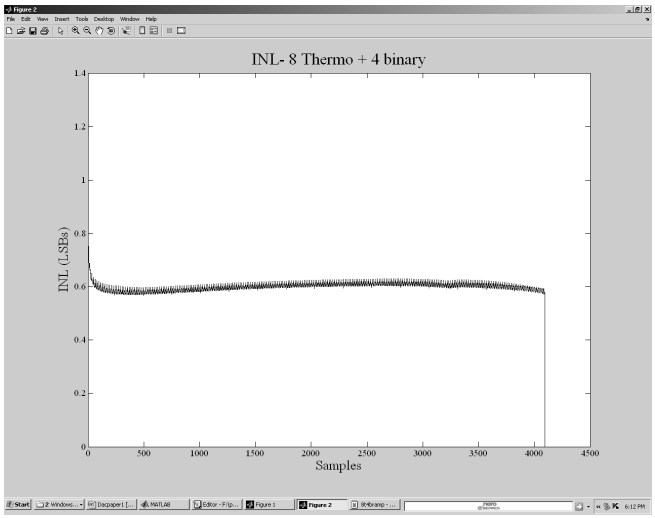
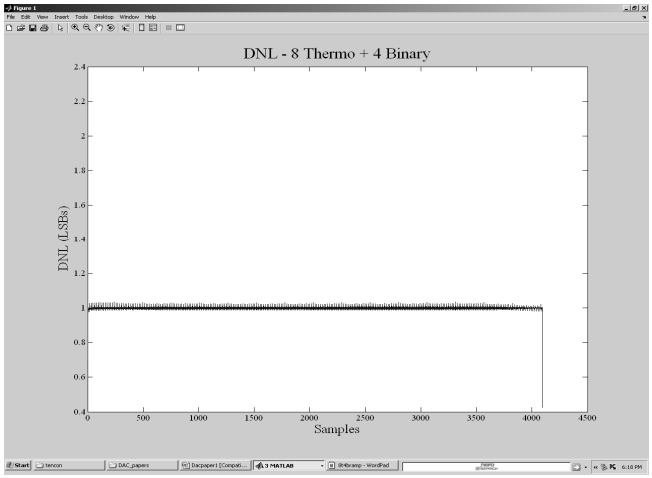
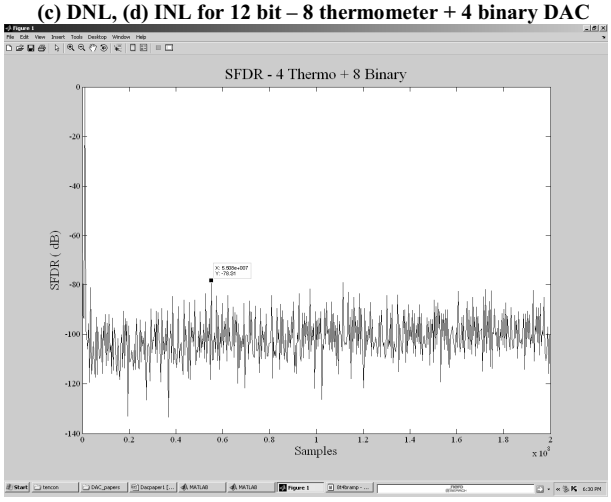


(C)

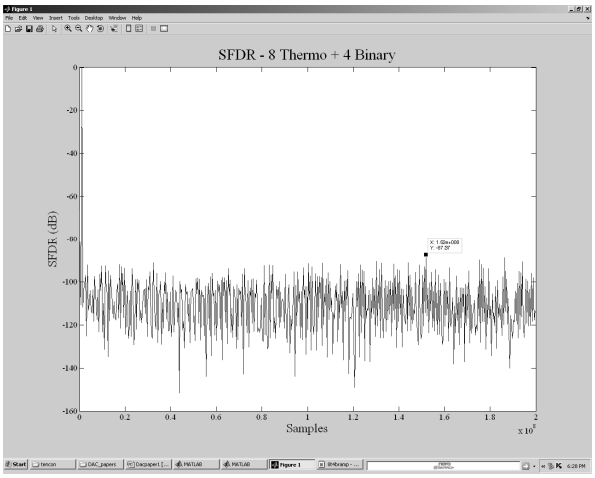


(d)

Fig. 7. (a) DNL, (b) INL for 12 bit – 4 thermometer + 8 binary DAC, (c) DNL, (d) INL for 12 bit – 8 thermometer + 4 binary DAC



(a)



(b)

Fig. 8. (a) SFDR @ 1MHz 12 bit – 4 thermometer + 8 binary DAC, (b) SFDR @ 1MHz 12 bit – 8 thermometer + 4 binary DAC

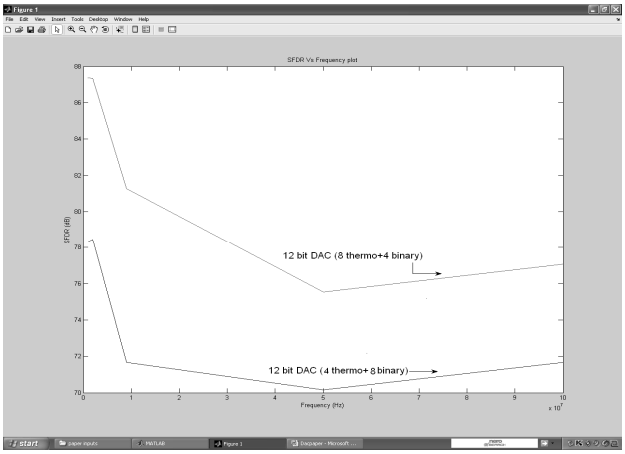


Fig. 9. SFDR Vs Frequency

TABLE 2. Simulation Results of the 12 bit DAC

Features/ Architecture	8 Thermo + 4 Binary	4 Thermo + 8 Binary
Resolution	12bit	12bit
Update Rate	400 MSPS	400 MSPS
DNL (LSBs)	0.036	0.65
INL (LSBs)	0.63	0.7
SFDR (dB)	87.37	78.31
Current source area (mm^2)	0.082	0.070
Digital area (mm^2)	0.023	0.0025
Power (mW)	120mW	102mW
Voltage	3.3 V	3.3 V
Process	350 nm	350 nm

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VI. CONCLUSION

In this paper, a 3.3V 12 bit NMOS Current Steering DAC implemented on a AMI 350nm CMOS technology has been discussed. The integration explores a 4 bit thermometer- 8 bit binary segmentation, as compared to the conventionally followed segmentation rules suggested by [6]. The static performance of the binary section has been significantly improved by achieving synchronization in current switching through the custom design of latches. This scheme opens the possibility of using more number of binary bits in the segmented DAC and hence occupies a silicon area of $0.0725mm^2$ which is 30% less than the conventional segmentation used in literature. Thus, this DAC, through a marginal sacrifice in static performance, however makes significant improvements in the silicon area occupied and the amount of power dissipated.

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