Voltage Regulator Module Design Considerations to Enhance Efficiency

Harish Padiyar U, Sumam David S.

Dept. of Electronics and Communication Engineering,
National Institute of Technology Karnataka, Surathkal,
Mangalore, India

hpadiyar@ieee.org, sumam@ieee.org

Mahant Shetti S.S

Chairman,
Karnataka Microelectronic Design Centre,
Manipal, India

mahant@karmic.co.in

Abstract— **The shrinking chip fabrication technologies reduces the power consumption and enhances the clock speeds of processors. Accordingly the new generation processors are expected to work below *1V* voltage profiles. The power supply designers are expected to deliver acceptable solutions with constraints like low voltage at large current, ripples below 2%, good transient response with high load slew rates etc. Few more constraints like small foot print, low cost and higher efficiency to meet the green energy initiatives, leaves very few options for designers. Keeping in view the decreasing voltage requirements of future processors, this paper proposes a loss minimization approach. This paper suggests a technique to select optimum switching frequency to maximize the power supply efficiency under all its operating conditions. The paper uses the steady state analysis of the converter to show the suitability of the solution as a cost effective approach.**

Keywords - Converter loss model, optimum switching frequency, synchronous buck converter, voltage regulator module

I. INTRODUCTION

The silicon process technologies have set a growth trend line for processors indicating a voltage profile of *1.0V* or low for their operation. With the clock speeds increasing, the power supply observes the processor as a low voltage, large current load with a very high slew rate. This power supply is popularly known as a voltage regulator module (VRM) though it belongs to switched mode power supply family. The VRM needs to meet the slew rate of about 4 - 5 A/ns for server class processors as compared to the present 450 A/μs [1], seen at the sensing point of the processor socket. The permissible output voltage deviation needs to be less than 2% for such load change. The high performance boards have entered the market with multi-core processor architectures. Every processor core uses a dedicated VRM in its proximity. Hence the scope for energy saving is tremendous within the motherboard and hence the industry is looking for a solution that satisfies these constraints at low cost.

In mobile platforms the VRM is powered from a power selector, which is either a battery pack or a power adaptor. The voltage range of Lithium battery cell is 4.2 - 2.9V and a pack of three or four cells stacked, the battery voltage is expected to be 16.8~8.7V. The power adaptor provides 19V to charge the battery and hence the VRM must be designed to work with a source voltage, ranging over 8.7-19V [2].

On the other hand, the compilers are exploring energy saving options by monitoring processor activity. The processor outputs a voltage identification code (VID), a digital code to indicate the state of processor and its voltage requirements [3-4]. These codes are used to set the reference voltage for the VRM control circuit.

The literature shows multi-phase interleaved converter as the most preferred topology due to their modularity and the best efficiency while supplying large currents of the order of hundreds of Amperes [5-6]. This topology employs multiple modules where each is a synchronous buck converter. The modules are identical in design and specifications except for they are switched in time phase. For any efficiency improvement solution to be adopted by industry, it needs to be implementable for existing modules. In this direction, many topology and control level solutions are proposed by different researchers. Autotransformer version of buck converters [7-8], self driven soft-switching techniques [9-10], two-stage architecture [2], [11-12], single-stage multiphase versions [13] etc, all are derived from basic synchronous buck converter topology [14-16]. These solutions look attractive but are with a definite premium of extra cost or complex control. This paper develops a loss model based analysis of a synchronous buck converter to propose a switching frequency selection criterion to ensure best efficiency for all operating points of the VRM for the future processor. This solution is cost effective as it does not need any expensive hardware. Moreover, this is a system level solution to VRM as it can be applied to the existing interleaved topology.

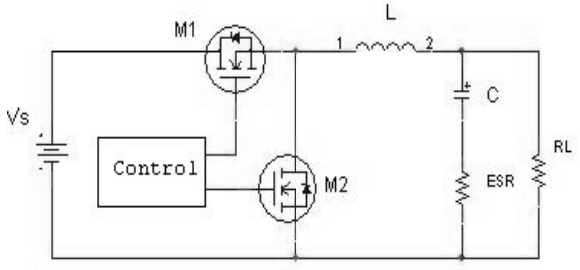

Fig.1 Synchronous rectifier buck converter

II. CONVERTER LOSS MODEL

To study the loss minimization in VRM, a synchronous buck converter as shown in Fig. 1 is used. A good switch selection

criterion would be the control MOSFET M_1 to switch faster to allow transfer of energy from input to output and the rectifier MOSFET M_2 to have a very low channel resistance (R_{DS}) as it works for longer duration. Hence, M_1 needs to be selected with lower Figure of Merit (FoM) to achieve higher efficiency [17]. FoM = $R_{DS}.Q_G$; where Q_G is the MOSFET gate charge. It is a practice to operate the converter in continuous current mode (CCM) to achieve good transient response. The load current continuity is generally decided by the input, output voltages and the magnitude of load current. Whereas the inductor value is very critical in meeting the slew rate requirement and hence all these form a part of the design specification. This would be a tough constraint for the designer to achieve good efficiency with acceptable transient response [18-19]. An optimal switching of converter [20] is reported in literature, which appears to be an assuring technique to improve VRM efficiency.

This work analyzes the converter losses under light load condition from energy efficiency perspective. It has identified the circulating energy flow at light loads compared to increasing load dependent losses at full load as a source of energy inefficiency. This approach is definitely a low cost solution, to achieve loss minimization at no additional expensive hardware requirement. To implement this approach, a loss model for the converter needs to be developed, analyzed to understand and explore the dependency of efficiency on switching frequency.

The converter loss model must include all the power dissipating components in the circuit, which are typically M_1 and M_2 on-state loss, driver loss, switching losses of both the devices, equivalent series resistance (ESR) loss of inductor and filter capacitor etc. The ripple current losses are predominant as it depends on switching frequency along with other circuit parameters [21-22]. The various components of switch power loss P_{LOSS_M} can be expressed as

$$P_{LOSS_M} = I_{RMS}^2 R_{DS} + \frac{I_O Q_{SW} V_S f_S}{I_G} + Q_G V_G f_S + \frac{Q_{OSS} V_S f_S}{2} \quad (1)$$

The (1) represent the power dissipation in a switch while working with a load current of I_O. It represents the channel resistance loss in R_{DS} due to the RMS value of the switch current I_{RMS}. The gate drive loss while pulse V_G supplying gate charge Q_G, output capacitor charge Q_{OSS} loss and switching charge Q_{SW} losses at source voltage V_S are also represented. I_G is the peak value of driver current while switching the device.

Similarly, the power loss in the inductor P_{LOSS_L} can be expressed as

$$P_{LOSS_L} = I_{RMSL}^2 R_L \quad (2)$$

where I_{RMSL} represents the RMS value of the current through inductor with an ESR of R_L. Similarly the power loss P_{LOSS_C} in the ESR R_C of the filter capacitor can be expressed as

$$P_{LOSS_C} = \frac{(\Delta I)^2}{12} R_C \quad (3)$$

where, ΔI is the peak to peak ripple current and

$$\Delta I = \frac{(V_S - V_O)D}{Lf_S} \quad (4)$$

The total loss P_{LOSS} can now be expressed as

$$P_{LOSS} = I_{RMS1}^2 R_{DS1} + \frac{I_O Q_{SW} V_S f_S}{I_G} + Q_{G1} V_{G1} f_S + \frac{Q_{OSS1} V_S f_S}{2} + I_{RMS2}^2 R_{DS2} + Q_{G2} V_{G2} f_S + \frac{Q_{OSS2} V_S f_S}{2} + I_{RMSL}^2 R_L + \frac{(\Delta I)^2}{12} R_C + \frac{Q_{RR2} V_S f_S}{2} \quad (5)$$

The subscripts *1* and *2* in (5) indicate the components that belong to M_1 and M_2 respectively. Due to the low stray inductance, the body diode of M_2 takes over the switch current; the moment gate pulse is removed. This reduces the switching losses in M_2 significantly when compared to that of M_1. The last term in (5) represent the reverse recovery charge Q_{RR} loss in body diode of switch M_2. Hence switching losses in M_1 are only considered. The (6) and (7) shows suitable representations for I_{RMSL} to find the RMS currents of M_1 and M_2, as

$$I_{RMSL}^2 = I_O^2 + \frac{(\Delta I)^2}{12} \quad (6)$$

$$I_{RMS1} = DI_{RMSL} \quad and \quad I_{RMS2} = (1-D) I_{RMSL} \quad (7)$$

III. METHODOLOGY

A circuit is designed with switches M_1, M_2 and filter passive components that meet the circuit efficiency and transient response. It appears from (5) that, the switching frequency is the only parameter that can be varied within a narrow range to explore any loss minimization. To appreciate the need for varying the switching frequency, a 90nm Intel® Pentium®4 processor with the following power specifications: Voltage requirement of 0.8V (sleep mode) to 1.6V (active mode), current requirement of 5A under no load to 91A under active loading was used in the simulation study. A VRM having interleaved topology with 12V nominal source voltage, load current of 10A to 30A per phase and 0.8V to 1.6V load voltage for each of the modules was used. Infineon BSC032NOS, MOSFETs are used for both control and freewheeling purpose. Coiltronics chip inductors were also used. The filter capacitance of 12.96mF is used to keep voltage ripple less than ±20mV for the lowest switching frequency. PSPICE circuit simulation environment of ORCAD® Capture 16.0 Version is used to simulate the circuit.

To satisfy the recommended selection criteria for switches, identical MOSFETs M_1 and M_2 were used. Table I shows the parameters of the MOSFET and the passive components used.

The losses in switches M_1, M_2, inductor ESR and filter capacitor ESR are then estimated and plotted in Fig. 2 – Fig. 5. Fig. 6 shows the variation in total converter losses as a function of switching frequency.

The converter loss depends on two criteria: one on switching frequency and the other on absolute load current magnitude. Further, the current ripples and the device switching process depend on switching frequency. The observations from Fig. 2 – Fig. 6 help, design and develop control strategies to meet the requirements of low output voltage VRM for future processors.

The MOSFET M_1 and M_2 have both conduction and switching frequency losses of which conduction losses are

dependent on the RMS value of current. As current ripples are reducing the conduction losses will decrease compared to the increase in switching losses with the increase in frequency. The optimal condition is reached at a frequency, beyond which the losses increase with switching frequency. The capacitor and inductor ESR losses are primarily due to current ripples and reduce with increasing switching frequency. Therefore the total converter losses are increasing with increasing frequency as the total losses are more sensitive to the switches than the passive elements.

Fig. 6 also indicates a possibility of loss minimization process by adopting an optimal switching frequency while working with different operating points. Fig. 7 shows the contribution of each of the circuit elements to power loss of the converter under different operating conditions.

TABLE I. VRM CIRCUIT COMPONENTS USED

Sl.No.	Parameter	Value
MOSFET		
1	Total Gate Charge Q_G	30nC
2	Switching Charge Q_{SW}	12nC
3	Output Charge Q_{OSS}	32nC
4	Reverse Recovery charge	15nC
5	Channel Resistance R_{DS}	2.7mΩ
6	Gate Pulse strength V_G	10V
7	Gate Driver current Capability I_G	2A
Inductor		
8	Inductance	0.5µH
9	ESR of Inductor	1.0mΩ
Filter Capacitor		
10	Capacitance	12.96mF
11	ESR of Capacitor	1.8mΩ

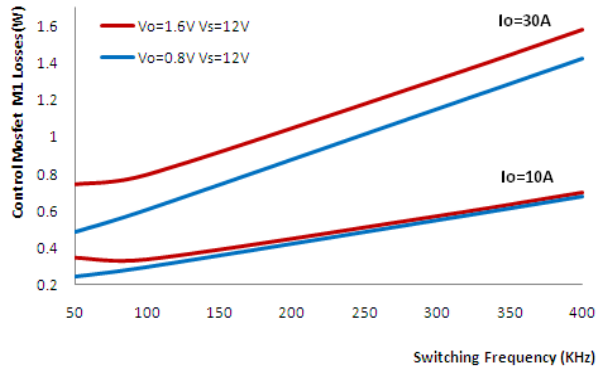

Fig. 2 Effect of switching frequency on Control MOSFET Losses

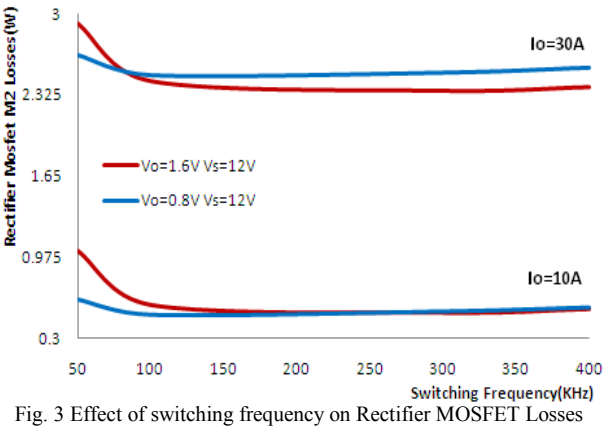

Fig. 3 Effect of switching frequency on Rectifier MOSFET Losses

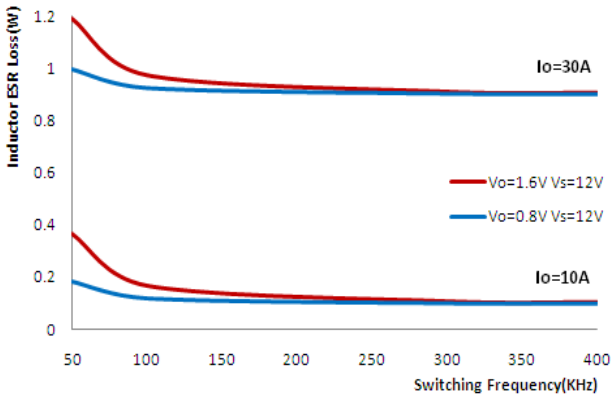

Fig. 4 Effect of switching frequency on Inductor ESR Losses

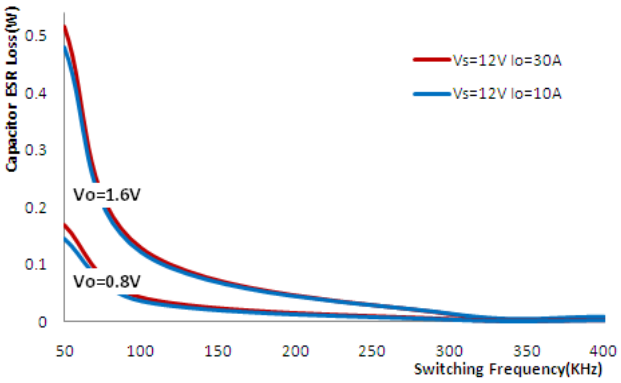

Fig. 5 Effect of switching frequency on filter Capacitor ESR Losses

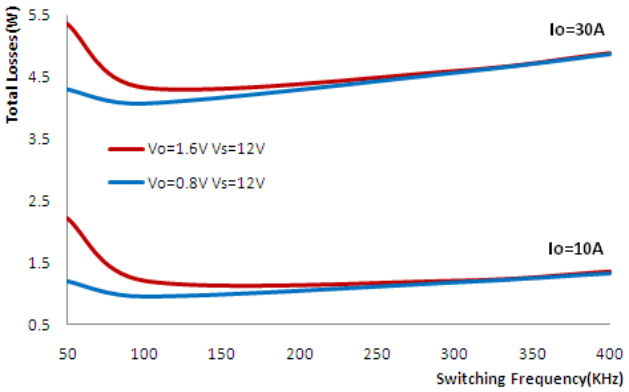

Fig. 6 Effect of switching frequency on VRM total Losses

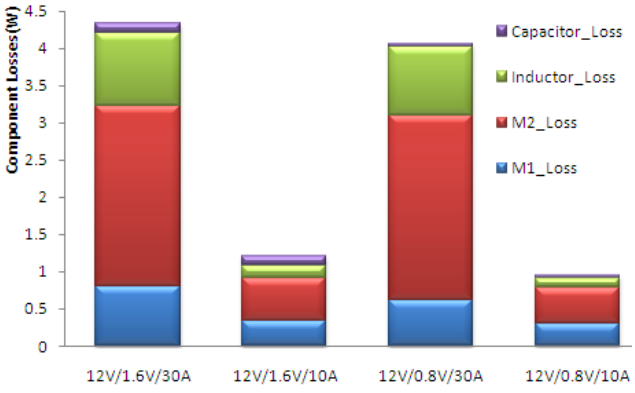

Fig. 7 Contribution of each circuit element to the total loss under various operating conditions

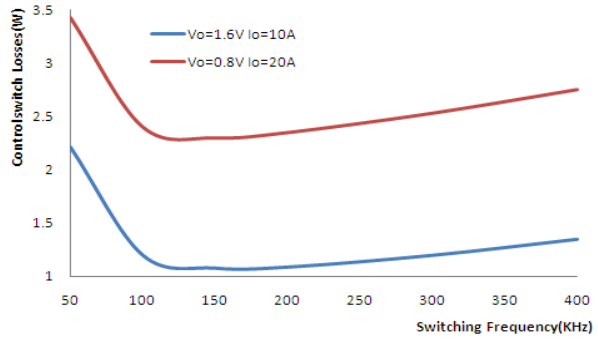

Fig. 8 Effect of switching frequency on Control Switch Loss for Po=16W

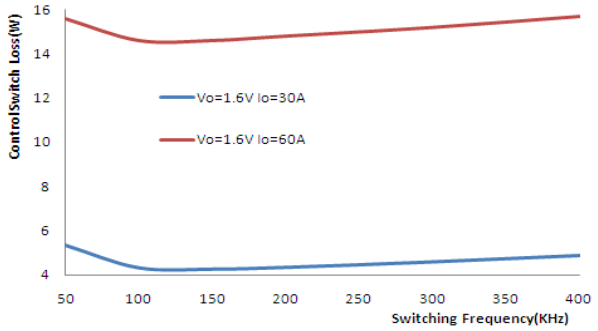

Fig. 9 Effect of switching frequency on Control Switch Loss for Po=48W

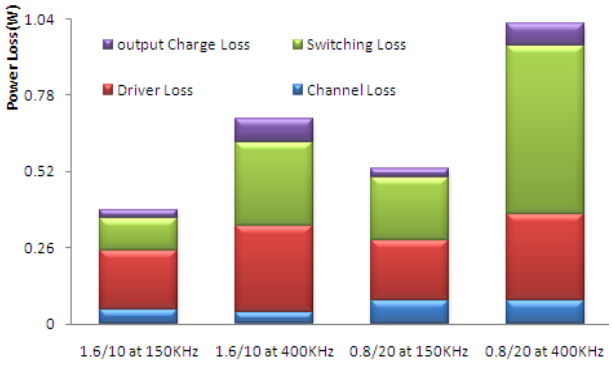

Fig. 10 Control switch Loss Components for different operating points

The Fig. 2- Fig. 6, Fig. 8 and Fig. 9 of the case studied, show the optimum switching frequency in the range of 100-200 kHz for the parameters selected. However, the specific optimal switching frequency for a given circuit can be obtained by analysing its typical and extreme working conditions. Also the VRM voltage conversion ratio being smaller, the M1 conduction losses are much smaller than that of M2. Fig. 8 and Fig. 9 shows the M1 losses as a function of frequency for a given power output with reduced output voltage. This indicates the dominance of frequency on its losses. Fig. 10 shows the influence of switching frequency on different components of M1 loss for different operating points. The set of first two column and second two column bars in Fig. 10 indicate the increase in switching frequency dependent loss for a given operating point. The first and the third column bar indicate the effect of frequency on power loss while output voltage lowered. Hence at lower output voltage, the channel loss gets shifted from M_1 to M_2 for a given load current. In other words, the frequency dependent losses then dominate over the reducing channel losses for M_1. Hence, while reducing the output voltage in VRMs we need to look for lower frequency operation to prevent converter becoming inefficient.

Also, it is essential to use multiple switches in parallel for M_2 to reduce the dominant channel losses compared to frequency dependent losses. Hence, for future processors with voltage profile below *1.0V*, it is a better strategy to balance out the conduction and frequency dependent losses to achieve higher efficiency. Thus, it is a low cost strategy to enhance the VRM efficiency. The MOSFET manufacturers are confident on their move to produce lower R_{DS} MOSFETs for reducing rectifier switch loss, and lower FoM MOSFETs for Control switch applications. This indicates the growing dominance of frequency dependent losses, as compared to diminishing channel losses.

IV. Conclusion

The green energy initiatives are looking for VRM designs to meet high efficiency profiles to power the processors below 1V. It is predicted that the load current magnitude and slew rate are expected to rise to extremely large values. The product designers of power supply or VRM in specific are looking for a system level solution that could retrofit the existing practices. In this context, this paper develops and analyses the converter loss model to draw the following conclusions.

- Efficient module design helps enhancing efficiency of interleaved converter.
- Loss model analysis shows switching frequency variation technique is effective as it has no additional hardware cost.
- The low output voltage reduces control switch ON time which forces the rectifier switch to dissipate more power for a given power.
- Use multiple rectifier switches in parallel to reduce the dominating conduction losses.
- The switching frequency has a strong influence on control switch losses and hence the only feasible option available is to lower the frequency.
- It is necessary to use more modules in parallel in time phase with lower loading per module to restrict the filter capacitor size.
- The rise time and steady state error depend on the passive element values and not on the switching frequency. The control bandwidth can be selected in relation to preferred switching frequency to meet the transient response [23-24].

The switch parameters given in Table I, though are converter operating point specific, vary only over a very narrow range. Hence the propositions and conclusions drawn are valid as can be seen from simulation results given in Fig. 11 and Fig.12. This shows that using lower switching frequency for lower output voltage yields better efficiency. The proposed concept of lowering the switching frequency suggests

using multiple rectifier switches and lower load per module in interleaved converter to help design efficient power supply for future processors.

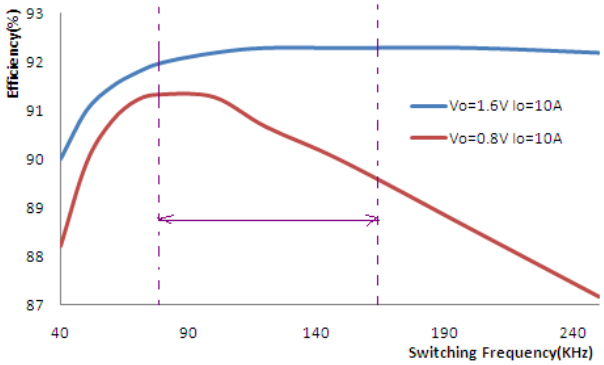

Fig. 11 Effect of switching frequency on Converter Efficiency

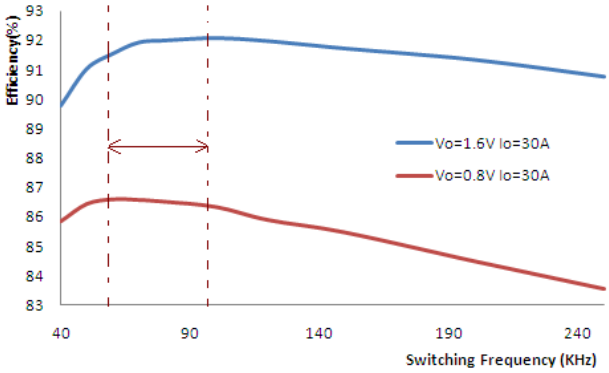

Fig. 12 Effect of switching frequency on Converter Efficiency

REFERENCES

[1] M. Zhang, M. Jovanovich and F. C. Lee, "Design Considerations for Low-Voltage On-board DC/DC Modules for Next Generations of Data Processing Circuits", IEEE Trans. on Power Electronics, pp.328-337, March 1996.

[2] Jia Wei and F. C. Lee, "Two stage voltage regulator for Laptop computer CPUs and the corresponding advanced control schemes to improve light load performance", IEEE APEC 2004, vol.2, pp. 1294-1300.

[3] Intel Corporation, Intel Pentium-4 Processor on 90nm process data sheet, February 2005.

[4] Intel Corporation, Voltage regulator down (VRD) - 10.1 design guidelines for desk top applications, April 2005.

[5] Xunwei Zhou, "Low-voltage High-efficiency Fast-transient Voltage Regulator Module", Ph. D dissertation, Virginia Polytechnic Institute and State University, 1999.

[6] X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen, H. Wu, L. Amoroso, F. C. Lee, and D. Chen, "Investigation of Candidate VRM Topologies for Future Microprocessors", IEEE Trans. on Power Electronics, vol.15, pp. 1172-1182, November 2000.

[7] Kaiwei Yao, Lee F.C., Yu Meng and Jia Wei, "Tapped-inductor buck converters with a lossless clamp circuit", IEEE APEC 2002, vol. 2, pp 693-698.

[8] Kaiwei Yao, Yu Meng, and Fred C. Lee, "A Novel Winding-coupled buck converter for High-Frequency, High Step-Down dc/dc Conversion", IEEE PESC 2002, vol. 2, pp. 651-656.

[9] J. Zhou, M. Xu, Julu Sunand and F. C. Lee, "A self driven soft switching voltage regulator for future microprocessors", IEEE Trans. on Power Electronics, vol.20, no.4, pp. 806-814, July 2005.

[10] Jia Wei and F. C. Lee, "Two novel soft switched, high frequency, high efficiency, non isolated voltage regulators-The phase shift buck converter and the matrix- transformer phase – buck converter", IEEE Trans. on Power Electronics, vol. 20, no.2, pp. 292-299, March 2005.

[11] Y. Ren, M. Xu, K. Yao, Y. Meng and F. C. Lee, "Two stage approach for 12 V VR", IEEE Trans. on Power Electronics, vol.19, no. 6, pp. 1498-1505, November 2004.

[12] Ming Xu, Julu Sun, and F. C. Lee, "Voltage divider and its application in the two stage power architecture", IEEE APEC 2006, pp. 499-505.

[13] Y. Jang, M. M. Jovanovic and Yuri Panov, "Multi–Phase buck converters with extended duty cycle", IEEE APEC 2006, pp. 38-44.

[14] X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen, H. Wu, L. Amoroso, F. C. Lee, and D. Chen, "Investigation of Candidate VRM Topologies for Future Microprocessors", IEEE APEC 1998, pp. 145-150.

[15] R. Erickson and D. Maksimovic, "High Efficiency DC-DC Converters for Battery-Operated Systems with Energy Management", Worldwide Wireless Communications, Annual Reviews on Telecommunications, June 1995

[16] R. Erickson and D. Maksimovic, "DC-DC Converter design for Battery-Operated Systems", IEEE PESC 1995, pp. 103-109.

[17] G. Belverde, C. Guastella, M. Mellito, S. Musumeci, R. Pagano and A. Reciti, "Advanced Characterization of Low-Voltage Power MOSFET in Synchronous Rectifier Buck Converter Applications", IEEE IAS Annual Meeting 2003, pp.1802-1809.

[18] Daniel W. Hart, Introduction to Power Electronics, PHI, 1997.

[19] R. Erickson and D. Maksimovic, Fundamentals of Power Electronics, Springer International Edition, 2001.

[20] Harish Padiyar U., Sumam David S., and S. Mahant Shetti, "A System Level Solution to Improve VRM Efficiency", IEEE IES ICIT 2009, pp.1-5.

[21] Infineon Technologies, Improving Efficiency of Synchronous Rectification by Analysis of the MOSFET Power Loss Mechanism, Application Note, Rev. 2. 0, 2009.

[22] Alpha & Omega Semiconductors Inc, "Quasi-clamped Inductive Switching Behavior of Power Mosfets", IEEE. PESC 2008.

[23] Pit-Leong Wong, Fred C. Lee, Xunwei Zhou and Jiabin Chen, "VRM Transient Study and Output Filter Design for Future Processors", Proceedings of VPEC seminar, 1997.

[24] Kaiwei Yao, Y. Ren and F. C. Lee, "Critical Bandwidth for the load transient response of voltage regulator modules", IEEE Trans. on Power Electronics, vol. 19, no.6, pp. 1454-1461, November 2004.