91dB Dynamic Range 9.5 nW Low Pass Filter for Bio-Medical Applications

Jayaram Reddy M. K, Sreenivasulu Polineni and Tonse Laxminidhi
Department of Electronics and Communication Engineering
National Institute of Technology Karnataka, Surathkal
Mangalore-575025, Karnataka, India
Email: jayaram.041@gmail.com laxminidhi_t@yahoo.com

***Abstract*—This paper presents a second order, fully differential, low pass filter. The filter has a tunable bandwidth in the range 4 Hz to 100 Hz and offers a dynamic range of 91 dB. The filter is based on the source-follower biquad operating in the sub-threshold region. The main idea is to exploit the strengths of sub-threshold source follower circuit, like low noise, low output impedance, high linearity and low power. The filter design has been validated in UMC 0.18 μm CMOS process. The filter consumes only 9.5 nW of power at 1.8 V supply, making it suitable for bio-medical applications. In terms of noise and dynamic range the reported filter is better than previous works found from the literature.**

***Index Terms*— Analog filter, low frequency, bio-medical, source follower, high dynamic range.**

I. Introduction

In bio-medical electronics there is a huge demand for portable low power battery operated devices. This necessitates the circuits used in the portable devices to be compact and consume low power. A feasible solution for designing low power circuits is to operate the MOS devices in sub-threshold region.

For pre-processing the bio-medical signals (typically amplitude ranging from 1μV to 10 mV and frequency ranging from 10 mHz to 10 kHz [1]), we require a pre-amplifier to amplify the weak bio-signals and low pass filter to remove the unwanted noise. Low pass filter (LPF) is the crucial part in the bio-medical device as the precision of the entire device depends on it. For ECG, EEG, pacemakers and other applications, filters with cut-off frequency ranging from 1 Hz to 100 Hz is required. The design of low frequency filter with low noise, high linearity, high dynamic range and low circuit area is quite challenging.

The design of fully integrated low frequency, low pass filter requires large time constant. To achieve large time constants several circuit topologies have been reported in the literature. Using active-RC circuits to achieve large time constant give high linearity but at the cost of area, as the values of resistors and capacitors needed are high. Switched capacitor circuits [2], [3] are not preferred due to the leakage issues in advanced CMOS technology. The most popularly used topology to achieve large time constant is transconductor-capacitor (g_m-C) filter topology. To achieve large time constant (C/g_m) in g_m-C filter with permissible on-chip capacitance several g_m reduction techniques have been reported in the literature [4], [5] and are: current division, source degeneration, multiple input floating gate (MIFG) and bulk-driven. Relative performance and limitations of these methods are summarized in the Table I.

In this paper, filter based on the source follower is presented as an alternative to g_m-C filter topology. The paper is organized as follows. Section II illustrates the source follower biquad and low pass filter architecture based on the source follower biquad. Simulation results are reported in the Section III. Finally, Section IV concludes the paper.

TABLE I
g_m REDUCTION TECHNIQUES FOUND IN LITERATURE AND THEIR LIMITATIONS.

Technique	Effective G_m	Limitations
Current Division	$\frac{g_m}{1+M}$ (M: Ratio of transistor sizes used for current division)	• Current ratio accuracy • Circuit area • Output dynamic range
Multiple Input Floating Gate	$\left(\frac{C_1}{C_1+C_2}\right) g_m$	• Large capacitor ratio • Circuit area • Input referred noise • Limited tunability
Source Degeneration	$\frac{g_m}{1+g_m R}$	• Large area for R • Thermal noise of R
Bulk Driven	$\left(\frac{\gamma_o}{2\sqrt{2\Psi_{FB}+V_{SB}}}\right) g_m$	• Finite input impedance • Process dependent

II. Subthreshold Source Follower Low Pass Filter

A. Source follower Biquad

The conventional source follower with capacitive load is shown in the Fig. 1a. This circuit can be considered as a first order low pass filter. M_1 is the input transistor, M_2 is a current source and C_L is the load capacitance.

The transfer function for source follower is given by

$$H(s) = \frac{g_m r_o}{sCr_o + g_{mb} r_o + g_m r_o + 1} \quad (1)$$

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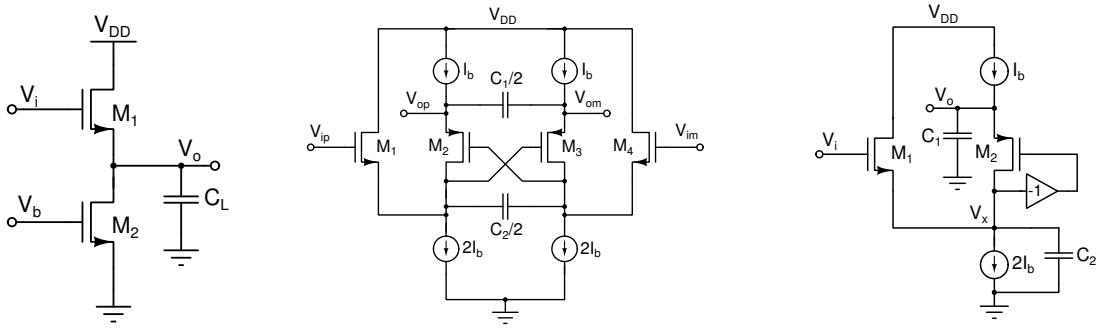

(a) (b) (c)

Fig. 1. (a) Source follower (b) Source follower based biquad (c) Single-ended circuit of the source follower biquad.

Where g_m and g_{mb} are the gate transconductance and bulk transconductance of the transistor M_1 respectively, r_o is the equivalent output resistance ($r_o = r_{o1}||r_{o2}$).

The circuit in Fig. 1a can be extended to realize a fully differential biquad as shown in the Fig. 1b. Here, the complex conjugate poles required for the second order response are generated using a positive feedback. It is comprised of four MOSFETs ($M_1 - M_4$), four current sources ($I_b, 2I_b$) and two capacitors (C_1 and C_2). Source follower biquad architectures are reported in [6]. However, the architecture in Fig. 1b has not been explored for its use for low-power, low-frequency applications. The inherent features of this biquad are: biquad does not require an additional common-mode feedback circuit as the common-mode voltage is self-biased by the NMOS and PMOS transistors V_{GS} and there is no instability issue as the loop gain of the positive feedback is inherently less than one. Furthermore, the filter is free of parasitic poles since there are only two nodes in the circuit and they are the integrating nodes. Also, it offers a good linearity since the the signal is directly processed in terms of voltage using local feedback.

A single-ended circuit of the biquad is shown in Fig. 1c and is used to simplify the analysis. The small signal equivalent of Fig. 1c is shown in the Fig. 2. The overall transfer function is given by (2), where $g_{mn1} = g_{m1} + g_{mb1}$ and $g_{mp2} = g_{m2} + g_{mb2}$.

The filter has a less than unity DC gain and it can be written as

$$A = \frac{g_m^2}{(g_m + g_{mb})^2} \tag{3}$$

Clearly, the DC gain is not unity and is equal to $1/(1+\eta)^2$, where $\eta = g_{mb}/g_m$ is the body-effect transconductance ratio (usually in the range $0.2 - 0.5$). Thus, the DC gain achievable is between -3.2 dB and -7.2 dB.

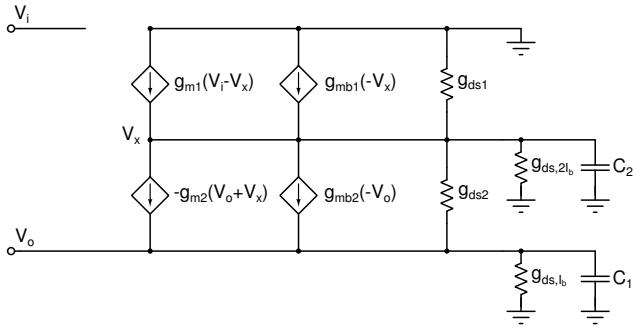

Fig. 2. Small signal equivalent circuit of Fig. 1c.

Neglecting channel length modulation and body effect, and assuming all transistors have same g_m and g_{mb}, the transfer function reduces to (4).

$$\frac{V_o}{V_i} = -\frac{1}{s^2\left(\frac{C_1C_2}{g_m^2}\right) + s\left(\frac{C_2}{g_m}\right) + 1} \tag{4}$$

The cut-off frequency (ω_o) and Quality factor (Q) are given by

$$\omega_o = \frac{g_m}{\sqrt{C_1C_2}} \tag{5}$$

$$Q = \sqrt{\left(\frac{C_1}{C_2}\right)} \tag{6}$$

To achieve low cut-off frequency, the value of g_m should be very small, since use of large on-chip capacitors are limited by silicon area constraints. Unlike prior works [6], where source followers are operated in saturation region, we operate

$$\frac{V_o}{V_i} = -\frac{g_{m1}(g_{m2} - g_{ds2})}{(g_{mn1} - g_{m2} + g_{ds1} + g_{ds2} + g_{ds,2I_b} + sC_2)(g_{mp2} + g_{ds2} + g_{ds,I_b} + sC_1) + (g_{mp2} + g_{ds2})(g_{m2} - g_{ds2})} \tag{2}$$

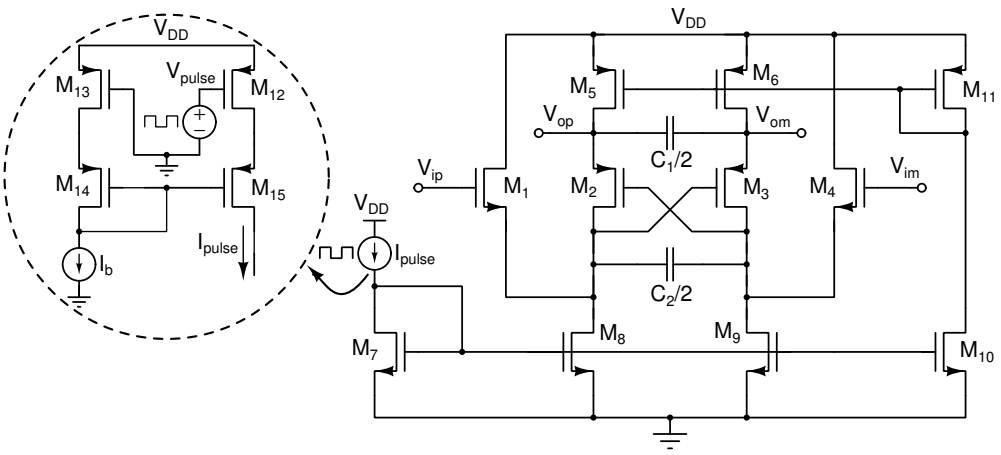

Fig. 3. Complete schematic of the source follower biquad based filter.

the transistors in sub-threshold region to minimize g_m. The expression for g_m in sub-threshold region is given by $g_m = I_D/nV_T$, where n is the sub-threshold slope factor (≈ 1.0), V_T is the thermal voltage ($\approx 26\,mV$) and I_D is the drain current. To achieve low g_m, the value of I_D used is low which results in low power consumption.

B. Low Pass filter architecture

The complete schematic of the proposed second order low pass filter is shown in Fig. 3.

To enhance the re-usability of the filter and to extract wide frequency bio-potential signals, the filter cut-off should be tunable. The filter is made tunable by switching the transistor currents with a desired duty-ratio. The frequency response scales proportionately with the duty-ratio. The scheme used to switch the currents is shown inside the dotted circle, and comprises of transistors ($M_{12}-M_{15}$), DC bias current (I_b) and voltage source (V_{pulse}).

C. Noise Analysis

Equivalent circuit of the filter for noise analysis is shown in Fig. 4. Both thermal noise and flicker noise are considered for the analysis.

The total input-referred noise (IRN) is given by

$$\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_{m1}}\left[1+\frac{g_{mn1}^2}{g_{m1}g_{m2}}\right] + \frac{K_F}{C_{ox}\cdot f}\left[\frac{1}{(WL)_1}+\frac{g_{mn1}^2}{(WL)_2\cdot g_{m1}^2}\right] \quad (7)$$

where k is the Boltzman constant, T is the Absolute temperature, γ is the noise co-efficient, K_F is the process dependent parameter, C_{ox} is the oxide capacitance, f is the frequency and W, L are width and length of the transistor. The effect of flicker noise is suppressed by choosing large transistors, as the flicker noise is inversely proportional to the transistor gate area. Thus the thermal noise is made the dominant contributor. The thermal noise integrated over the passband is given by

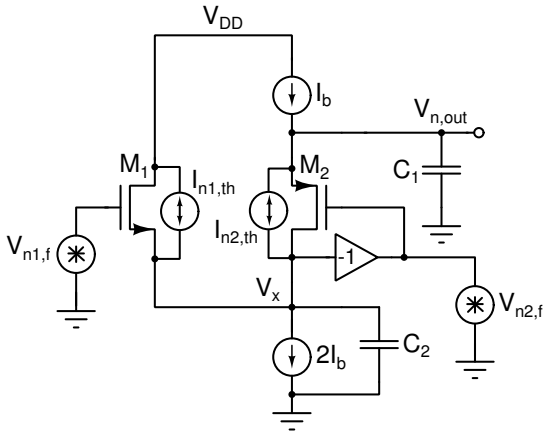

Fig. 4. Equivalent circuit for noise analysis.

$$\overline{V_{n,in,th,int}^2} = \frac{4kT\gamma}{\sqrt{C_1C_2}}\sqrt{\frac{g_{m2}}{g_{m1}}}\left[1+\frac{g_{mn1}^2}{g_{m1}g_{m2}}\right] \quad (8)$$

Asumming all transconductanes to be equal and neglecting body-effect, the expression for thermal noise is equal to

$$\overline{V_{n,in,th,int}^2} = \frac{8kT\gamma}{\sqrt{C_1C_2}} \quad (9)$$

III. Results and Discussions

The proposed Butterworth low pass filter is designed and simulated in UMC 0.18 μm CMOS technology. For the given transconductance of 20.8 nS (g_m = g_{m1} = g_{m2}) and bandwidth of 100 Hz, the value of integrating capacitors are found to be $C_1/2 = 12.4\,pF$ and $C_2/2 = 24.12\,pF$ including parasitics. The current I_b is set to 1 nA. The frequency response of the filter with the varying duty-ratio of current switching is shown in Fig. 5. The cut-off frequency is found to be adjustable in the range 4 Hz – 100 Hz for the duty-ratio of 1% to 100%. Fig. 6 shows the plot of filter cut-off frequency as a function

of switching duty-ratio. The DC gain of the filter is found to be -3.2 dB, as expected.

Table II summarizes the filter performance and compares it with the similar works found in literature. To examine the filter linearity, the switching duty-ratio is set to 100% with $I_b = 1nA$ ($f_c = 100\,Hz$ setting). The filter is excited with sinusoidal signal of amplitude 1.03 V_{pp} differential at 10 Hz. A total harmonic distortion (THD) of 1 % is obtained. With an in-band (0.1 Hz to 100 Hz) input-referred noise (IRN) of 10.24 μV_{rms}, the filter is found to offer a dynamic range (DR) of 91 dB. It is to be noted that the total power consumed by the filter is only 9.5 nW operating on 1.8 V supply. This high dynamic range is best among the similar filters found in the literature. The Equivalent output noise of the filter is shown in Fig. 7.

Monte-carlo simulations are performed to evaluate the performance of filter for device process variations and mismatch. The maximum deviation (3σ) of cut-off frequency is found to be less than 10% of the nominal value, without the use of any bandwidth fixing loop. The distribution of cut-off frequency is shown in the Fig. 8.

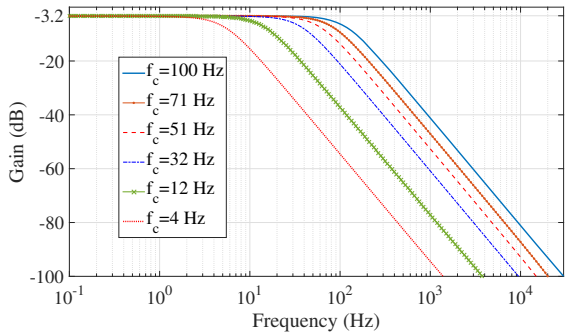

Fig. 5. Magnitude response of the filter for different duty cycles of current pulse. The cut-off varies between 100 Hz to 4 Hz. The settings used for these results are in the format [clock frequency, duty cycle, cut-off frequency (f_c)]: [10 kHz, 100%, 100 Hz], [10 kHz, 70%, 71 Hz], [5 kHz, 50%, 51 Hz], [5 kHz, 30%, 32 Hz], [1 kHz, 10%, 12 Hz], [1 kHz, 1%, 4 Hz].

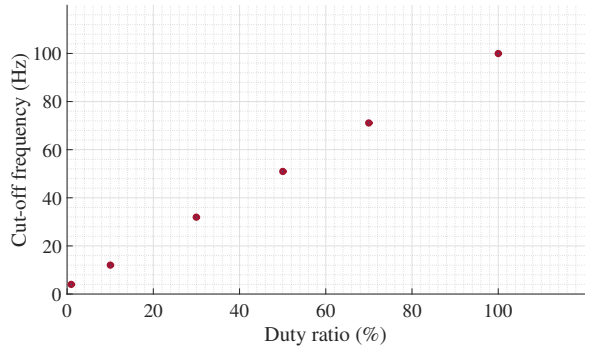

Fig. 6. Tuning graph showing the filter cut-offs for different duty cycle of current pulse.

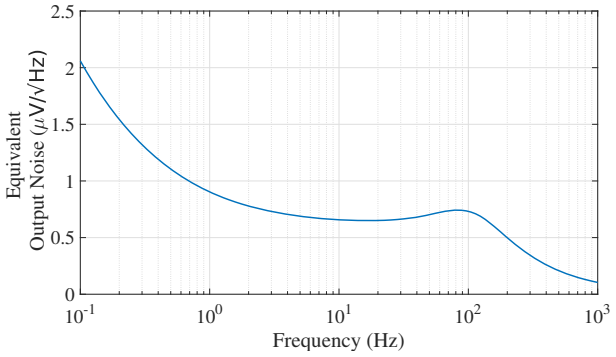

Fig. 7. Output-referred noise of the filter.

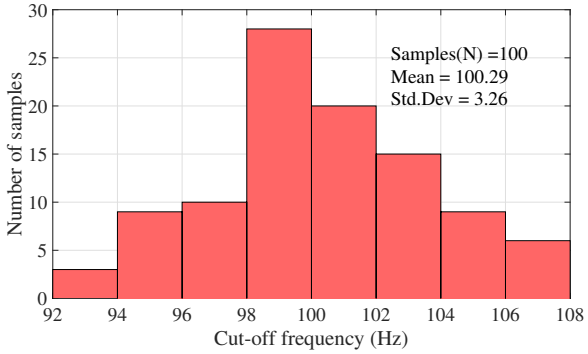

Fig. 8. Monte-carlo simulation of filter Cut-off for 100 runs.

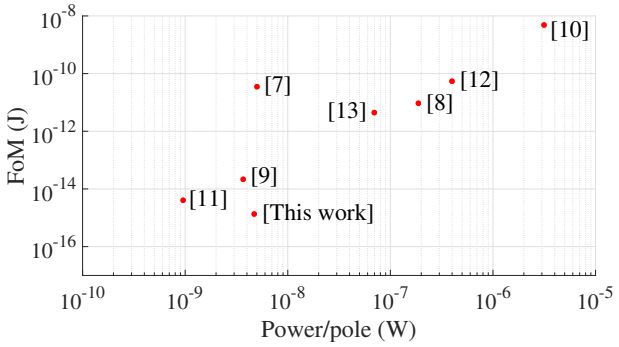

Fig. 9. FoM vs Power/pole.

To compare this work with the state-of-the-art low frequency filters, a Figure-of-Merit (FoM) [9], [14] is used and is defined by

$$FoM = \frac{P}{N \times f_c \times DR} \tag{10}$$

where P is the total power consumption, N is the filter order, f_c is the filter cut-off frequency and DR is the dynamic range.

TABLE II
COMPARISON OF THE CIRCUIT PERFORMANCE WITH RELATED WORKS.

Parameters	[7] † [2011]	[8] ⋆ [2012]	[9] † [2013]	[10] † [2014]	[11] ⋆ [2015]	[12] ⋆ [2016]	[13] † [2017]	This Work ⋆
V_{DD} (V)	1	3	3	3	1.5	0.9	1	1.8
Technology (μm)	0.35	0.35	0.35	0.35	0.35	0.13	0.18	0.18
Power (μW)	0.005	0.75	0.015	6.31	0.0019	0.8	0.35	0.0095
DC Gain (dB)	0	-6	0	–	0	4.1	-8	-3.2
Filter Order	1	4	4	2	2	2	5	2
Bandwidth (Hz)	2m	40	100	1.95	250	47.98	50	100
THD (dB)	-40	-59	-60.7	-40	-40	-40	-49.9	-40
IRN (μV_{rms})	32	500	29	791	89	17.38	97	10.24
DR (dB)	63.8	54	64.8	50.65	59.6	43.8	49.8	91

† Measured ⋆ Simulated

Lower FoM indicates better filter performance. From the filter simulation results, the FoM is found to be 1.16×10^{-15}J, which is better compared to the state-of-the-art filters. Fig. 9 compares the filters in the literature by plotting FoM as function of power per pole.

IV. CONCLUSION

High dynamic range, low noise, low power, tunable filter based on sub-threshold source follower is presented. The filter designed in UMC 0.18 μm CMOS process reports a bandwidth of 4 Hz – 100 Hz with 9.5 nW power consumption at 1.8 V supply. With the dynamic range of 91 dB, the filter is proved to be a better candidate for bio-medical applications. In addition, the filter is also found to be energy efficient.

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REFERENCES

[1] Reid R. Harrison. "A versatile integrated circuit for the acquisition of biopotentials." in *Proc. Custom Integrated Circuits Conf.*, San Jose, CA, USA, pp. 115–122, Sep. 2007.

[2] K. Nagaraj, "A parasitic-insensitive area-efficient approach to realizing very large time constants in switched-capacitor circuits." *IEEE Transactions on Circuits and Systems*, vol. 36, no. 9, pp. 1210–1216, Sep. 1989.

[3] Wing-Hung Ki and Gabor C. Temes. "Area-efficient gain-and offset-compensated very-large-time-constant SC biquads." in *Proc. 1992 IEEE International Symposium on Circuits and Systems (ISCAS)* vol. 3, pp. 1187-1190 , May. 1992.

[4] A. Veeravalli, E. Sanchez-Sinencio, and J. Silva-Martinez. "Transconductance amplifier structures with very small transconductances: A comparative design approach." *IEEE Journal of Solid-State Circuits*, vol. 37, no. 6, pp. 770–775, Jun 2002.

[5] L. Zhou and S. Chakrabartty. "Design of low-Gm transconductors using varactor-based degeneration and linearization technique." in *Proc. Biomedical Circuits and Systems Conference (BioCAS).*, Atlanta, CA, USA, pp. 1–4, Oct. 2015.

[6] Stefano D'Amico, Matteo Conta, and Andrea Baschirotto, "A 4.1-mW 10-MHz fourth-order source-follower-based continuous-time filter with 79-dB DR," *IEEE Journal of Solid-State Circuits*, vol.41, no. 12, pp. 2713-2719, 2006.

[7] E. Rodriguez-Villegas, A. J. Casson, and P. Corbishley, "A subhertz nanopower low-pass filter," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 58, no. 6, pp. 351–355, Jun. 2011.

[8] Liu Y.T, Donald Y.C. Lie, Weibo Hu, and Tam Nguyen. "An ultralow-power CMOS transconductor design with wide input linear range for biomedical applications." in *Proc. 2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2211–2214, May. 2012.

[9] T.-T. Zhang, P.-I. Mak, M.-I. Vai, P.-U. Mak, M.-K. Law, S.-H. Pun, F. Wan, and R.P. Martins, "15-nW biopotential LPFs in 0.35-μm CMOS using subthreshold-source-follower biquads with and without gain compensation, *IEEE Transactions on Biomedical Circuits and Systems,* vol. 7, no. 5, pp. 690702, Oct. 2013.

[10] G. Domnech-Asensi, Gins, Juan Manuel Carrillo-Calleja, Julio Illade-Quinteiro, Flix Martnez-Viviente, Jos ngel Daz-Madrid, Francisco Fernndez-Luque, Juan Zapata-Prez, Ramn Ruiz-Merino, and Miguel Angel Domnguez, "Low-frequency CMOS bandpass filter for PIR sensors in wireless sensor nodes." *IEEE Sensors Journal*, vol. 14, no. 11, pp. 4085–4094, Nov. 2014.

[11] Chutham Sawigun and Prajuab Pawarangkoon. "A compact subthreshold CMOS 2nd-order gm-C lowpass filter." in *12th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, pp. 1-4, Jun. 2015.

[12] Arya Richa, and Joo P. Oliveira. "Gm-C biquad filter for low signal sensor applications." in *Proc. 2016 MIXDES-23rd International Conference Mixed Design of Integrated Circuits and Systems,* pp. 207–210, 2016.

[13] Chuan-Yu Sun and Shuenn-Yuh Lee. "A Fifth-Order Butterworth OTA-C LPF with Multiple-Output Differential-Input OTA for ECG Applications." *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2017.

[14] E. Vittoz and Y. Tsividis, "Frequency-dynamic range-power," in *Trade-Offs in Analog Circuit Design*, pp. 283–313, Springer US, 2002.