A Novel Zero Blind Zone Phase Frequency Detector for Fast Acquisition in Phase Locked Loops

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***Abstract*—The inability to sense the transitions in the input by conventional phase frequency detector (PFD) during the reset operation leads to blind zone, which reduces the acquisition speed and the detection range. The pull down network in proposed design is modified so as to eliminate the reset pulse for phase difference beyond the dead zone in order to have a full detection range and less cycle slippage. As the design gives the right polarity for phase differences close to $\pm 2\pi$, the acquisition time is reduced substantially. The Transfer characteristic of the PFD manifests an identical response. The PFD design is implemented in 180nm CMOS technology and consumes 1.36mW at an operating frequency of 1GHz.**

I. Introduction

Charge Pump Phase Locked Loops are widely used in high speed frequency transceivers - clock and data recovery, frequency synthesizers and high speed clock generators of microprocessors. The PFD serves as an essential integral block as it carries out the phase and frequency comparison, thereby generating suitable control signals for the loop to acquire and maintain its lock. The sensitivity of the PFD along with the nature of the control signals play an essential role in the performance of the overall PLL system. The development in high speed communication applications have motivated the need for fast acquisition PLLs with very low steady state phase error.

Phase Frequency Detector is a simple tri-state machine consisting of basic memory elements, the state diagram of which is shown in Fig 1. Extensive research has been carried out to increase the effective input range and linearity of PFD operation. The simplest and conventional phase frequency detector is shown in Fig 2, has been presented in [1]. Further, many architectures have been developed which include pre-charge type PFD [2], ncPFD [3], latch based PFD [4]- [7], and a couple of designs with non-linear transfer characteristics [8] [9].

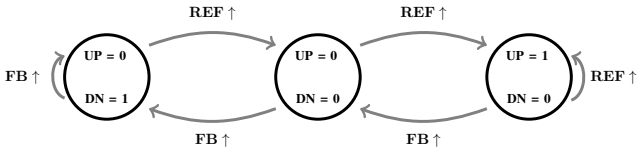

Fig. 1. Tri-state FSM Logic for PFD

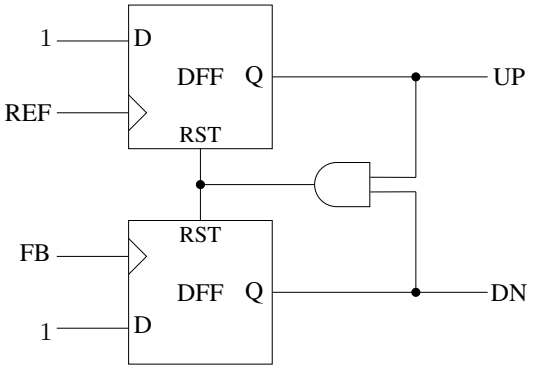

Fig. 2. Conventional Phase Frequency Detector

The transfer characteristics of an ideal PFD is shown in Fig. 3(a). However, in reality, the effective detection range of PFD is less than 2π due to practical limitations. The PFD operation faces limitations at two major phase intervals called dead zone and blind zone. The two non idealities are explained in detail in section II.The proposed design modifies the PFD architecture so as to generate the reset pulse only when the two inputs are close to each other. The proposed PFD removes the dependency of blind zone on the reset pulse which also removes the lower bound defining the blind zone. This design topology aims at low power, highly sensitive (REF and FB slew) and a linear design with zero blind zone for high frequency operations.

The paper is organized as follows, section II discusses the non-idealities of the conventional PFD. Section III discusses the proposed design and working mechanism. Section IV discusses the results obtained during simulations followed by conclusion.

II. Non idealities of Conventional PFD

The *dead zone* is seen in the vicinity of zero phase difference. Here, the pulse width of PFD output signals is not enough for settling of charge pump currents. This creates static phase error and also contributes to jitter. In order to avoid this, both the outputs of PFD are kept ON with the help of a reset pulse. The lower bound of the reset pulse width is a function of the settling time of the charge pump current. The minimal pulse width of reset signal has not decreased significantly with the scaling of CMOS technology. As the

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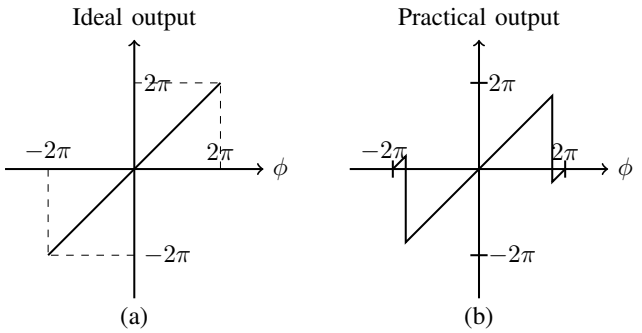

Fig. 3. Normalized characteristic curves of (a) ideal and (b) practical PFDs

frequency of operation increases, the reset pulse occupies a major portion of time period and thereby limits the frequency of operation. The maximum frequency of operation of PFD is given by the width of reset pulse (T_{res}) [11].

$$F_{max} = \frac{1}{2T_{res}} \tag{1}$$

The *blind zone* becomes significant when the phase difference between the two input signals is in the vicinity of 2π which is $[2\pi - \Delta, 2\pi]$ and $[-2\pi, -2\pi + \Delta]$. When the phase difference between the inputs falls into the blind zone and one of the outputs is high, the PFD detects the lagging signal edge first and fails to detect the rising edge of leading phase signal which results in reversed phase information. A phase difference of $2\pi - \Delta$ will be reversed and detected as $-\Delta$ which slows down the acquisition process. Therefore, it is important to alleviate the blind zone which increases the effective operation range of PFD. The blind zone (T_{BZ}) is defined by two components in the conventional design of PFD, the width of the reset pulse (T_{res}) and the precharge time (T_{pch}) of the pull up network [10].

$$T_{BZ} = T_{res} + T_{pch} \tag{2}$$

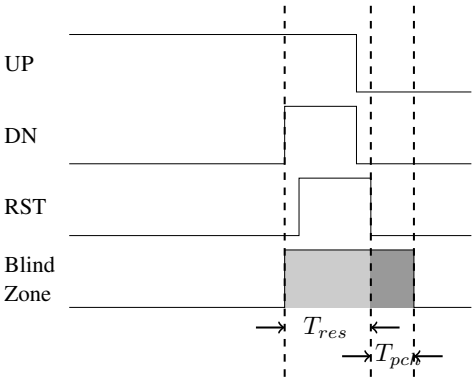

Fig. 4. Blind Zone

The conventional PFD fails to detect transitions in the input signals when the phase difference is large, near 2π. The reset pulse masks the transition of either of the two signals REF and FB. This interval of phase difference is the *blind zone*. At high frequencies, the blind zone occupies major portion of the reference time period which deteriorates the performance of the PLL. This introduces cycle slippage which slows down the frequency acquisition and also defines an upper limit to the maximum operational frequency, F_{max}. The lower bound of reset pulse width mainly depends on the settling time of the charge pump which defines the lower bound of blind zone. Most architectures attempt to push the rising edges out of the reset pulse thus pushing the transition out of the blind zone. But these attempts to alleviate blind zone effects are limited by PVT variations [10].

III. Proposed Design

A number of designs have been developed in the past to suppress the effects of the reset pulse and precharge time to alleviate blind zone range, the common techniques include adding delay elements to the inputs of D Flip Flop [5] which are equal to reset pulse width, thereby reducing the blind zone. The precharge effect can be reduced by adding suitable delayed input signals to the pull up branch [10].

A close look at the PFD operation reveals that reset pulse is essential when the phase difference is extremely small and is not required throughout the input phase difference $[-2\pi, 2\pi]$. Therefore, if the PFD can be designed to incorporate this fact, one can avoid complicated circuits that are used to minimize the blind zone effect. The proposed PFD is designed to provide reset pulse only at small phase differences, but still maintaining its simplicity in architecture.

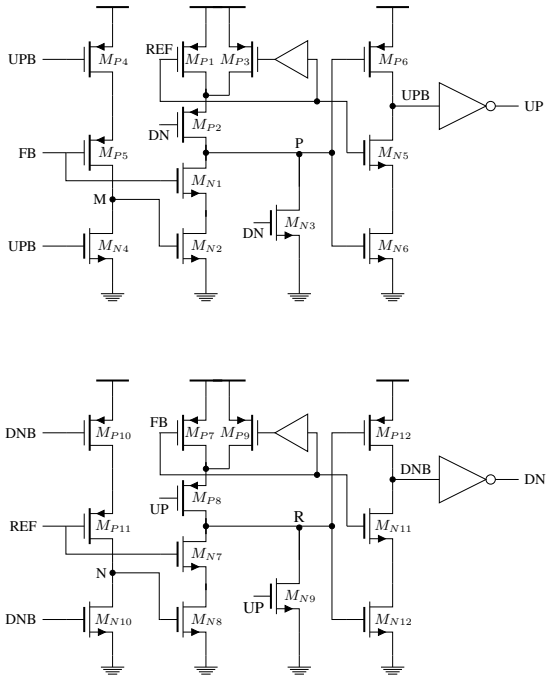

Fig. 5. Proposed Phase Frequency Detector

The proposed PFD is shown in Fig 5 and the corresponding timing diagram in Fig. 6. The pull down branch and the pull up networks of the conventional dynamic PFD have been modified suitably to get the desired operation. The nodes P and R are the decisive nodes in the schematic. The transistors M_{P1}, M_{P2} and M_{P7}, M_{P8} form the pull up networks. The transistors M_{N1}, M_{N2} and M_{N7}, M_{N8} forms one set of pull down network whereas M_{N3} and M_{N9} acts as an additional pull down network.

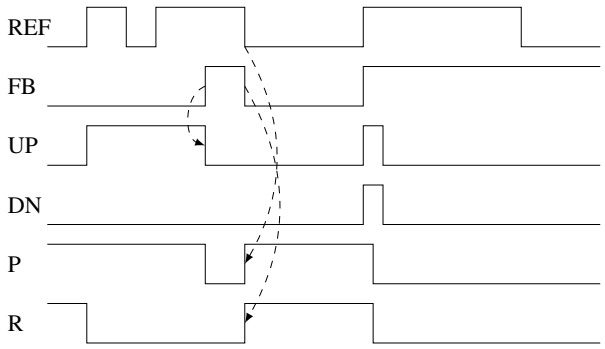

Fig. 6. Timing diagram for the proposed PFD

Initially the inputs (REF and FB) are at logic low and PFD is in the state where UP and DN are at logic low. The nodes P and R are precharged to V_{DD} through their corresponding pull up networks.

A transition in REF signal from low to high will pull down the node UPB through M_{N5}, M_{N6} and UP signal goes to logic high. Thus, the state machine has made a transition to state UP=1 and DN=0. Following this, the node R gets discharged through M_{N9} as soon as UP is driven to logic high and the pull up network M_{P7}, M_{P8} is disabled as gate of M_{P8} is driven high. Further, the node M is charged to V_{DD} through M_{P4}, M_{P5}. Currently, the PFD is in the state UP=1 and DN=0. Any transition in the REF signal will not change the state of the PFD.

In this state, a transition in FB signal from low to high discharges node P through M_{N1}, M_{N2} and UP is pulled down to logic low. As node R had been discharged when UP=1, there is no transition in DN signal. Thus, the state machine makes a direct transition from state UP=1, DN=0 to UP=0, DN=0 unlike conventional designs. The signals UP and DN were pulled down through different sets of pull down branches which eliminated the need for explicit reset pulse at phase difference greater than dead zone range. A similar working explanation can be provided transition to state UP=0, DN=1 by transition in signal FB followed by signal REF. This happens when the delay between the two input signals is greater than the dead zone range.

In the above case, if the delay between the two signals is very small that the phase difference is within the dead zone, P and R being precharged to high will pull up both UP and DN signals. As soon as UP and DN make a transition to logic high, the nodes P and R are pulled down through M_{N3} and M_{N9} transistors correspondingly. Thus, we get a minimal width Reset pulse without the need for an explicit reset pulse generation circuit. With suitable scaling of M_{N3} and M_{N9}, the width of reset pulse can be modified. The strength of pull down path formed by M_{P1}, M_{P2} and M_{P7}, M_{P8} should be more than pull up network to ensure proper operation for phase difference in the range $[\pi, 2\pi]$ and $[-2\pi, -\pi]$ ensuring no reversal in phase information.

The blind zone of the network is still present because of large precharge time of internal nodes P and R. A general technique to alleviate this effect is to add precharge transistors. We have added two transistors M_{P3} and M_{P9} driven by delayed input signals to turn on the pull up paths at the rising transition of the inputs. The delay added should be equal to the precharge time (T_{pch}), this completely eliminates the blind zone. Further the signals UP and DN fed to the pull down branches M_{N3} and M_{N9} can also be delayed to increase the stability of the system and modify the width of reset pulse.

IV. Simulation Results

The design is implemented in 180 nm CMOS technology. The PFD consumes power of 1.36 mW when operated at an input frequency of 1 GHz with a supply of 1.8 V. The design was subjected to multiple tests to verify its functionality and to benchmark its improvement.

To examine the performance of the proposed design a Phase Locked Loop test bench was set up using Verilog-AMS to provide an identical environment to the blocks under test as shown in Fig 7. To test the functionality, the conventional D-Flip Flop based PFD and the proposed PFD were subjected to 500 MHz reference within the loop. The proposed PFD outperformed the conventional PFD by faster acquisition and lesser cycle slippage.

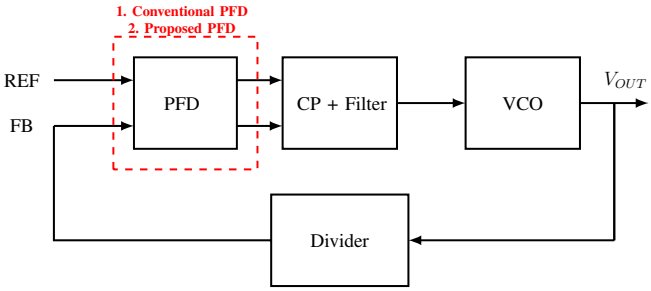

Fig. 7. Test bench for PFD functionality in the loop

A similar test bench was set up for a frequency synthesiser with the PFD input at a frequency of 1 GHz, from another frequency synthesiser. It is observed that the cycle slippage has significantly reduced in the proposed PFD due to the eliminated blind zone. Acquisition of PLL with proposed and conventional PFDs is compared in Fig. 8. Clearly, PLL with proposed PFD offers faster frequency acquisition. The decrease in frequency acquisition time is found to be around 18% for 1GHz which is in good coherence with the literature.

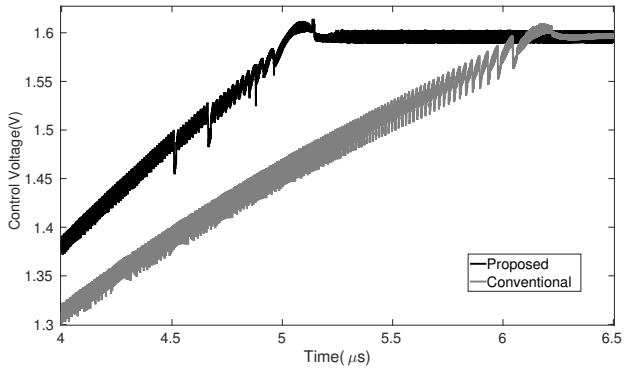

Fig. 8. Around 18% faster frequency acquisition is observed in the proposed PFD as compared to the proposed PFD

The proposed PFD was also simulated for all corners, with 1 GHz input. The normalized transfer characteristics of the proposed PFD for typical (TT) corner and the two extremes slow-slow (SS) and fast-fast (FF) corners are shown in Fig 9. The design maintained a good performance to yield faster acquisition.

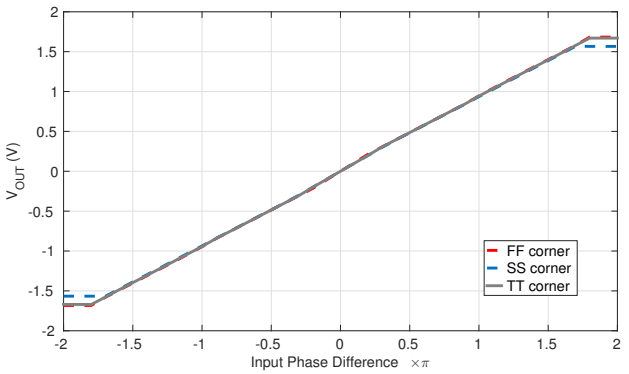

Fig. 9. Transfer curves for corners for an operating frequency of 500MHz

The proposed PFD is compared with some of the designs found in literature w.r.t. power in Table I.

TABLE I
SIMULATION RESULTS AND COMPARISON

Ref	Supply	Technology(μm)	Power(mW)
[5]	-	0.25	1.4 @500MHz
[6]	1.8	0.18	1.56 @500MHz
[7]	1.2	0.13	1.44 @1GHz
This work	1.8	0.18	1.36 @1GHz

V. CONCLUSION

The explicit reset mechanism is the major contributor to the blind zone. The input detection range and linearity is deteriorated by the blind zone. As the mechanisms to alleviate effect of reset pulse on blind zone is limited by PVT variations, a new circuit topology has been proposed which removes the need for an explicit reset pulse. The effect of reset pulse on blind zone has been completely removed. The effect due to precharge time is eliminated through application of delayed inputs which nullifies the blind zone completely. With improved linearity, this topology reduces the cycle slippage and improves the acquisition rate of locking. The proposed design involves a simple design modification in the pull down network and operates at very high frequency with relatively low power consumption.

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