Design and Analysis of Multi-Loop Feed Forward Control Schemes for DVR under Distorted Grid Conditions

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Abstract— Voltage sags are considered as important power quality problems and the Dynamic Voltage Restorer(DVR) is an effective solution to mitigate the sags and other power quality problems related to voltage. The DVR involves two major aspects: (i) reference generation and (ii) control algorithm. Under unbalanced grid conditions the presence of negative sequence components in the grid voltage causes sustained oscillations in the estimated *dq*- voltages, which makes sag detection difficult with conventional SRF-PLL and there by chances of controller malfunctioning. In this paper, a Delayed Signal Cancellation (DSC) pre-filter based Positive and Negative Sequence Extractor (PNSE) is employed to extract the Instantaneous Symmetrical Components (ISC) of the grid voltage and filter out the harmonic voltages from the estimated *dq*-voltages. As the response of the DVR mainly depends on the controller action this paper presents an multiloop PI feed forward controller for enhancing the operation of DVR under distorted grid conditions. The efficacy of the proposed controller is illustrated by comparative study with multiloop feed forward P controller using time response and relative stability analysis. Simulation studies are performed in PSCAD/EMTDC for a 10kV medium voltage DVR under various voltage disturbances such as symmetric and asymmetric voltage sags.

Keywords—DVR; Instantaneous Symmetrical Components(ISC); Multiloop Feed Forward controller;

I. INTRODUCTION (*HEADING 1*)

In India, renewable generation from wind and solar has increased substantially during past few years and forms a significant proportion of the total generation in the grid. Indian government is looking forward for facilitating large scale integration of such variable Renewable Energy Sources (RES), keeping in view the security of the grid. The basic technical challenge comes from the variability of wind and solar power which affects the load, generation balance, varying demand for reactive power and impact on voltage stability.

Wind farms in India connected to 66 KV or above are governed by Indian Electricity Grid Code (IGEC) [1] as per the Electricity Act, 2003. As per IEGC wind farms connected at or above 66 kV should remain connected to the grid during system fault as specified in following Fig.1 and can be disconnected from the grid only if the operating point falls below the specified value. V_{pf} represents the minimum voltage required for normal operation of wind turbine which is about 80% of nominal system voltage and V_f represents 15% of nominal system voltage. During grid voltage unbalance, active and

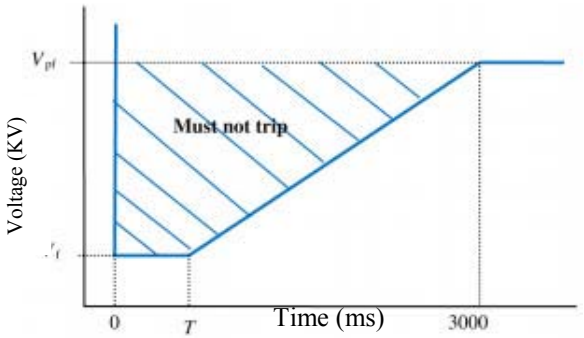

Fig.1. Fault clearing time and voltage limits of IGEC

reactive power, dc-link voltage, and also the THD in grid current need to be curtailed. Hence custom power devices like DVR [2], [3], [4] are installed with proper control which incorporates the features such as compensation of voltage sags, swells and harmonics mitigation.

Several works has been done on different aspects of DVR performance. Control of DVR for fast detection and its respective compensation plays significant role. The literature presents several algorithms for control of DVR such as Open Loop Control [5], Voltage Feedback Control [6], [9], Multiloop Control [7], [8] and Multiloop Control with Feedforward Path [10],[16]. In open loop control the frequency response of the system has inadequate phase and gain margin. Further the damping of the system with open loop control of DVR is unsatisfactory [16]. In single voltage loop control the trade off between steady state response, transient response and stability is quite demanding because large control gains are generally required for good steady state and transient performance but it generally deteriorate the system stability. On the other hand if smaller gain is used to ensure adequate stability margin a significant steady state error may appear and system may react much slower[6].

To obtain the optimum value of the controller parameter root locus design (RLD) [11],[12],[13] is used as it is the most effective tool for tuning the values of controller parameter[14]. It provides the knowledge about the location of poles and its range based on which controller parameter can be designed [15] but it is a single parameter design method. To overcome this limitation in this paper an extended RLD [14], [15] method is used.

So far in literature multiloop feedforward controller involves

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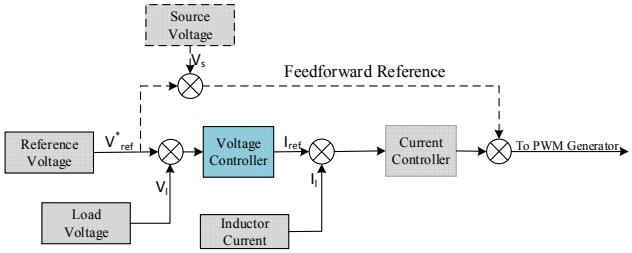
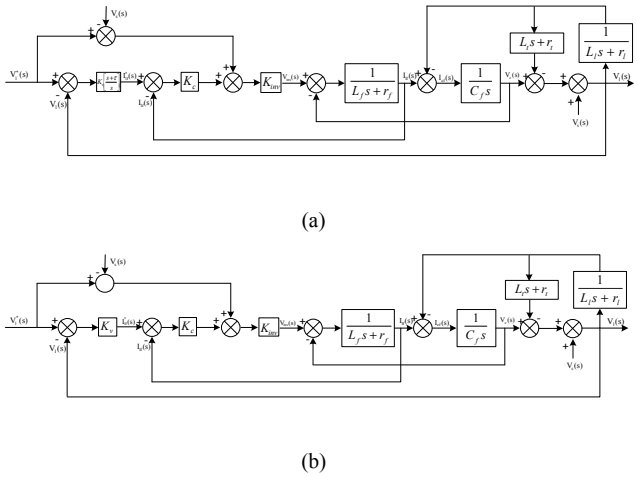


Fig.2. General control scheme for DVR

propotional controller(outer loop)[5],[6],[7],[8] but in this paper an attempt is made to develop a multiloop feedforward control structure with PI controller(outer loop) to improve the dynamic performance of DVR. This paper discuss about design and analysis of multiloop feed forward scheme by replacing the popularly adopted P controller with PI controller for voltage control. During unbalance grid conditions, harmonic ripple is observed in *dq*-voltages of a conventional SRF-PLL which makes it difficult to detect sag and thereby causes maloperation of DVR . Thus filtering techinique is required. In this paper DSC pre-filter is used to filter out these ripples which is discussed in detail [17].The contents are organised as follows: section II describes multiloop feed forward structure with P and PI controller. Further tuning procedure is explained and comparative studies of time response and relative stability analysis with repective to P and PI controllers is presented. In section III, multiloop feed forward PI based scheme is validated by a medium voltage (MV) DVR connected to 10 kV MV-level distribution system which is developed in PSCAD/EMTDC.

II. CONTROL OF DVR

Multiloop controller generally consists of two loops, the outer loop as voltage feedback which aims for regulating the load voltage and the inner loop as current feedback which enhances the dynamic response of the system. Further the voltage loop can have either load voltage [10] or capacitor voltage [15] as feedback. From simulation studies, it is found that when capacitor voltage is considered as a feedback the steady state value of the load voltage is slightly less than the reference value (the difference is same as the transformer loss). Therefore, load voltage feedback is considered in the outer loop. Similarly, current loop can have either inductor current [15] or capacitor current [14] as feedback but in this paper for analysis purpose, the inductor current is considered as current loop feedback. This section primarily focusses on the design of voltage controller (outer loop) with proportional controller based inner loop (current control) as fixed and further, analysis of multiloop feedforward control scheme with P and PI controllers for voltage control (outer loop) is performed to figure out the better scheme. The general control scheme for DVR is illustrated in Fig. 2. In Fig.2 it is shown that when voltage sag occurs the DVR load-side voltage is compared with its reference value and the error is multiplied with the voltage error feedback gain and fed to the second stage as a reference for the current loop. This current reference is compared with the actual inductor current and the error is multiplied with the current error gain to form the inner feedback loop. The resulting quantity of this loop is subsequently fed to the PWM generator of the inverter.



(a)

(b)

Fig.3. Block diagram representation of multiloop feedforward controller (a) P-based controller (outer loop) (b) PI based controller (outer loop)

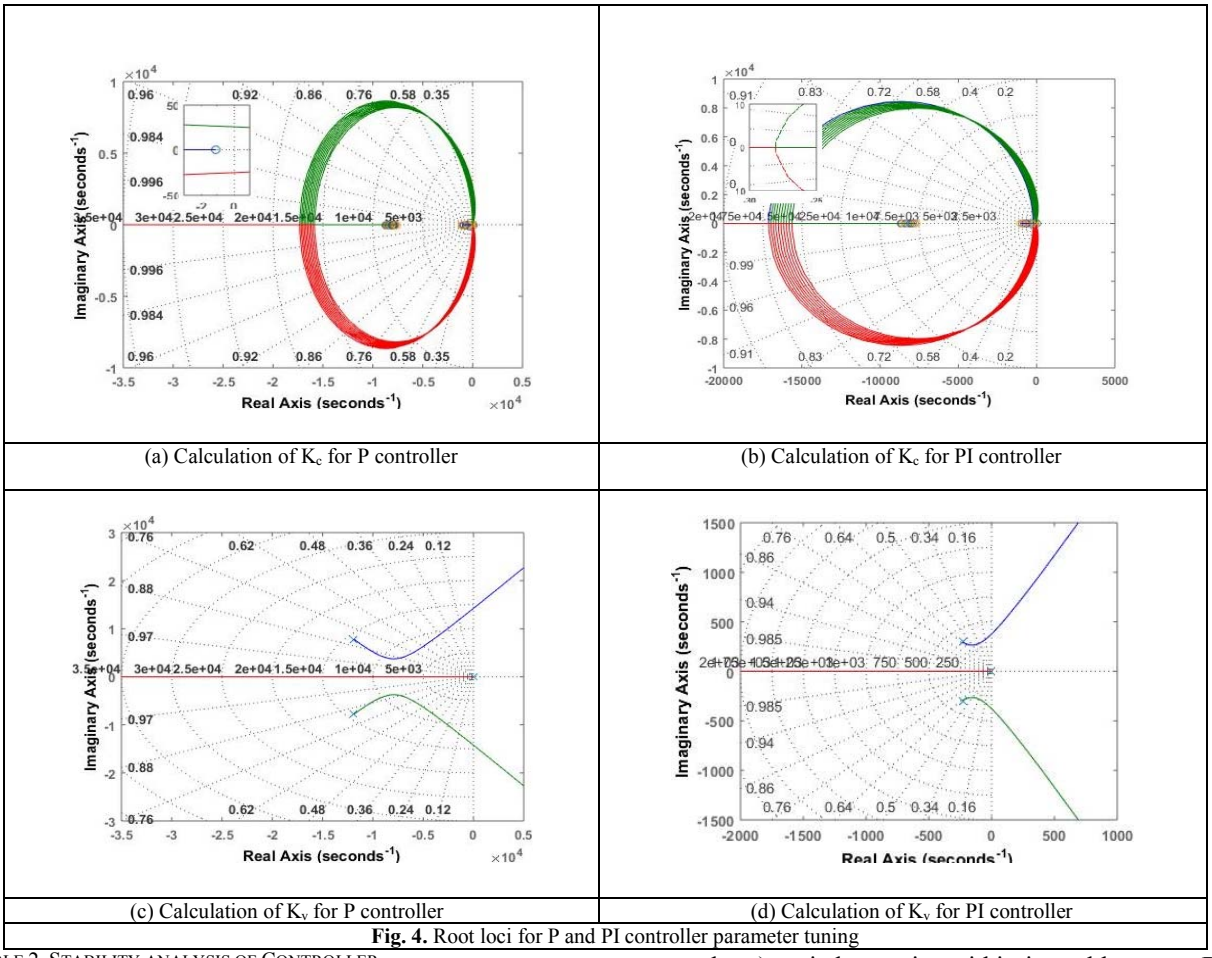
The multiloop feedforward control structure with P and PI controller in voltage loop (with fixed P based controller in current loop) is shown in Fig.3. The closed loop transfer function of respective control scheme (Fig. 3(a), (b)) is given in Table 1. It can be observed from the transfer function of multiloop feedforward controller (P and PI): (i) with respect to reference voltage: terms $K_{inv}(L_l s+r_l)$ and $K_{inv}s(L_l s+r_l)$ are added in the numerator and (ii) with respect to load voltage: the term $K_{inv}(L_l s+r_l)$ and $K_{inv}s(L_l s+r_l)$ are reduced in the numerator when compared with multiloop without feedforward transfer function. This implies that, it upsurges the DVR capability to track its reference value and downturn the effect of source voltage. Also, adding feedforward path does not affect the stability of the system as it does not change the characteristic equation of the controller (compare to without feed forward) which is observed from their respective transfer function. Further the inherent delay in feedback signal of the control system can raise to problems like excessive overshoot and undershoot in the injected voltage following a sudden change in $V_s(s)$. With addition of feedforward signal to the inverter input voltage provides instantaneous response to the change in $V_s(s)$ and thereby overcomes the above issues. Finally, it can be concluded that multiloop feedforward controller is better than the multiloop without feedforward and in this paper for further analysis multiloop feedforward controller is considered.

A. Parameter Tuning

The objective of tuning the controller is to find the gain parameters of P and PI for achieving the faster-dynamic response and enhancing the relative stability of DVR. Generally, root locus method is used to design the parameters of controller. The conventional root locus method [11], [12], [13] is a single parameter design method i.e. it cannot track the optimal value of multiple controller parameters (such as three parameter K_v, K_c and ζ in PI controller) simultaneously. So, in this paper an extended RLD method [14], [15] is adopted to tune the controller parameters. Fig. 4 shows the extended RLD for tuning the parameters of P and PI controller.

TABLE 1. CLOSED LOOP TRANSFER FUNCTION

Voltage/ Current Controller	With respect to reference voltage	With respect to load voltage
P / P	$G_{a4} = \frac{n_{a41}\, s + n_{a40}}{d_{a43}s^3 + d_{a42}s^2 + d_{a41}\, s + d_{a40}}$	$G_{b4} = \frac{n_{b43}s^3 + n_{b42}\, s^2 + n_{b41}\, s + n_{b40}}{d_{b43}s^3 + d_{b42}s^2 + d_{b41}\, s + d_{b40}}$
PI / P	$G_{a5} = \frac{n_{a52}\, s^2 + n_{a51}\, s + n_{a50}}{d_{a54}s^4 + d_{a53}s^3 + d_{a52}s^2 + d_{a51}s + d_{a50}}$	$G_{b5} = \frac{n_{b54}s^4 + n_{b53}s^3 + n_{b52}\, s^2 + n_{b51}s + n_{b50}}{d_{b54}s^4 + d_{b53}s^3 + d_{b52}s^2 + d_{b51}s + d_{b50}}$



(a) Calculation of K_c for P controller

(b) Calculation of K_c for PI controller

(c) Calculation of K_v for P controller

(d) Calculation of K_v for PI controller

Fig. 4. Root loci for P and PI controller parameter tuning

TABLE 2. STABILITY ANALYSIS OF CONTROLLER

Parameters	PI controller with FF path	P controller with FF path
Gains	K_c, K_v and τ	K_c and K_v
Relative Stability	3.5	2e-05
Damping Factor	1	1

To tune the value of K_c, the root locus for K_c is drawn for each value of K_1 and K_2 varied stepwise from its minimum stable value to maximum stable value obtained by Routh Hurwitz(RH) Stability Criterion as shown in Fig. 4(b). Based on maximum relative stability the optimal value of K_c is obtained. Similarly, for tuning K_v shown in Fig.4(d), the root locus of K_2 (proportional gain of outer loop) is plotted for the obtained value of K_c and each value of K_1 (integral gain in outer loop) varied stepwise within its stable range. Based on maximum relative stability the optimal value of K_2 is obtained. From the obtained values of K_c (Fig. 4(b)) and K_2 the root locus is plotted for transfer function having gain K_1 and its value is calculated based on relative stability. The ratio of K_1 and K_2 (τ) graph is shown in appendix. Similar procedure is followed for P controller. To design the controller with high robustness, relative stability is considered for optimum tuning of controller parameters. It is essential that tracking accuracy of the load voltage should be sustained during voltage sags. Further, it is important to note that each parameter is bounded to its physical implementation. Table 2 showcase the tuned gains of the controller along with their relative stability. It indicates that the relative stability of PI is

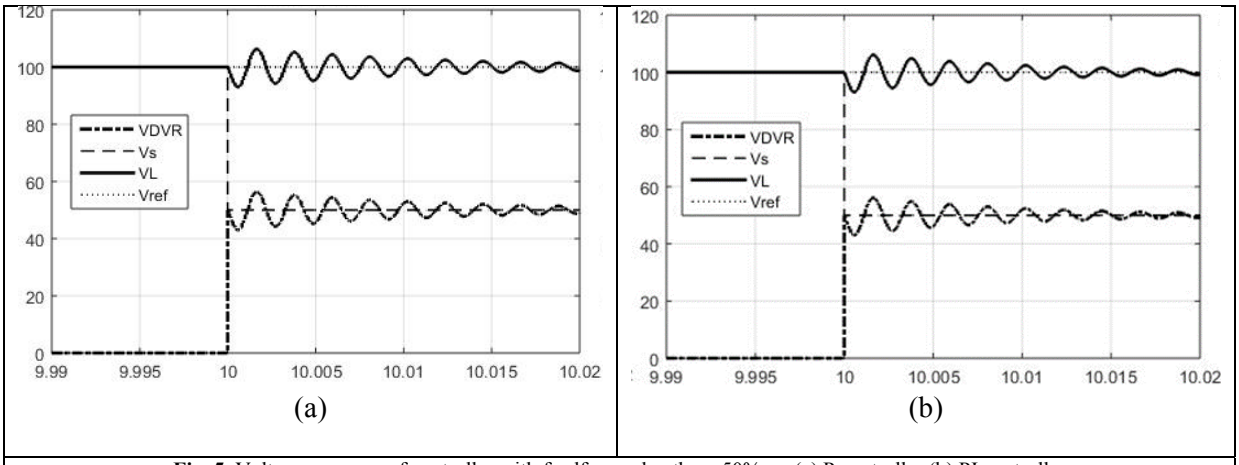


Fig. 5. Voltage response of controller with feedforward path on 50% sag(a) P controller (b) PI controller

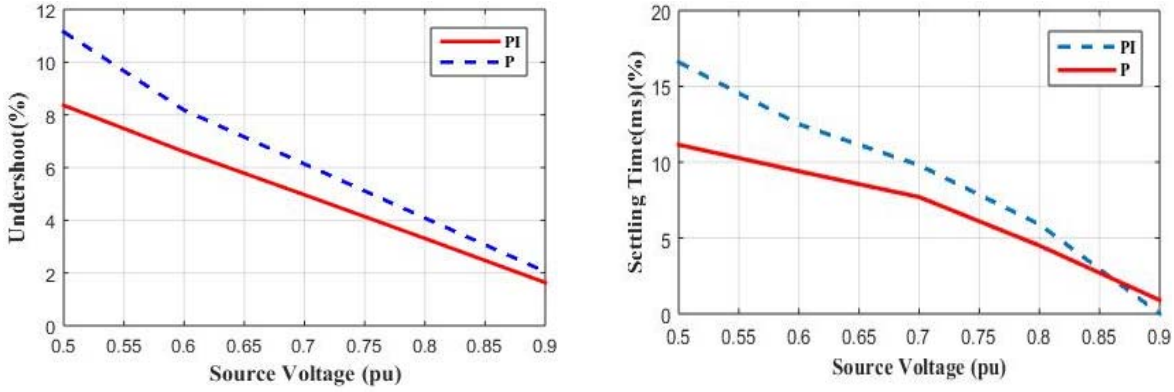


Fig. 6. Time Response of System with Source Voltage Variation: (a) Undershoot (b) Settling Time

much larger than the P controller. Stability margin signifies that for wide voltage distortions may cause P controller to get into unstable region. The preceding subsection discuss the performance analysis of controller in terms of overshoot and settling time. Thus, controller gains obtained in this subsection are utilized for the time response analysis.

B. Time Response Analysis:

To study the dynamic performance of DVR the multiloop feed forward control structure (both P and PI) is implemented in *dq*-frame. The supply voltage (V_s) is subjected to 50% sag (extreme case) and the voltage response is plotted as shown in Fig.5 by assuming PLL as an ideal one (i.e. there is no delay involved in tracking the phase angle) and also assuming PLL pre-filter is perfect (i.e. *dq* voltages are perfect DC). From Fig.5 it can be observed that the instant when the sag is created DVR starts injecting the compensation voltage to maintain constant nominal value of load voltage. Further it can be seen that both DVR and load voltages are subjected to some oscillation before settling down to its final value. The maximum deviation from its final value and the time taken by the load voltage to settle within its final value depends on the type of the controller used. In case of P and PI controller the maximum deviation of load voltage from its reference value is 11.15% and 8.36% respectively. The time response of controller is verified by creating a sag of 0.1 pu to 0.5 pu as shown in Fig. 6. When the sag is more than 0.45 pu the PI has an undershoot of 8.36% whereas P has an undershoot of 11.15% and on the other hand P has settling time of 11.5ms whereas PI has 16.6s. It looks P performs slightly better in terms of settling time, but overall PI has low undershoot as compared with P as shown in Table 3. From Table 3 it can be easily seen that though the P controller has better settling time, its stability margin is very less (Table 2) and some slight variation in the system parameters may leads to its instability. PI controller has better relative stability and less overshoot compared to P. So, PI controller is preferred for considered system.

Table 3 Time Response of P, PI controller with FF path for Voltage sags. Table Styles

Supply Voltage (pu)	Undershoot (%)		Settling Time(ms)	
	PI	***P***	***PI***	***P***
0.9	1.635	2.05	0	0.9
0.8	3.31	4.085	5.9	4.5
0.7	4.965	6.137	9.8	7.7
0.6	6.6	8.18	12.5	9.4
0.5	8.36	11.15	16.6	11.15

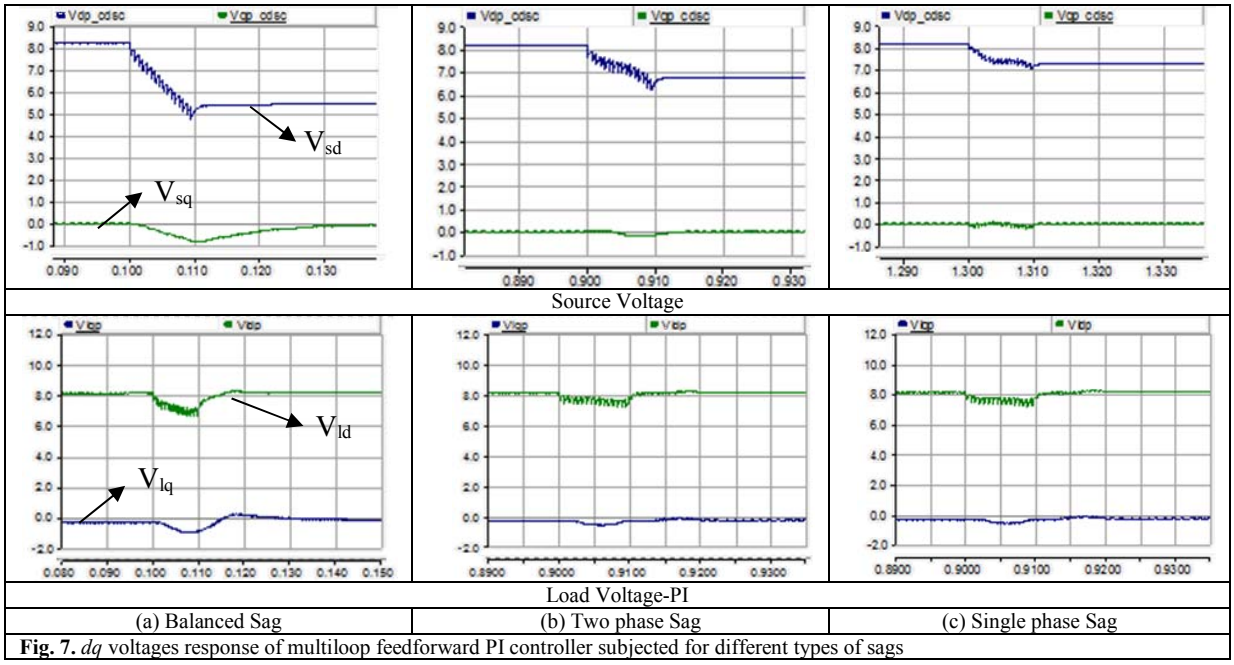


Fig. 7. *dq* voltages response of multiloop feedforward PI controller subjected for different types of sags

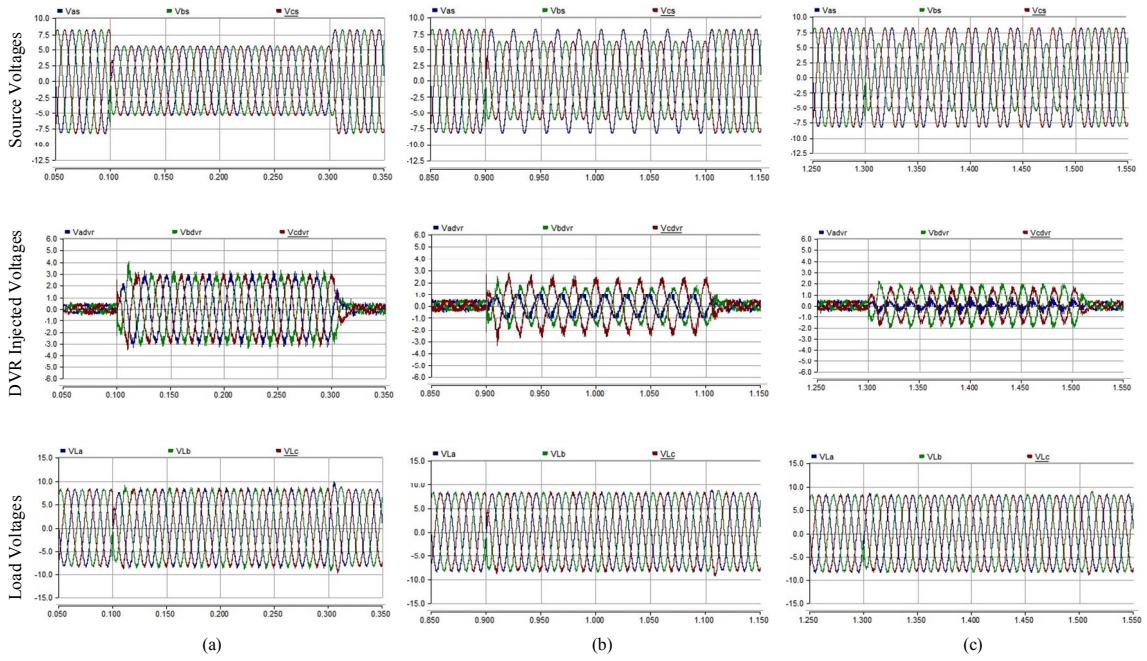


Fig.8. Simulation results of PI feed forward voltage controller based DVR under (a) Balanced sag, (b) Two phase sag, (c) Single phase sag

III. Simulation Results

In this section, a real-time simulation (PLL dynamics are considered) of 10kV, 1MVA medium voltage DVR is implemented in PSCAD to verify the efficacy of DSC prefilter based multiloop feedforward PI control. Fig. 7 shows *dq* load voltage response (V_s – source voltage, V_l – load voltage) of PI controller for symmetric and asymmetric voltage sags. The following discuss the different scenarios considered for the simulation studies. At first a balanced three-phase symmetric fault scenario is created at t=0.1s which results in three-phase voltage sag. The grid voltage drops to 70% of its nominal value. However, by observing the load and DVR voltage it is clear that the DVR compensates and maintains the load voltage at its nominal value. In second scenario (Fig. 7(b)) a two-phase fault is created at t=0.9s for 200ms. It results a voltage drop of 30% at its nominal value in phase-b and phase-c creating an unbalanced sag situation. It can be clearly observed that though there is unbalance sag in source voltage the DVR control scheme maintains the load voltage to its nominal value as

shown in Fig. 7(b). Fig7(c) depicts the third scenario where DVR control scheme is tested for single-phase sag. Starting from t=1.3s a fault is created for 200ms which reduce the source voltage of phase-b to 70% of its nominal value and the DVR maintains the load voltage constant. From the Fig.7 it is observed that transients in the load voltage slightly differs from the results obtained in the section II. It is due to introduction of PLL dynamics considered in the real-time system. Further for the multiloop feedforward PI controller, the three phase-abc waveforms are shown in Fig. 8. It is observed that the DSC pre-filter based multiloop feed forward PI controller for DVR compensates the voltage disturbances viz balanced and unbalanced sags.

IV. Conclusion

In this paper, a multiloop feed forward PI controller (voltage control) is presented to enhance the operation of DVR under distorted grid conditions. DSC-PLL is used to extract the instantaneous symmetrical components of grid voltage and filter out the harmonic voltages from the estimated *dq*-voltages. The considered multiloop structure consists of outer loop (capacitor voltage feedback) and an inner loop (inductor current feedback). Firstly, advantages of multiloop feedforward structure is presented and comparative studies (relative stability and time response analysis) are carried out between P and PI controllers to figure out the better scheme. From the analysis, it is observed that the relative stability of PI controller is higher than the P controller and though P controller seems to have better settling time, but it exhibits more overshoot compared to PI. Thus, PI controller performs better with wide stability margin and less undershoot. The efficacy of the multiloop PI controller is validated through medium voltage DVR using PSCAD simulations.

Acknowledgment

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Appendix

$n_{a41} = (K_vK_c+1)K_{inv}L_l : n_{a40} = (K_vK_c+1)K_{inv}r_l : d_{a43} = C_fL_f(L_l+L_t)$
$d_{a42} = C_f(L_fr_l + L_lr_f) + K_cK_{inv}C_f(L_l+L_t) + C_f(L_tr_f + L_fr_t) + C_fL_f :$
$d_{a41} = C_fr_f(r_l+r_t+1) + K_vK_cK_{inv}L_l + K_cK_{inv}C_f(r_l+r_t) + L_l + L_t :$
$d_{a40} = K_vK_cK_{inv}r_l + K_cK_{inv} + r_l + r_t : n_{b43} = C_fL_fL_l : n_{b42} = C_f(L_lr_f + L_fr_l) + K_cK_{inv}C_fL_l$
$n_{b41} = K_cK_{inv}C_fr_l + C_fr_lr_f + L_l - K_{inv}L_l : n_{b40} = (1-K_{inv})r_l$

The value of d_{b40}, d_{b41}, d_{b42} and d_{b43} is same as d_{a40}, d_{a41}, d_{a42} and d_{a43} respectively.

$n_{a52} = (K_c+1)K_{inv}L_l : n_{a51} = K_cK_{inv}(L_l+\tau r_l) + r_l : n_{a50} = K_cK_{inv}\tau r_l :$
$d_{a54} = C_fL_f(L_l+L_t)$
$d_{a53} = C_f(L_fr_l + L_lr_f) + K_cK_{inv}C_f(L_l+L_t) + C_f(L_tr_f + L_fr_t) + C_fL_f :$
$d_{a52} = C_fr_f(r_l+r_t+1) + K_vK_cK_{inv}L_l + K_cK_{inv}C_f(r_l+r_t) + L_l + L_t :$
$d_{a51} = K_vK_cK_{inv(}L_l+\tau r_l) + K_cK_{inv} + r_l + r_t : d_{a50} = K_vK_cK_{inv}\tau r_l :$
$n_{b54} = C_fL_fL_l$
$n_{b53} = C_f(L_lr_f + L_fr_l) + K_cK_{inv}C_fL_l : n_{b52} = K_cK_{inv}C_fr_l + C_fr_lr_l + (1-K_{inv})L_l : n_{b51} = (1-K_{inv})r_l : n_{b50} = 0$

The value of d_{b50}, d_{b51}, d_{b52}, d_{b53} and d_{b54} is same as d_{a50}, d_{a51}, d_{a52}, d_{a53} and d_{a54} respectively.

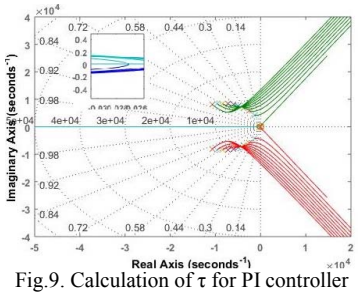

Fig.9. Calculation of τ for PI controller

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