Design and FPGA Implementation of Dual Self-Tuning Filter based Controller for Single Phase Shunt Active Filter

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***Abstract*—The use of power electronic devices injects harmonics into the grid causing serious power quality problems. To limit the current harmonics in accordance with IEEE Std 519, Shunt Active Power Filter (SAPF) may be used. Instantaneous power theory (pq theory) is widely used for current harmonic mitigation in SAPF. The Low Pass Filter (LPF) is used in pq theory based controllers for fundamental component extraction. The drawbacks of LPF are additional phase delay at the fundamental frequency and presence of lower frequency oscillations. A dual Self-Tuning Filter based controller is proposed to overcome these limitations. The simulation studies under different system conditions are carried out using MATLAB/SIMULINK to verify the effectiveness of the proposed method. The hardware co-simulation using ZedBoard Zynq-7000 Development Board is carried out to validate the simulation results.**

***Index Terms*—Shunt Active Power Filter, pq-theory, PI controller, Self Tuning Filter, Current harmonic mitigation**

I. Introduction

The use of power electronic devices are increasing exponentially. These devices inject harmonics into the grid, which leads to a serious distortion of the power supply current and voltage, decreasing the quality of power supply. Passive and active filters can be used for harmonic compensation. However, passive LC filters are bulky, load dependent and inflexible. They can also cause resonance problems in the system. To overcome these disadvantages, shunt active power filters (SAPF) are introduced, which compensate for the current harmonics and reduce the total harmonic distortion (THD).

Shunt Active Filter based controller has two control loops i.e DC-link Voltage Control and Current harmonic mitigation. There are two classes of methods for current harmonics mitigation: the frequency methods and the time domain methods. The frequency methods are based on the Fast Fourier Transformation (FFT) [1] and the Recursive Discrete Fourier Transformation (RDFT) [2]. These methods involve heavy calculation and require a lot of memory. The time domain methods are more preferred because of their fast response and simple design. Some of the commonly used time domain methods are the p-q method of instantaneous power [3]–[6] and the d-q method (fundamental frequency and/or higher harmonics) [7]. Implementation of pq method [8] is simple. However, it has a limitation of poor performance under distorted grid conditions. From literature, it is observed that the pq method uses a low pass filter (LPF) [9] for fundamental component extraction. The limitations of LPF are phase delay at fundamental frequency and presence of lower frequency oscillations.

In this paper, a dual self-tuning filter (STF) based pq method is used for current harmonic mitigation to overcome the drawbacks of the classical pq method. PI controller is used for DC link voltage control.

II. System Description

The block diagram of a single phase SAPF is in Fig *1*, where i_s is the source current, i_l is the load current, i_c is the current used for compensating the load harmonics and reactive power, u_s is the source voltage. The SAPF comprises of a DC link capacitor (C_{dc}), a filter inductor (L_c) and a single-phase voltage source inverter with four controllable switches. u_{dc} is the voltage across C_{dc} and L_l is the surge impedance.

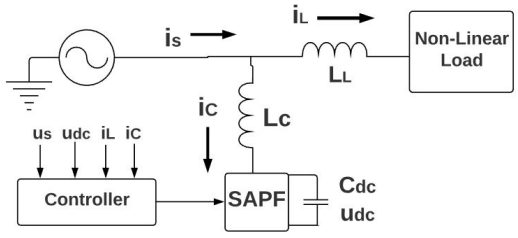

Fig. 1: Block diagram of single-phase SAPF

III. Controller Design

The block diagram of a SAPF control scheme is shown in Fig.*2*. It consists of a PI controller, Reference current calculator and Hysteresis controller. Source voltage and load

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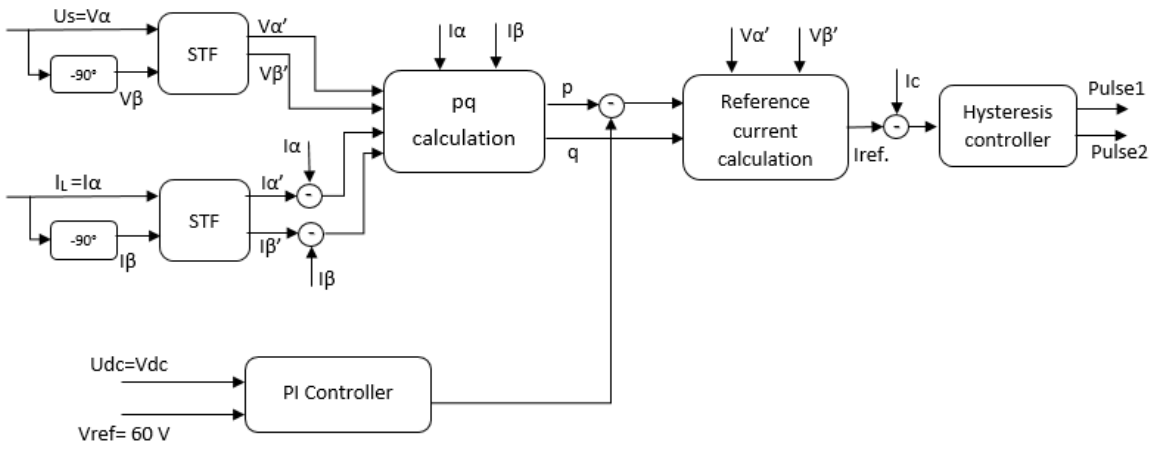


Fig. 2: Block diagram of single-phase SAPF controller

current are sensed and transformed into a fictitious alpha-beta frame by adding a delay of 90^o. These signals are then fed as inputs to two STFs. STF extracts the fundamental component of the signal with zero phase delay. The harmonic component of the load current is obtained by subtracting the output of the STF from the original signal. p and q are then calculated by using equations (2) and (3). PI controller is used for DC link voltage control. The output of the PI controller is subtracted from the p component. The reference current is calculated using equations (4) and (5). The reference current is then subtracted from the compensation current and the error is then fed as inputs to the hysteresis current controller so as to generate the desired pulses.

A. *Self-tuning Filter*

Fig *3* shows the frequency response of LPF for fundamental frequency of 50Hz. It can be observed that, there is a phase delay and attenuation at the fundamental frequency.

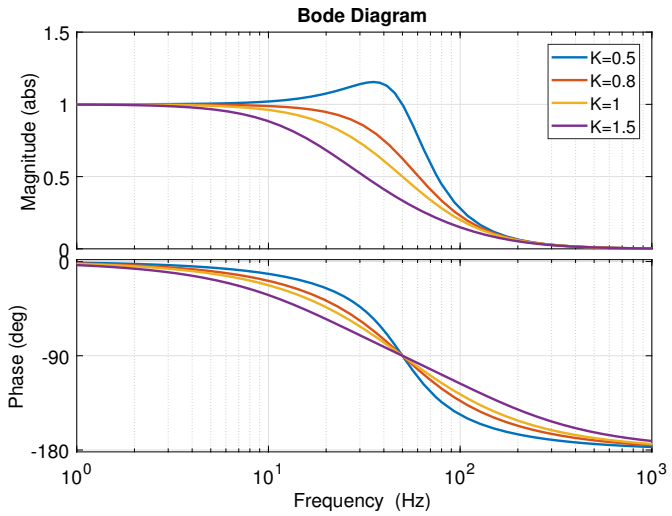


Fig. 3: Bode Plots of second order LPF

STF [10] has zero attenuation and zero phase delay at the fundamental frequency. The frequency response of STF is shown in Fig *4*. It acts as an integrator in the alpha-beta

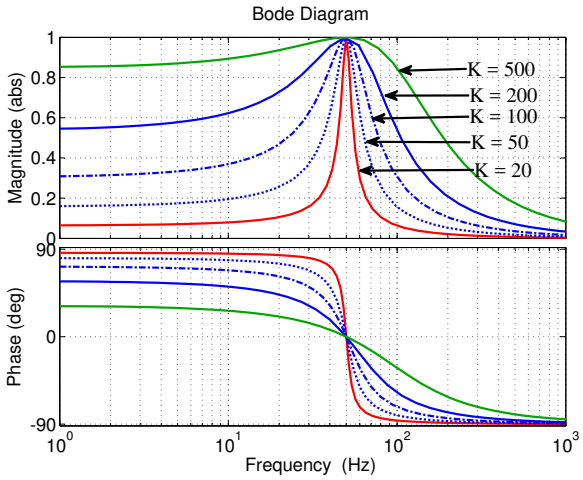


Fig. 4: Bode Plot of STF

domain. The block diagram of STF is attached in Fig.*5*. The resonant frequency for integrator is ω. The integrator output is negligible for frequencies other than ω. The gain K and the feedback loop act as an error correction part of the circuit. Hence, by choosing the desired frequency ω_1, the required output can be obtained. The transfer function of STF is given as:

$$H(s) = K\frac{s + K + j\omega_1}{(s + K)^2 + (\omega_1)^2} \tag{1}$$

B. *p-q Calculation*

The p-q theory is a generalized theory of the instantaneous reactive power in three-phase circuits. It is a tool used for the control of active power and analysis of three phase power systems in order to detect problems related to harmonics, reactive power and unbalance [3]. The equations of p-q

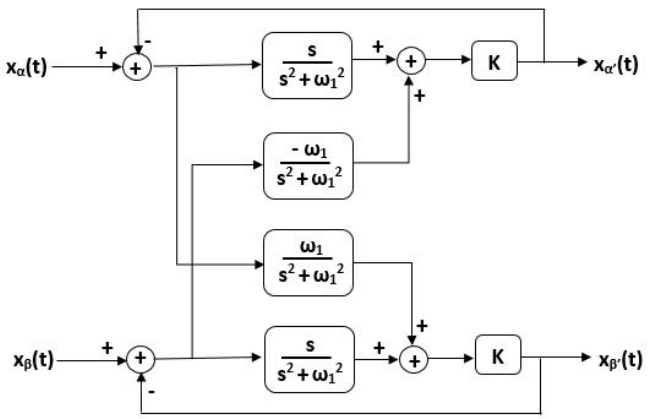


Fig. 5: Block diagram of Self-tuning filter

calculations are as follows:

$$p = V_{\alpha'}(I_{\alpha h}) + V_{\beta'}(I_{\beta h}) \tag{2}$$

$$q = V_{\alpha'} I_{\beta} - V_{\beta'} I_{\alpha} \tag{3}$$

Here, p is the instantaneous active power and q is the instantaneous reactive power. $V_{\alpha'}$ and $V_{\beta'}$ are the fundamental components of the source voltage. $I_{\alpha h}$ and $I_{\beta h}$ are the harmonic components of the load current. $I_{\alpha'}$ and $I_{\beta'}$ are the fundamental components of load current.

C. PI Controller

PI controller consists of a feedback control loop that calculates an error signal by taking the difference between the output of the system and the reference point. The transfer function of PI controller is of the form $(K_p + \frac{K_i}{s})$ where K_p and K_i are constants.

D. Reference Current Calculation

The equations to calculate the reference compensation currents are given by:

$$I_{\alpha\_ref} = \frac{V_{\alpha'} * p - V_{\beta'} * q}{V_{\alpha'}^2 + V_{\beta'}^2} \tag{4}$$

$$I_{\beta\_ref} = \frac{V_{\beta'} * p + V_{\alpha'} * q}{V_{\alpha'}^2 + V_{\beta'}^2} \tag{5}$$

Here, I_{α_ref} is the reference alpha current and I_{β_ref} is the reference beta current.

E. Hysteresis Controller

Hysteresis controller compares the Voltage Source Inverter (VSI) current with that of the reference current and pulses are generated accordingly. These pulses are given as gating signals to the switches of VSI. The logic of hysteresis current control is as follows:
If i_c is less than (i_{ref} - HB) S_1, S_4 ON and S_2, S_3 OFF
If i_c is greater than (i_{ref} + HB) S_1, S_4 OFF and S_2, S_3 ON
Here, S_1, S_3 are the upper switches of the two legs and S_2, S_4 are the lower switches. HB is the hysteresis band. i_c is the compensation current and i_{ref} is the reference current calculated.

IV. Results

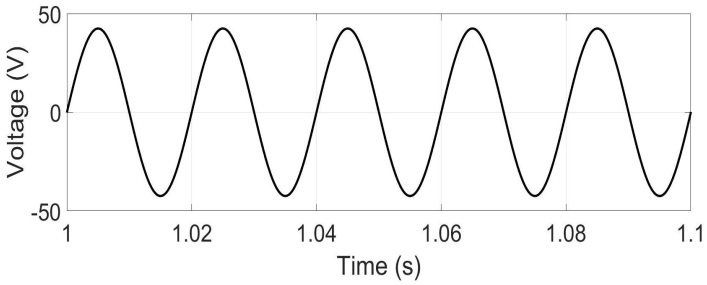
The system is designed using MATLAB/Simulink and Xilinx System Generator. A Programmable voltage source is used to simulate grid voltage and rectifier connected RL load forms the non-linear load. The reference voltage for PI controller is taken as 60V. The specifications of the various components used are shown in Table *I*

TABLE I: Specifications of Components

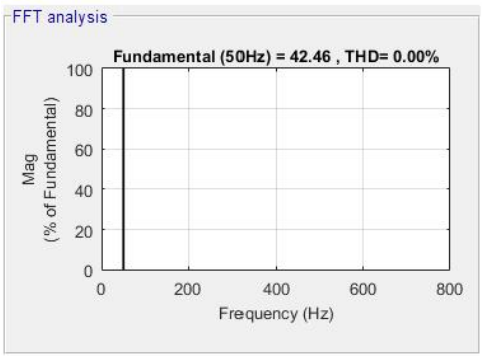
Components	Description
Source	Single phase AC source, 30Vrms, 50Hz
RL load	5Ω, 30mH
Capacitor	2 capacitors of 4.7nF
FPGA	ZedBoard [Xilinx Zynq-7000 all programmable SoC(APSoC)]

A. Simulation Results

1) Steady State Analysis with ideal source: In this case, the system is tested under non-distorted voltage source and constant load. The waveform and the THD of the source voltage is shown in Fig *6a* and Fig *6b* respectively.



(a) Waveform

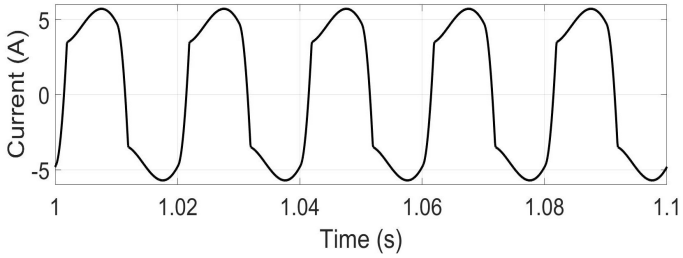


(b) THD

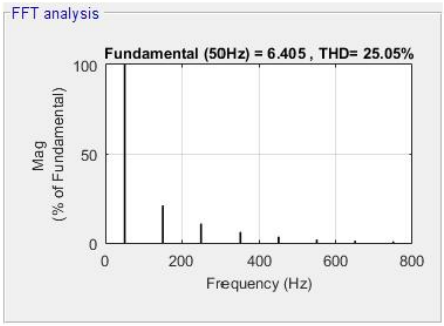
Fig. 6: Ideal source voltage u_s

The load current is non-linear as shown in Fig *7a*. The THD of the load current is 25.05% as shown in Fig *7b*. If compensation is not done, the source current is same as distorted load current. Due to SAPF, harmonics are reduced

to a THD of 3.76% which comply with the IEEE-519 [11]. Source current is shown in Fig *8a* and THD is shown in Fig *8b*. Compensation current is the current injected by the SAPF in the grid as shown in Fig *9*. The voltage across the capacitor is shown in Fig *10*. It can be observed that u_{dc} settles down to 60V.

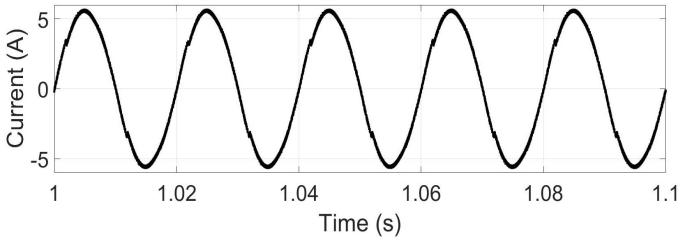


(a) Waveform

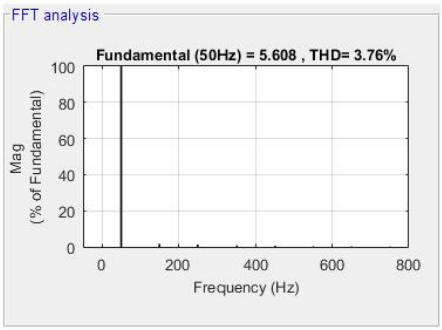


(b) THD

Fig. 7: Load current i_l for ideal source voltage



(a) Waveform



(b) THD

Fig. 8: Source current i_s for ideal source voltage

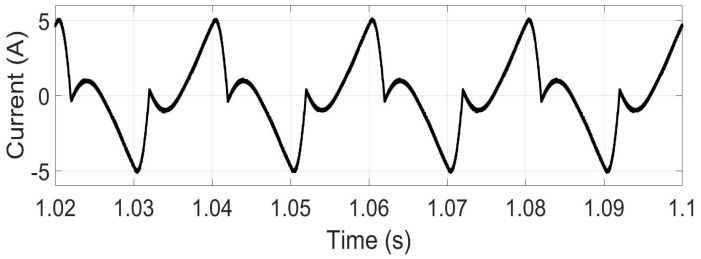


Fig. 9: Compensation current i_c for ideal source voltage

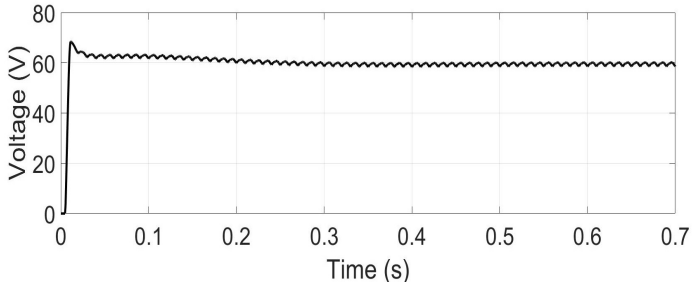
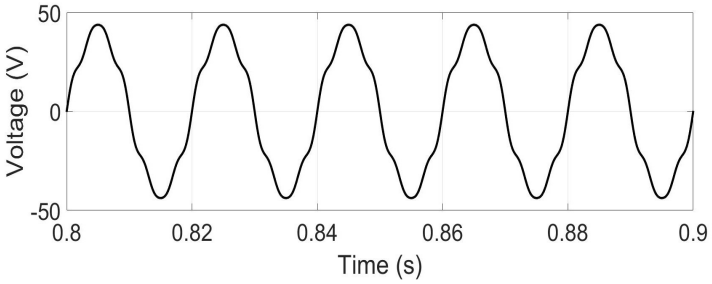
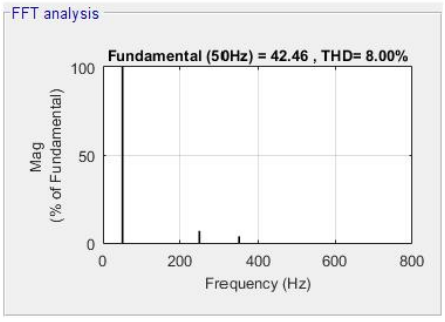


Fig. 10: Voltage across capacitor (u_{dc}) for ideal source voltage

2) Steady State Analysis with distorted source: The distorted voltage source of 8% THD (7% of the fifth harmonic and 3.87% of the seventh harmonic) is used and is shown in Fig *11a*. The THD of the source voltage is shown in Fig *11b*.



(a) Waveform

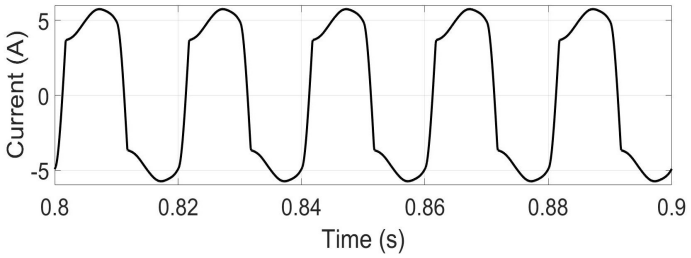


(b) THD

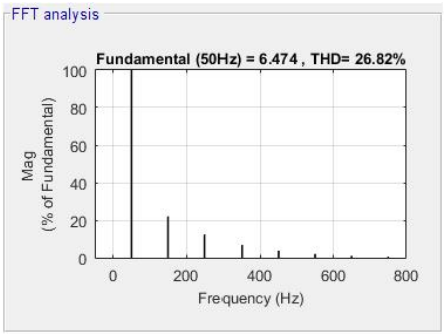
Fig. 11: Source voltage u_s with 8% harmonics

The waveform and the THD of load current and source current are shown in Fig *12a*, Fig *12b*, Fig *13a* and Fig

13b respectively. The THD of the load current is 26.82% and source current has THD of 3.91%. The waveform of compensation current is shown in Fig *14*. The voltage across the capacitor settles down to 60V as shown in Fig *15*.

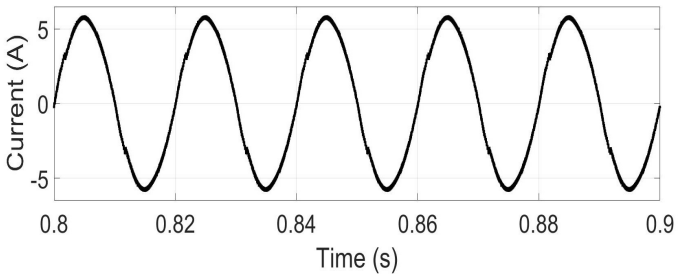


(a) Waveform

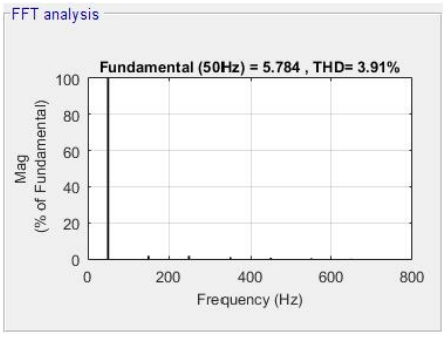


(b) THD

Fig. 12: Load current i_l for 8% harmonics in source



(a) Waveform



(b) THD

Fig. 13: Source current i_s for 8% harmonics in source

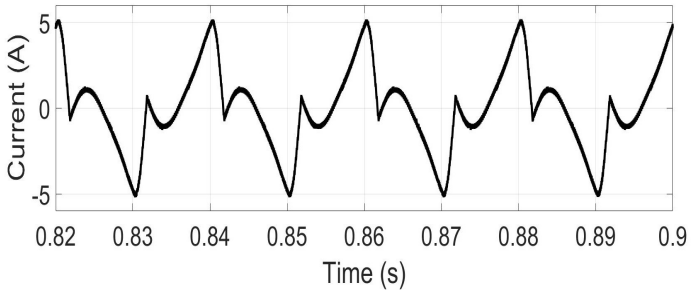


Fig. 14: Compensation current i_c for 8% harmonics in source

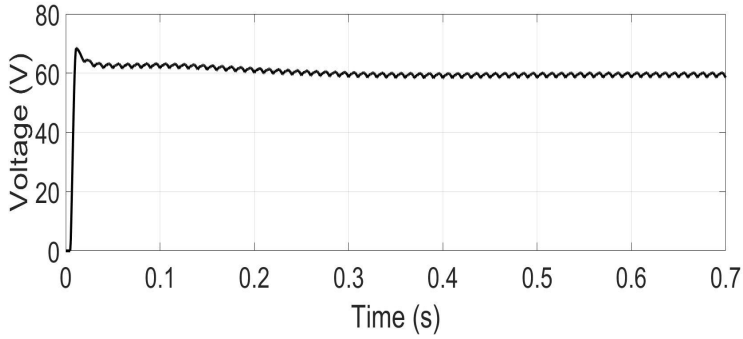
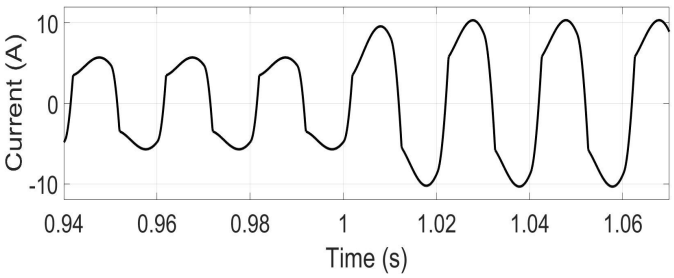


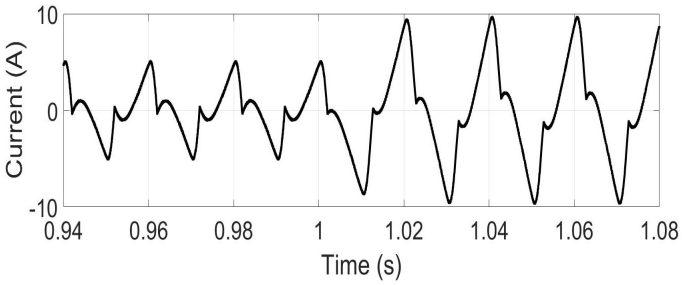
Fig. 15: Voltage across capacitor (u_{dc}) for 8% harmonics in source

3) Dynamic analysis with ideal source: At 1s, when the load is decreased by 50%, the load current, the compensation current and the source current are shown in Fig *16a*, Fig *16b* and Fig *16c* respectively. It can be observed that as the load is decreased, the load current, the compensation current and the source current are increased by 100%. The voltage across capacitor changes at 1s due to the system dynamics, but it settles down to 60V after 2-3 cycles as shown in Fig *16d*.

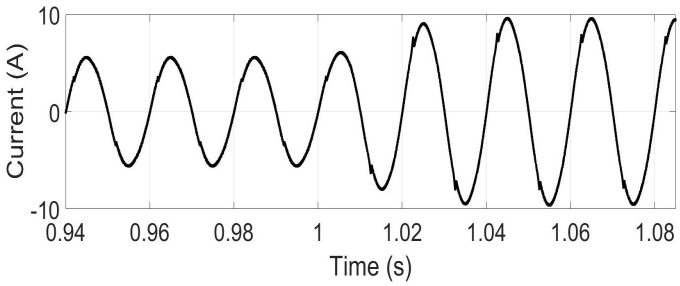
At 0.5s, when the load is increased by 100%, the load current, the compensation current and the source current are shown in Fig *17a*, *17b* and Fig *17c* respectively. As the load is increased, the load current, the compensation current and the source current are decreased by 50%. The voltage across capacitor changes at 0.5s due to the system dynamics, but it settles down to 60V after 2-3 cycles as shown in Fig *17d*.



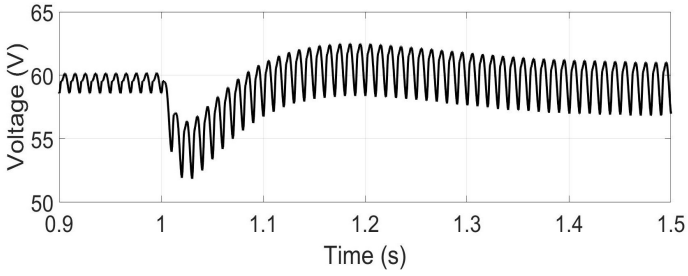
(a) Load current i_l



(b) Compensation current i_c

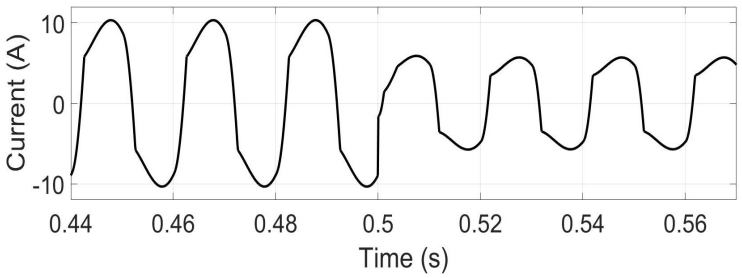


(c) Source current i_s

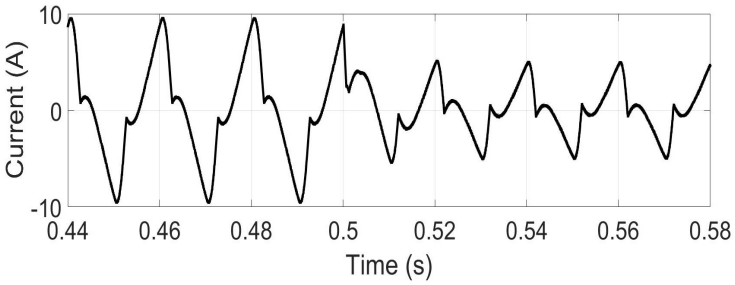


(d) Voltage across capacitor (u_{dc})

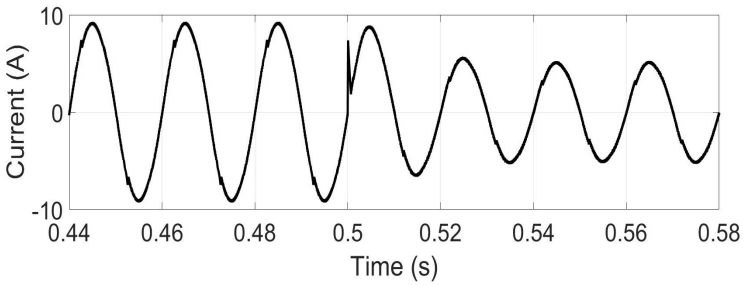
Fig. 16: Results for decrease in load



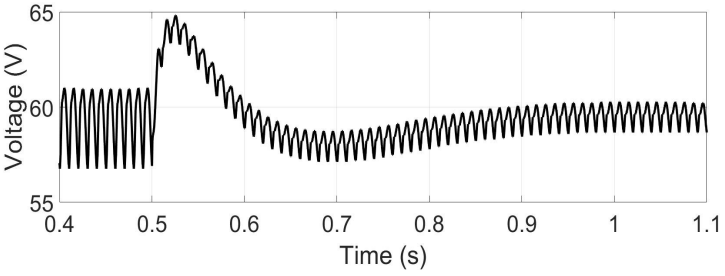
(a) Load current i_l



(b) Compensation current i_c



(c) Source current i_s



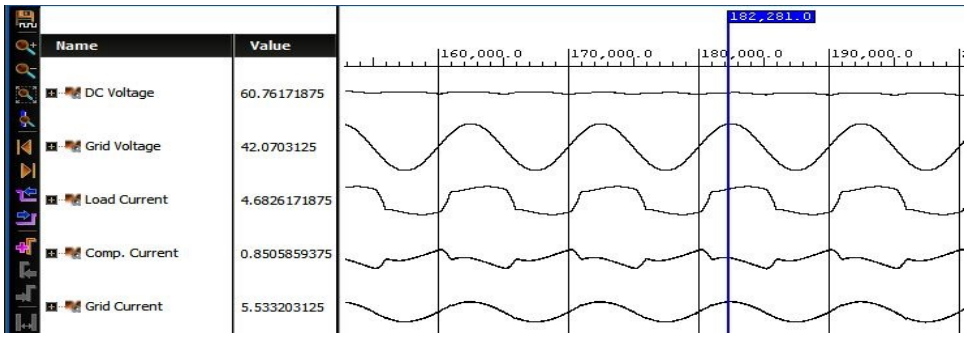
(d) Voltage across capacitor (u_{dc})

Fig. 17: Results for increase in load

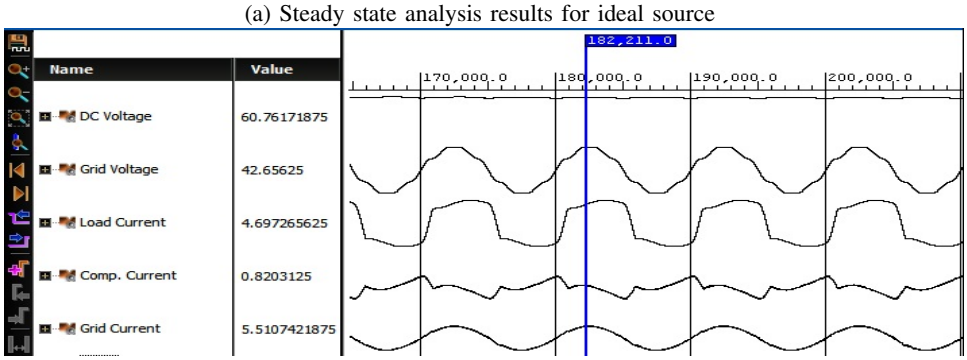
B. Hardware Co-simulation Results

In hardware co-simulation, the controller is implemented using FPGA and power circuit is implemented in MATLAB and the results are analyzed. Hardware co-simulation was performed using Zedboard FPGA with the help of the Xilinx System Generator. The waveforms obtained for steady state ideal grid voltage conditions are shown in Fig *18a.* DC link voltage, grid voltage, load current, compensation current and grid current can be seen in the figure. Fig *18b* shows DC link voltage, grid voltage, load current, compensation current and grid current under distorted grid conditions (8% harmonics). The waveforms obtained for ideal grid voltage and dynamic decrease (50%) in the load are shown in Fig *18c.* The figure shows DC link voltage, grid voltage, load current, compensation current and grid current. The waveforms obtained for ideal grid voltage and dynamic increase (50%) in load are shown in Fig *18d.* In the figure, DC link voltage, grid voltage, load current, compensation current and grid current can be observed.

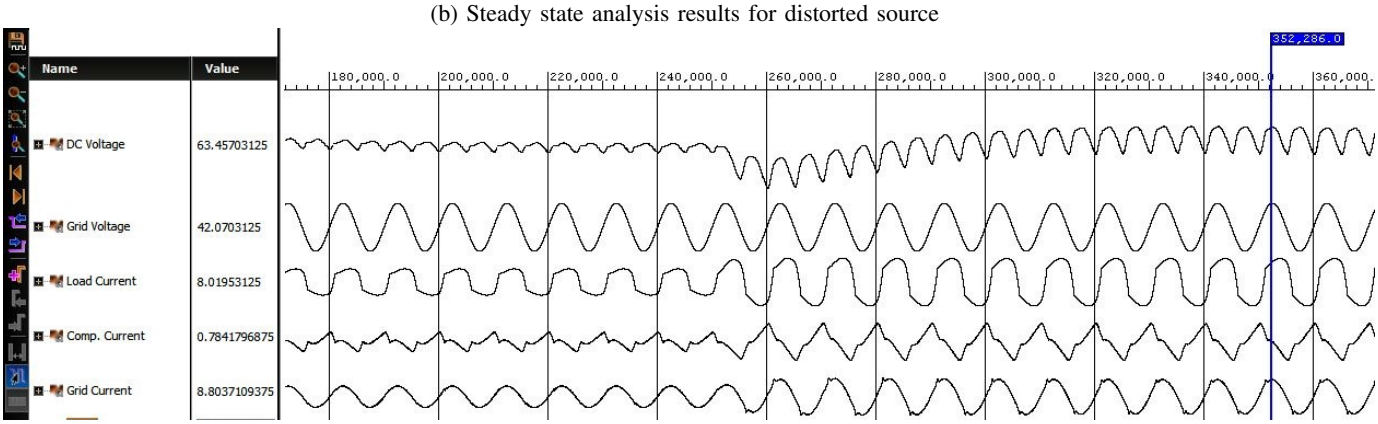
For all the above cases, it can be observed that the results obtained from hardware co-simulation are same as that of MATLAB simulation results.



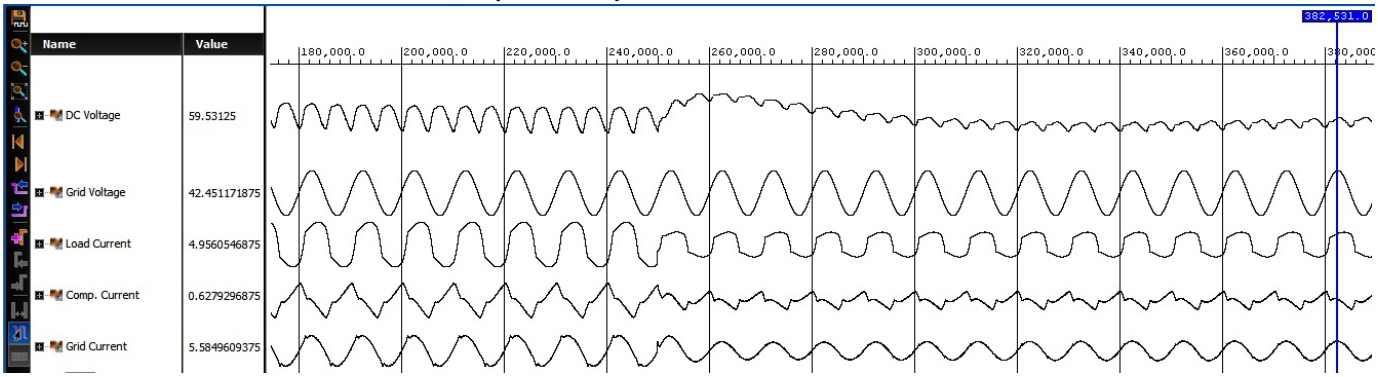
(a) Steady state analysis results for ideal source



(b) Steady state analysis results for distorted source



(c) Dynamic analysis results for decrease in load



(d) Dynamic analysis results for increase in load

Fig. 18: Hardware Co-simulation results

V. Conclusion

The use of dual STF based SAPF helps to mitigate harmonics in single phase circuits with non-linear loads. Reactive power required by the nonlinear load is completely compensated by SAPF and power factor at source end becomes almost unity. THD of source current is reduced to less than 5% by using SAPF. DC link voltage is maintained constant irrespective of load changes and source distortions. So, it can be concluded that dual STF based controller for SAPF is efficient and it overcomes the drawbacks of classical pq method.

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