

Development of DSP Based High Speed Numerical Distance Relay and its Evaluation Using Hardware in Loop Power System Simulator

Sham M V and Dr. K P Vittal, *Member, IEEE*

Department of Electrical and Electronics Engineering, National Institute of Technology Karnataka, Surathkal, Mangalore, India

Abstract—Numerical distance relays are used for the protection of long transmission lines. These relays require specialized hardware for high speed signal acquisition and computation of relaying quantities. The digital signal controller (DSC) and the data converters used in the relay have a major influence on the performance of the relay. In order to achieve high reliability and to reduce the size of the relay, it is desirable to use minimum hardware components. The newly arrived DSC and special range of data converters are offering optimal hardware solutions. This paper presents design and developments of distance relay hardware based on DSC TMS320F28335 and ADS8556 a simultaneous sampling type analog to digital converter (ADC), both from Texas Instruments. The distance relay designed using above hardware is evaluated through hardware in the loop (HIL) experimental setup. The fault transient signals are obtained from EMTDC/PSCAD considering a typical 220KV transmission line and these signals in turn are injected to the proposed relay through Doble F6150 power system simulator to perform elaborate dynamic tests.

Index Terms— Digital Signal Controllers, EMTDC/PSACD, power system simulator, Numerical Distance Relay

I. INTRODUCTION

Distance relays are widely used for the protection of transmission lines by measuring the impedance between the relay installation point and the fault location. Since the impedance of the transmission line per kilometre remains almost constant throughout the length of the transmission line, the impedance measured by the relay is proportional to the distance to fault on the line. Distance relays provide an excellent way of obtaining zone discrimination, selectivity, and speed of operation by ensuring precision trip decision up to a certain range of distance [1-3]. The advancements in digital technology have given birth to numerical distance relays and has gained wide acceptance in power utilities. These relays being programmable use both hardware and software components. The hardware mainly consists of signal

conditioning circuits, DSC and ADC modules. The accuracy and operating speed of the relay depends greatly upon these modules. Further, the Distance relaying algorithms demand considerable computation power. Therefore, a floating point processor will be preferred over a fixed point processor for achieving higher accuracy and faster computations. In a numerical protection relay, the dynamic range of the input signal is often very high. It is also expected that the relay maintain its measurement accuracy across the entire input range. For distance relay application, the phase relationship between the signals sampled from different channels is as important as the value of the signal to measure the impedance accurately. Therefore, a simultaneous sampling bipolar ADC is required in these applications [4].

The objective of the reported work here is to highlight the merits of hardware development and outcome of performance evaluation of a distance relay built using a 32 bit floating point digital signal processor TMS320F28335 and a six channel simultaneous sampling analog to digital converter ADS8556, which has $\pm 12\text{v}$ input voltage range. The DSP programming for generating the control signals required for data acquisition system and implementation of the distance relaying algorithm are explained. To demonstrate the working of the newly developed relay hardware, a 220 KV two source power system connected by a 180 kilometre transmission line is modelled using PSCAD/EMTDC [10]. All types of faults are applied at various lengths of the transmission line and fault samples data files are created in COMTRADE (Standard defines a common format for the exchange of electrical power system transient data) format. The COMTRADE files are loaded onto DOBLE F6150 power system simulator, which produces the test signal waveforms in real time. These signals are applied to the numerical distance relay hardware and the trip signal output of the relay is monitored continuously, which is known as hardware in the loop testing.

The paper is organized as follows. Section II presents Numerical distance relay hardware development. The development of relay software including the relaying algorithm, fault detection logic implementation along with the

simultaneous sampling of all six channels. The second trace is the end of conversion (EOC) signal issued by analog to digital converter to indicate that the conversion over and the data is ready to read. The time taken by the ADC to convert all six channels is about 1.17micro seconds. The read pulses, as specified in the device datasheet are generated to read digitized data of all six channels and it is shown by the third trace of Fig.3. Channel A will be read, each time the read pulse makes transition from high to low [5]. The digitized output of the ADS8556 over its entire operating range is tested and tabulated in the Table 1.

Table 1 Digitized output of the ADS8556

Input voltage(volts)	Hex output code
10	7FFF
5	3FFF
0+	0000
0-	FFFF
-5	C000
-10	8000

III. SOFTWARE DEVELOPMENT OF NUMERICAL DISTANCE RELAY

The software for the numerical distance relay is developed in embedded C language. For this purpose Code composer studio4 (CCS4)[®] is used as a development tool. The CCS4 provides easy debugging and real time refreshing capabilities.

On boot up all the interrupts are disabled, multiplexed I/O pins are programmed as general purpose I/O pins, watchdog timer is disabled and the CPU clock is set to 150MHz by setting PLL multiplier equal to 5. CpuTimer0 is used to generate the start of conversion signal of 3200Hz with 50% duty cycle. Therefore, SOC is applied to all six channels at every 0.3125 milliseconds. The input signals are simultaneously sampled and held by the respective sample and hold circuits. Then all six channels will be converted simultaneously. During the conversion period busy signal (EOC) will remain high and becomes low after conversion is finished. So, the busy signal is used as an interrupt signal to the DSC. After receiving the interrupt DSC will jump to the ADC interrupt service routine. The whole process of processor initialization is shown in form of a flow chart in Fig.4.

Fig.5. shows the flow chart of the ADC interrupt service routine. The ADC interrupt service routine is used to perform the below mentioned functions.

- a) To read the ADS8556 output and store the data into respective sample tables.
- b) Compute the real and imaginary parts of fundamental component of all voltage and current signals using recursive full cycle window algorithm.
- c) Compute zero sequence current.
- d) Calculate all phase to ground and phase to phase impedances.
- e) Fault detection using Mho relay characteristics.
- f) Determine the type of fault.

After reading all the channels magnitude and phase of the three phase voltages and current are calculated using the full cycle window algorithm. The Full cycle window Fourier algorithm is used in recursive [6] mode for saving computation time by using following equations

$$x_c^{w+1} = x_c^w + (x_{w+N} - x_w) \cos\left(\frac{2\pi}{N}w\right) \quad (1)$$

$$x_s^{w+1} = x_s^w + (x_{w+N} - x_w) \sin\left(\frac{2\pi}{N}w\right) \quad (2)$$

Where,

X_c = Real part of the fundamental component

X_s =Imaginary part of the fundamental component

N =Number of samples per cycle.

X_k = K^{th} sample

W = Current window

The zero sequence current is computed using the three phase currents. The zero sequence current is used as discriminator between ground faults and phase faults. In the present work mho type impedance relay is used for fault detection just as a sample case. The protection relay of this type simply calculates the apparent impedance of the line under its protection. This measured impedance from the relay to fault location is then compared with the protection reach settings. If the line impedance measured is within the relay characteristics, it will operate and issue trip signal to the circuit breaker/s of the transmission line and isolate it from the rest of the connected system. The total execution time or distance relay logic program is 78 micro seconds, which can be observed from the trace D2 (TIME) of Fig.6.

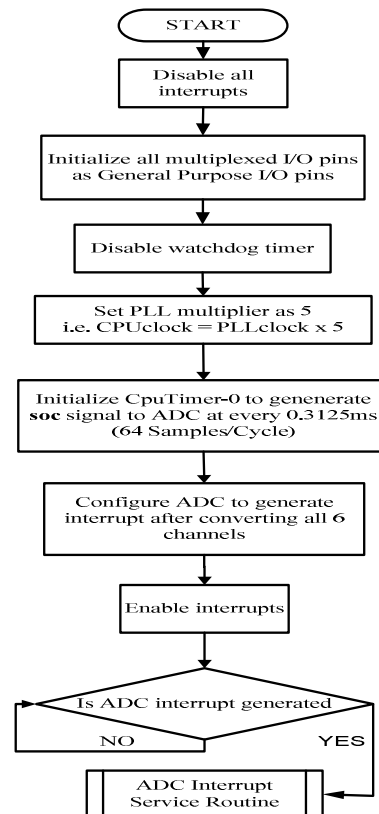


Fig. 4. Processor initialization for implementing numerical distance relay

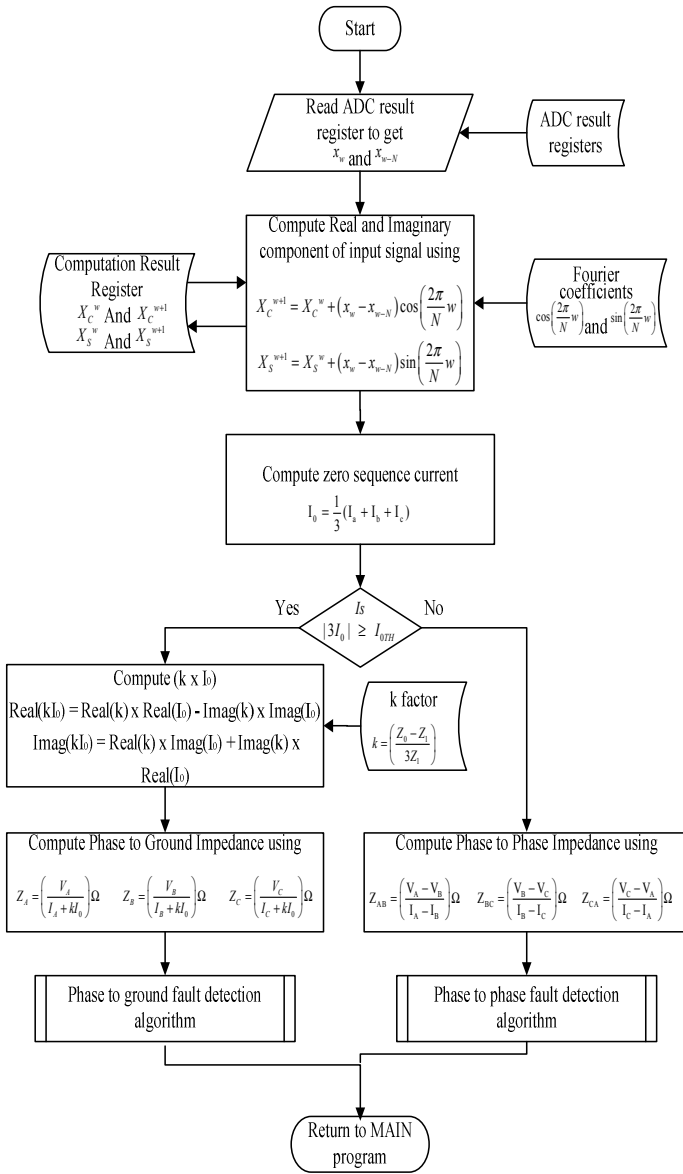


Fig. 5. ADC interrupt service subroutine

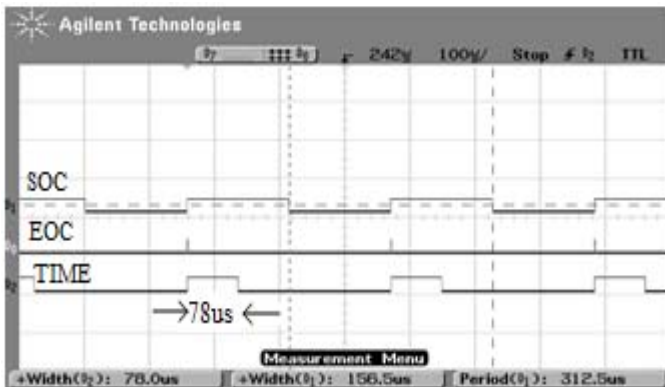


Fig. 6. Execution time of the distance relay

IV. FAULT TRANSIENT SIGNAL SIMULATION AND DISTANCE RELAY MODELLING IN PSCAD

The single line diagram of the model power system selected for simulation is as shown in Fig. 7.

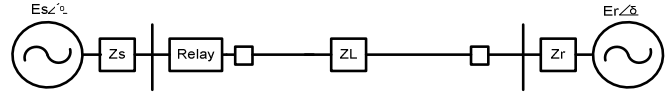


Fig. 7. power system model selected for simulation

The power system consist of two 220 KV Thevinin equivalentv sources E_s and E_r at the sending and receiving end respectively. Two sources are connected by a 180 kilometre length transmission line. The system parameters are given in the appendix. The power system is simulated for all types of fault conditions along the different lengths of the transmission line. The voltage and current signals obtained at the relay point are sampled at the rate of 64 samples per cycle. The simulation study is extended to implement the modeling distance relay also. As a part of relay function, the magnitude and phase of the fundamental component of all phase voltages and currents are extracted using the FFT block available in the EMTDC/PSCAD software. The ground and phase impedances are calculated using the formula listed in the Table 2. Both the real and imaginary parts of the compensation factor (K) is considered for the impedance calculation of line to ground units [7]. A mho relay characteristic is used to detect the fault. The first zone of the relay is set to protect 85% of the line. PSCAD simulation results for a phase A to phase B fault at 100KM of the transmission line is presented to verify the relay model. Fig. 8 shows the impedance trajectory of the AB fault at 100 KM. Fig.9 shows the time taken by the simulated distance relay to issue the trip signal. It can be seen from the figure that trip signal is issued after 11.80 milliseconds from the fault initiation. Operating times can vary with fault current, with fault position relative to the relay setting, and with the point on the voltage wave at which the fault occurs. Operating times for the fault occurring on zero and peak position of the phase A voltage waveform for AG and AB faults are tabulated in the Table 3. It can be observed from the table that the time for operation increases if the fault occurs on the peak point on the voltage waveform. Also, the operating time increases as the fault location is farther from the relay point. This validates the model of the distance relay.

Table 2 Formula for impedance calculation

Fault type	Formula
Line to ground faults	$V_x / (I_x + 3KI_0)$ Where X is faulted line K is the compensation factor $(Z_0 - Z_1) / 3Z_1$
Line – Line / Line-Line-Ground faults.	$(V_x - V_y) / (I_x - I_y)$; Where X & Y are the faulted lines
Three phase faults	V/I

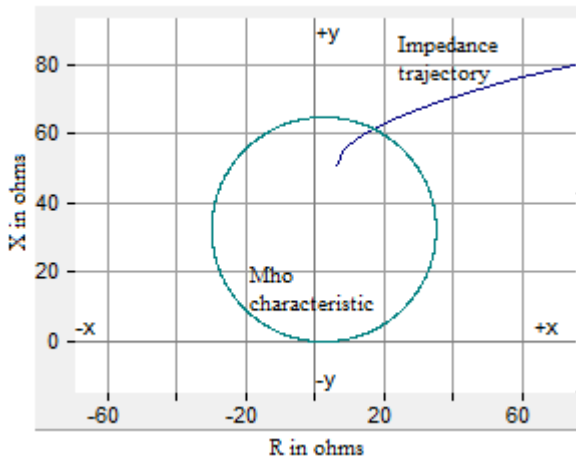


Fig. 8. Impedance trajectory for AB fault at 100KM of the line.

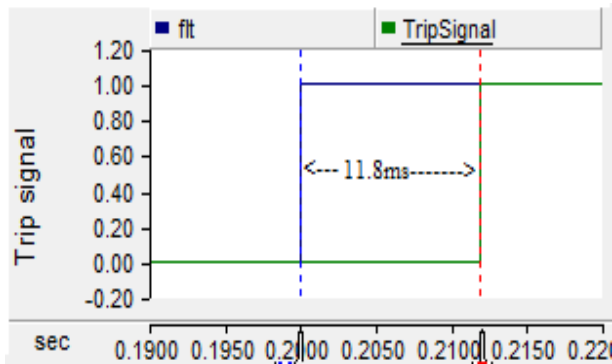


Fig. 9. Time taken to issue the trip signal for AB fault at 100KM

Table 3 Time taken to issue trip signal

Point on the phase A voltage waveform	Type of fault	Fault distance	Time to issue trip signal(ms)
Zero	AG	150	21.31
Peak	AG	150	27.00
Zero	AB	100	11.80
Peak	AB	100	15.60

V. RELAY TEST RESULTS

The newly designed DSC TMS320F28335 based relay hardware is evaluated for all types of fault at different length of the transmission line using same fault data sets used for testing software model of distance relay presented in above section. About 100 test cases have been considered to verify the performance of DSC based distance relay with relay model is PSCAD. It is found close to 100% match in performance of both. As a sample only two cases are presented with oscilloscope screen shots. The real time test signals generated by DOBLE F6150 power system simulator during line to line fault, namely A-B fault at 100 kilometers from the relay location is shown in Fig. 10. The first waveform shows the scaled fault current of phase A reproduced by the DOBLE F6150. Only one channel is shown here, as it is not possible to show all six channels simultaneously on the oscilloscope. The second waveform of the same figure is the trip signal issued by the relay. It can be seen that the relay issues the trip signal in about 11.2 milliseconds, which is approximately equal to the operating time obtained through EMTDC/PSCAD

simulation as shown in the Fig.9. Similarly for a phase A to ground (A-G) fault at 150 kilometers from the relay location is shown in the Fig. 11. It can be seen that the relay issues trip signal in about 19.6 milliseconds.

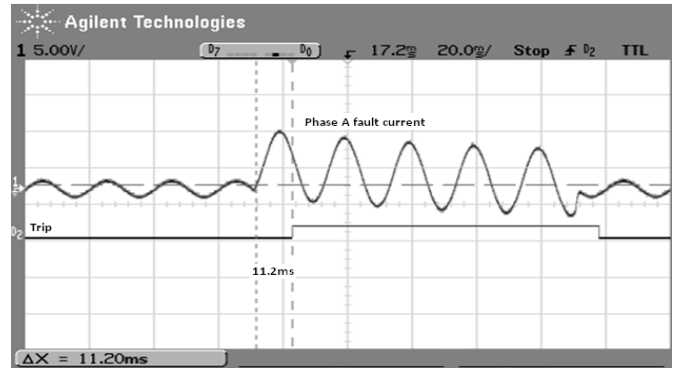


Fig. 10. Fault current waveform and the trip signal issued by the distance relay for AB fault at 100KM.

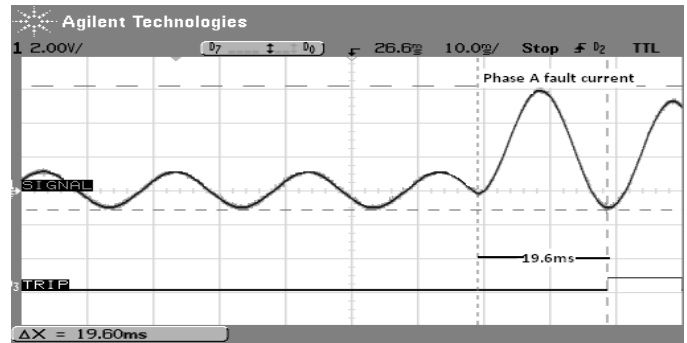


Fig. 11. Fault current waveform and the trip signal issued by the distance relay for AG fault at 150KM.

The photographic view of the experimental setup used for carrying out the present work is as shown in the Fig. 12.



Fig. 12. Photograph of the Experimental setup

VI. CONCLUSION

Numerical distance relay hardware is built using newly available DSC TMS320F28335 and ADS8556 devices from Texas Instruments to explore possibility of enhancing the operating speed of the relay and to incorporate more functionality in future development work. The Relay hardware developed as a part of research work is tested using the hardware in the loop method using DOBLE F6150 power

system simulator. It is found that the combinations of these new devices like DSC TMS320F28335 and simultaneous conversion type ADC ADS8556, eliminates the need of external hardware such as sample and hold circuits, reference signal generators etc. This provides a convenient platform for developing a high speed and modular numerical protection relays, which are more reliable due to reduced hardware components.

APPENDIX

Table A.1: Simulated power system parameters

Equivalent Voltage Sources	
Base Voltage	220 KV
Source impedance Z_s	$26.45 \angle 80^\circ \Omega$
Source impedance Z_r	$26.45 \angle 80^\circ \Omega$
Load angle δ	20°
Frequency	50 Hz
Transmission Line	
Resistance	0.03467 Ohms/KM
Series Reactance	0.42336 Ohms/KM
Line Length	180 KM

REFERENCES

- [1] Badri, Vishwakarma, Ram. D. "Power System Protection and Switchgear", Tata McGraw Hill ,2007.
- [2] Stanely H. Horowitz, Arun G. Phadke, "Power System Relaying", John Wiley & Sons, May 2009.
- [3] J.LewisBlackburn, Thomas J. Domin, "Protective Relaying: Principles and Applications", CRC press, 2006.
- [4] A Numerical protection relay solution, Texas instruments, September. 2010.
- [5] 16-,14-,12-Bit ,Six Channel, simultaneous sampling analog to digital converters, Texas instruments , August 2009.
- [6] Hatem A. Darwish and Magdy Fikri, "Practical considerations for recursive DFT Implementation in Numerical Relays", IEEE Transactions on Power Delivery, VOL:22, Issue:1, JANUARY. 2007, Pages:42-49
- [7] M. Sanaye-Pasand, H. Seyedi, "Simulation, analysis and setting of distance relays on double circuit transmission lines". Australasian Universities Power Engineering Conference, AUPEC, September. 2003, pages:177-183.
- [8] C2833x/C2823x C/C++ Header Files and Peripheral Examples Quick Start, Texas instruments ,June 28, 2010.
- [9] TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232, Digital Signal Controllers (DSCs), Texas instruments ,March 2011.
- [10] PSCAD/EMTDC User's Manual: Ver.4.2, Manitoba HVDC Research Centre, 2005.
- [11] Transwin 3.3 User's guide, Doble engineering company, September. 2010