Fast Startup Crystal Oscillator Design

Puneeth Kumar and Rekha S.
Department of Electronics and Communication
National Institute of Technology Karnataka
Surathkal, Mangalore-575025, India.
puneeth@hotmail.com, rsbhat_99@yahoo.com

***Abstract*—Generating the clock that is reliable, accurate and available as soon as the power is up is very essential for any application that requires the time base reference. For generating these clocks, crystal oscillator is a very good option. But usually the crystal oscillator circuit suffers from slow startup. Therefore, it is essential to improve the startup time with optimally controlled crystal drive such that crystal drive power rating is not compromised. We propose a method that discusses about increasing the negative resistance during startup using a startup circuit for fast start. Once the reliable startup is achieved, the startup circuit is disconnected for lower negative resistance in stable operation mode. In the 32768 Hz real time clock generating oscillator, the startup time can be improved from 330 ms to 220 ms using the conventional startup method. With the proposed method, lesser startup time of 160 ms is achieved.**

***Keywords*—Crystal oscillator; Startup circuit; Stable Clock generator; Gm-stage.**

I. Introduction

Electronic systems especially in low-power Micro Controller Unit (MCU) and watch systems needs clocks with frequency accurate and stable. Accurate frequency generation circuits consume lot of power, a concern in battery operated portable devices. Accurate clock available as soon as powered up will reduce the wait time in MCU units for Real Time Clocks (RTC). In the sensor/transceiver application, if the transmission message is preceded with a header of a specified length, then it is possible to turn on the receiver periodically to detect a transmission and not miss the transmitted data. The faster the system can be powered up, performs its function and powers down, the lesser is the power that is needed.

Crystal oscillators are used in systems that require a very stable clock reference. As they are inherently stable, they take both time and energy to start oscillating. For time reference in real time clock applications where accuracy is most important, crystal oscillator is the the most suited circuit [1]. If the integrated circuit requires a crystal oscillator circuit, which most do, then the ability to quickly start the crystal to produce a valid stable clock signal is very important without compromising on power dissipation in crystal. Therefore, it is required to address the trade-off between the fast startup and crystal power and reliability.

There are different methods to speed up the clock start by injecting the noise/signal, starting the clock in sync with another ring oscillator [2], [3]. These methods need extra circuit to generate the clocks. Also these methods can start the clock fast, but may not ensure the stable clock output. Power dissipation can be reduced by providing reduced power supply to the oscillator core [4], [5]. The crystal power dissipation is very important factor in determining the stability and reliability of the oscillator. Most of the time, power dissipation is limited by external resistor in series with crystal. This external resistor drop reduces the voltage across the crystal. But, this requires extra resistor and also may contribute to failure in some corners. In [6], author proposes a startup improvement method with periodically switching off the amplifier to avoid the saturation. With the saturation of oscillation, the stored energy in the crystal's equivalent inductor and capacitor is saturated. After the saturation, if the amplifier is disabled, the oscillation will start decaying; and if we enable it again, it will start growing again. Fast startup can also be achieved with large currents [7], [8] thereby affecting the transconductance. But for normal operation, these currents have to be reduced later to control the power dissipation.

In this paper, a novel method has been proposed to get fast startup by increasing the negative resistance across the crystal terminals. The amount of negative resistance to be increased and the time to which it has to be kept active, will decide the startup time and also the crystal drive. The control is based on the number of clock cycles generated. To avoid the crystal over-drive, a digital feedback circuit is designed to control the startup, based on optimized crystal drive voltage. Rest of the paper is organized as follows. Section II describes the basics of the crystal oscillator circuit and the negative resistance. Crystal Oscillator model is explained in section III. Design of the circuit is proposed in Section IV. Results are discussed in section V. Section VI concludes the paper.

II. Crystal oscillator basics

The principle behind any oscillator is a positive feedback loop satisfying the Barkhausen criterion. In the case of crystal oscillator, accuracy of the generated clock depends on the reference element used. For oscillator's basic reference element there are number of crystalline materials available. But Quartz has many characteristics such as good mechanical strength, less variation of size and shape with temperature etc., hence it is most widely and commercially used crystalline element. Figure 1 shows the simplified electrical equivalent model that describes the quartz crystal, where C_O is the shunt capacitance, L_M is motional inductance, C_M is motional capacitance and R_M is the motional resistance some times referred to as Equivalent Series Resistance (ESR).

The oscillator block diagram shown in Figure 2 is a general architecture usually found in Integrated oscillators in MCUs. The architecture shown is of the pierce oscillator.

Bias generator generates the reference current and voltage. Gm-stage is the negative resistance generator along with

978-1-5386-1887-5/17/$31.00

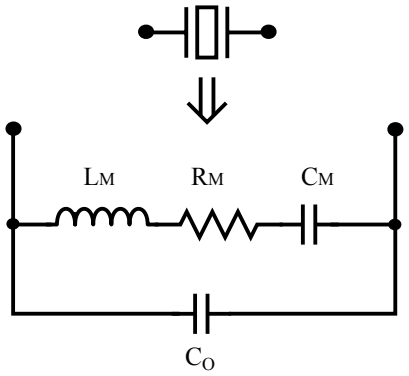

Fig. 1: Quartz crystal electrical model.

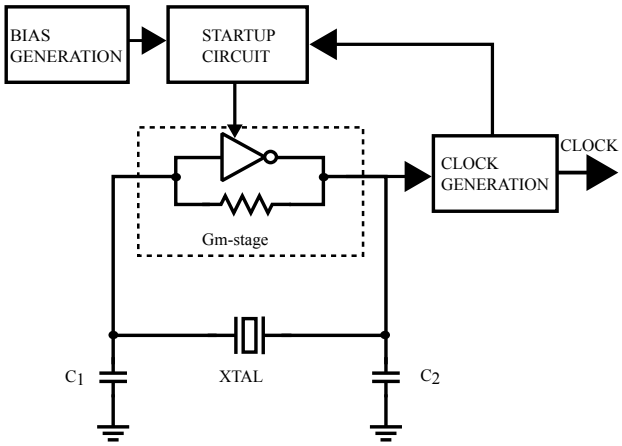

Fig. 2: Block diagram of the oscillator.

parallel capacitors across the crystal. The resistance shown across the inverting amplifier is a large resistance used for biasing the inverting amplifier. The gain stage can be a single transistor (MOSFET or BJT) or in integrated circuits it could be an inverter. Voltage buildup at the output of the Gm-stage is sinusoidal in nature. To use it as a clock in digital circuits, it is required to convert it into full logic swing. Clock generation circuit does this function.

Startup circuit is used for reducing the crystal clock generation and stabilization time. There are many types of startup circuits that are being used. Usually the startup circuit is switched off to save power after a predefined number of clocks are generated or stable clock is obtained.

A. Negative Resistance

To obtain the stable oscillation, there should be balance between the reference element and rest of the oscillator circuit. As shown in Figure 2, the oscillator circuit consists of a transconductance stage. To find the impedance presented to the reference element by the oscillator, the circuit can be replaced by a small signal current source as shown in Figure 3. The detailed small signal analysis is explained in the next section. Figure 3 shows the setup for negative resistance analysis. Z_{IN} is the impedance presented to the reference element by C_1, C_2, and the inverter. It is the effective series combination of the capacitors in series with inverter amplifier. Choosing

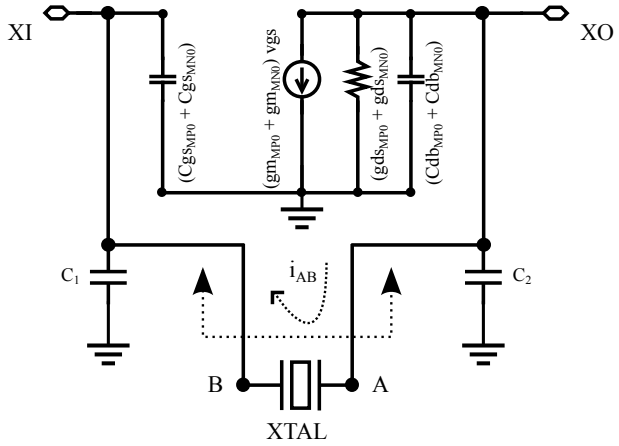

Fig. 3: Pierce oscillator negative resistance analysis.

an appropriate C_1 and C_2 value from crystal datasheet will set the crystal's load capacitance. This will set the negative resistance part which is independent of the Gm-stage gain. This analysis suggests that an arbitrary negative resistance can be synthesized for an oscillator using the appropriate transfer characteristic and capacitor values [9].

$$Z_{IN} = \frac{V}{I} = \frac{V_{AB}}{I_{AB}} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_1} - \frac{g_m}{\omega^2 C_1 C_2} \quad (1)$$

$$\text{Negative resistance}(R_N) = -\frac{g_m}{\omega^2 C_1 C_2} = -g_m X_{C1} X_{C2} \quad (2)$$

The negative resistance can be modeled as shown in Figure 4.

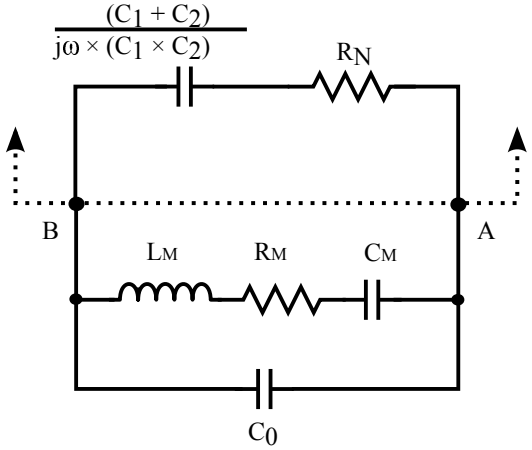

Fig. 4: Crystal oscillator negative resistance model.

B. Startup time

The requirement for startup time varies from system to system based on how the clock is used. For microprocessor the clock should be available as soon as the initial power is applied and startup time is the time to achieve the sustained clock from power up. In phase locked loop circuit the clock should be not only sustained but it should be within the defined accuracy. The startup time of a crystal oscillator is determined

by the noise or transient conditions at turn on, small signal envelope expansion due to negative resistance and large signal final amplitude limiting [10].

The envelope expansion is only a function of total negative resistance and the motional inductance of the crystal. As shown in Figure 4, the simplified equivalent series RLC circuit contains the motional inductance (L_M), the sum of the applied negative resistance of the oscillator and the motional resistance of the crystal (R_S) and the effective series capacitance of the entire network dominated by the motional capacitance (C_M). The equation of the un-driven network model of the crystal (refer Figure 4) can be written as below [10].

$$s \times L_M + R_S + \frac{1}{s \times C_M} = 0 \tag{3}$$

Solving this equation, we can see that, as the net resistance R_S is negative, the poles lie in the right half of the s-plane. The resulting time domain solution for the differential equation can be written as in Equation 4.

$$V(t) = K_i \times \left[e^{\left(-\frac{R_S}{2L_M}\right) \times t} \right] \times sin\left[2\pi t \sqrt{\frac{1}{L_M C_M}} + \phi_i \right] \tag{4}$$

where K_i is a constant and ϕ_i is an arbitrary phase, both related to the initial startup conditions. The exponential expansion is valid only for small signal conditions as the power available to the circuit is limited.

The time constant of the envelope expansion is proportional to the startup time of the oscillator given by

$$\tau = -\frac{2L_M}{R_S} = -\frac{2L_M}{(R_M + R_N)} \approx \frac{2L_M}{|R_N|} \tag{5}$$

Since $|R_N| >> |R_M|$

The time constant for envelope expansion is positive. It is inversely proportional to the net negative resistance of the oscillator and the motional resistance. Also directly proportional to the motional inductance. Due to the large motional inductance of crystals and the limited net negative resistance, crystal oscillators have long startup times.

C. Crystal drive level

The drive level of a crystal refers to the power dissipated in the crystal. The maximum drive level of a crystal is often specified in the data sheet of the crystal in μW. Drive level is the maximum power the crystal can handle where all the electrical parameters are guaranteed. Drive level of the crystal is given by

$$\text{DL} = R_M \times 2 \times \left(\pi f_{XTAL} \left(C_M + C_L\right) V_{pp}\right)^2 \tag{6}$$

Where,
C_L is load capacitance for the specified crystal frequency ($C_L = C_1 = C_2$).
f_{XTAL} is crystal oscillator parallel resonance frequency.
V_{pp} is peak to peak voltage across the crystal.

Drive level is defined in crystal datasheet to avoid number of problems such as high EM emission, reliability issues like physical damage to the crystal, attempting to start at an overtone or failing to start at all etc. It also affects the thermal stability and premature aging in crystal.

III. System Model

As shown in Figure 2, Gm-stage is the negative resistance generator along with parallel capacitors at terminals XI and XO, across which crystal is connected. As shown in detailed Figure 5, CMOS transistors MP0 and MN0 are connected in inverter configuration and forms the inverting gain stage. The resistance Rb shown across the inverting amplifier is a large resistance used for biasing the inverting amplifier. C_1 and C_2 are the load capacitance of crystal also referred as C_L in crystal datasheet.

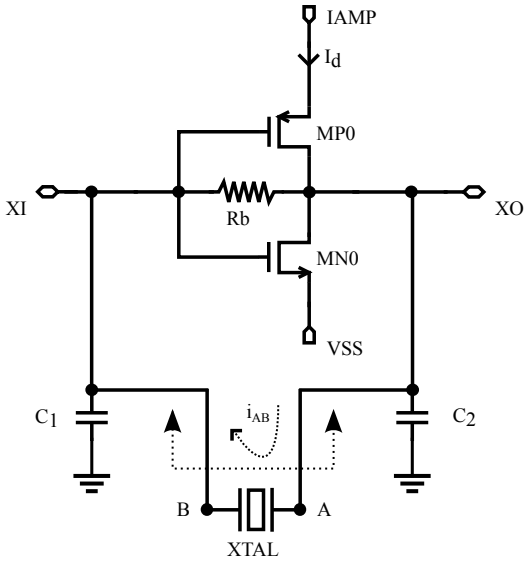

Fig. 5: Core amplifier circuit

A. Small signal Analysis

Small signal analysis [11] of the circuit gives the gain equation of the amplifier as in Equation 7.

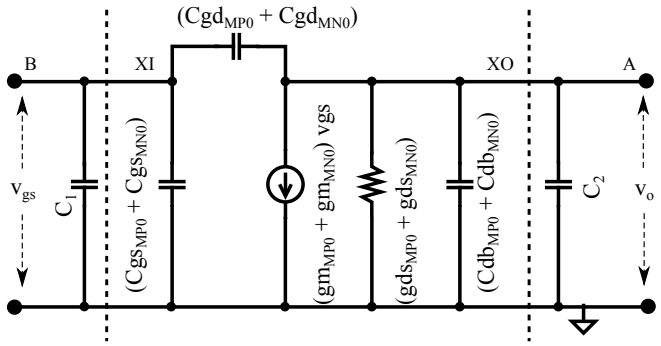

Fig. 6: Small signal model of amplifier

$$A = A_0 \left[\frac{1 - \frac{s}{z}}{1 + \frac{s}{p}} \right] \tag{7}$$

At the frequency of interest, the impedance of Cgd and Cdb capacitors of the devices are very large compared to the impedance offered by C_L. Hence,

$$A_0 = -\left(gm_{MP0} + gm_{MN0}\right) R_0$$

$$R_0 = \frac{1}{(gds_{MP0} + gds_{MN0})}$$

$$z = \frac{(gm_{MP0} + gm_{MN0})}{(Cgd_{MP0} + Cgd_{MN0})}$$

$$C_0 = (Cgd_{MP0} + Cgd_{MN0} + Cdb_{MP0} + Cdb_{MP0} + C_L)$$

$$p = -\frac{(gds_{MP0} + gds_{MN0})}{(Cgd_{MP0} + Cgd_{MN0} + Cdb_{MP0} + Cdb_{MP0} + C_L)}$$

$$= -\frac{1}{R_0 C_0} \approx -\frac{(gds_{MP0} + gds_{MN0})}{C_L}$$

Zero occurs at very high frequency, hence it is a single pole system in the region of interest. Gain Bandwidth product (GB) is a constant and is given by the following.

$$GB = A_0 \times p$$

$$= \left(-\left(gm_{MP0} + gm_{MN0}\right) R_0\right) \times \left(-\frac{1}{R_0 C_0}\right)$$

$$GB = \frac{(gm_{MP0} + gm_{MN0})}{C_L}$$

Gain-Bandwidth product is directly proportional to the sum of transconductance of both the transistors and inversely proportional to the load capacitance (C_L). Plots of sum of the transconductance and the gain of the amplifier are shown in Figures 7 and 8.

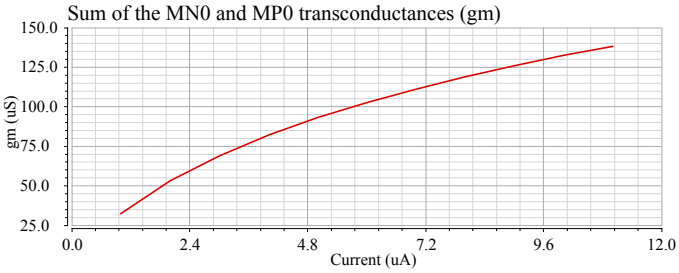

Fig. 7: AC Simulation - $(gm_{MP0} + gm_{MN0})$ of the amplifier.

Figure 7 shows the the variation of gm with amplifier current (I_d). For a current variation of approx 10 μA causes 100 μS change in sum of the transconductance. Amplifier current is varied to change the negative resistance. Figure 8 shows the small signal gain of amplifier for max 11 μA (Full startup current) and min 1 μA (normal mode current). It is observed that gain bandwidth product is varied as total gm changes (as C_L is held constant). Since gain bandwidth is different, gains are different at 32768 Hz frequency for normal mode and startup mode currents. This I_d variation in amplifier changes the negative resistance and hence the gain in the loop, which causes faster startup.

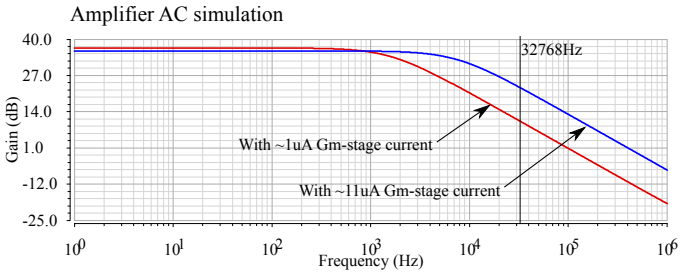

Fig. 8: AC Simulation - Gain plot of the amplifier.

B. Negative resistance

To ensure robust startup of the crystal oscillator, the magnitude of the negative resistance must be at least 5 times greater than Equivalent Series Resistance (ESR) during the initial start-up of the crystal but can be 2 to 3 times greater than ESR after start-up and during steady state operation. Figure 9 shows the plot of negative resistance versus I_d.

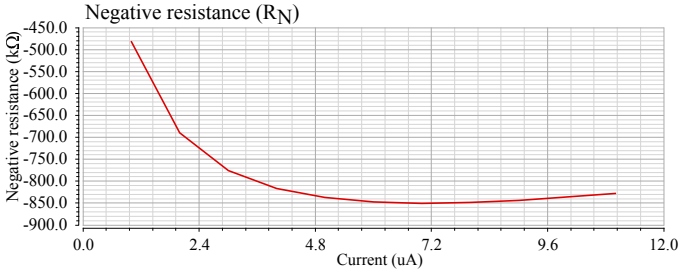

Fig. 9: Negative resistance vs. I_d plot

It is observed that the negative resistance reduces as current is reduced in startup circuit. From Figure 7 and from Equation 2 we can infer that negative resistance reduces as the amplifier current is reduced. Also it is observed that negative resistance is well above 2-3 times of ESR (70 $k\Omega$).

IV. Proposed Design

Based on the theory discussed in previous section, a fully integrated circuit is designed and simulated in 180 nm CMOS process. Bias generator, in Figure 2, is a Widlar self biased current generator circuit.

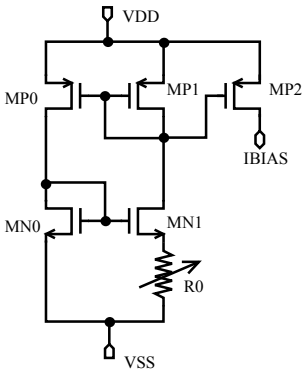

Fig. 10: Bias generation circuit

Clock generator is self referenced Schmitt trigger circuit, used for converting the sinusoidal waveform to full swing square waveform. Circuit is shown in Figure 11.

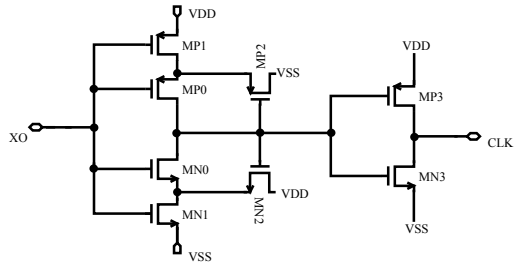

Fig. 11: Clock generation circuit

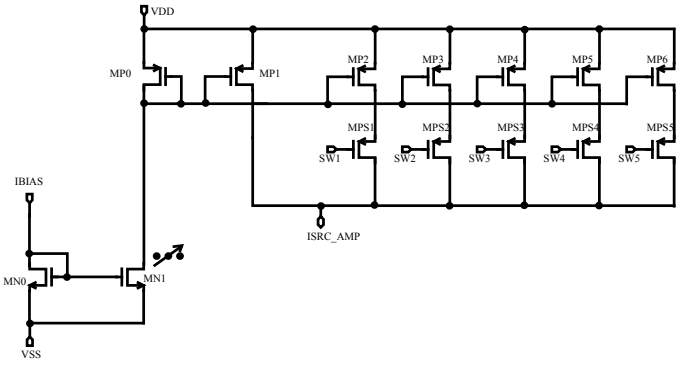

Fig. 12: Startup current generation circuit

Startup circuit is used for reducing the crystal clock generation and stabilization time. As shown in Figure 12, with 5 mirrored legs, current is increased in Gm-stage. The switches (SW1-SW5) are used for controlling the current in each leg. Once the clock starts, it is counted for definite number of cycles (For example 2^8 cycles). Then each current mirror is cutoff in sequence, effectively reducing the current in the inverter amplifier.

Startup time is improved by increasing the current in Gm-stage. However, to avoid the overdrive of crystal the time duration for which the current is given is controlled by the timer circuit. The digital timer circuit controls the current reduction in linear and equal intervals. As shown in Figure 13, a series of D-latches count for specified clock periods before cutting off the current mirrors.

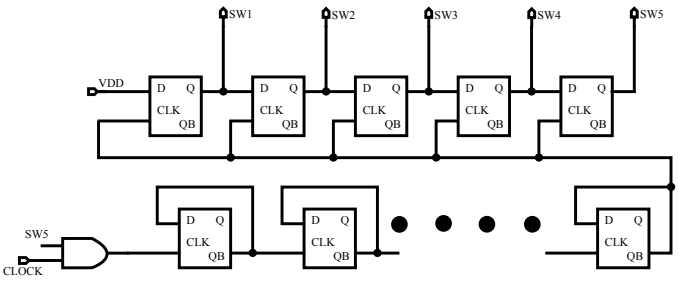

Fig. 13: Digital control generation circuit

V. Results and Analysis

The circuit is simulated and results are compared for startup behavior, without startup circuit and with conventional single step startup circuit with that of proposed step wise negative resistance reduction method.

The voltage buildup of the crystal as shown in Figure 14 is without startup improvement circuit. Gm-stage current is approx 1 μA (current is representation of the negative resistance). It can be observed that the crystal oscillation buildup to a set voltage (approx 1 Volt) is taking long time, approximately 330 ms.

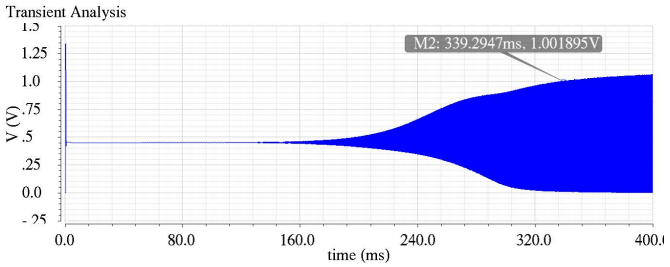

Fig. 14: Voltage buildup across the crystal without startup improvement circuit.

One method of improving the startup time is by giving the startup current for a long time to ensure quick startup, then at arbitrary large time, it may be switched off when external controller decides. This circuit is simulated with a higher current of approx 11 μA (same as the peak current when startup circuit is active). As shown in Figure 15, with increased current, the startup time is reduced to approximately 70 ms. But in this case, the voltage buildup across the crystal is beyond the set voltage and this increases the power dissipation in crystal and goes beyond the rated power of the crystal.

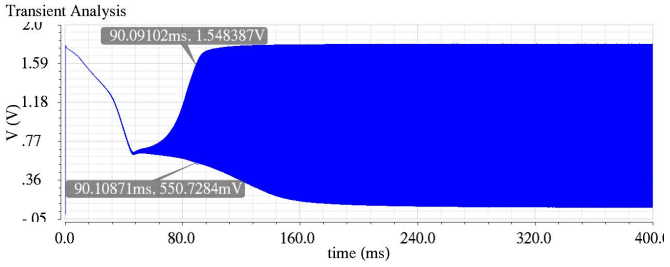

Fig. 15: Voltage buildup of high power mode

From theory and the previous simulation result as in Figure 15, it has been found that the startup time can be improved by increasing the current in amplifier. Conventionally to avoid the overdrive of the crystal, it is switched to low power mode after the oscillations are built up sufficiently or to the set level of voltage (approx 1 V). However, sudden change of the drive will alter the crystal voltage buildup and may cause the clock instability. As shown in Figure 16, it is required to wait till approx 220 ms for the voltage to buildup again. This method will not improve the startup time much but will limit the crystal drive.

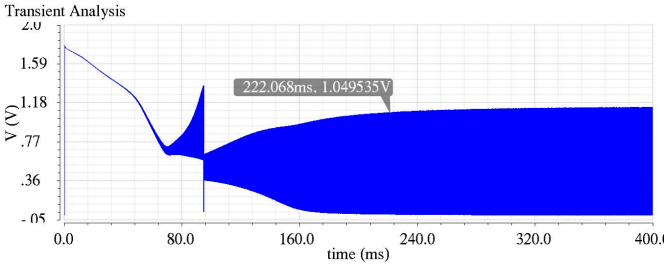

Fig. 16: Voltage buildup with low power mode

In the proposed method to improve the startup time, the high current mode is held till the voltage across the crystal is built up sufficiently and remove the current drive in multiple steps than in a single step. This way, extra drive is provided just long enough for startup process to happen. As shown in Figure 17, the steps are kept at regular time apart and faster startup of 160 ms is observed.

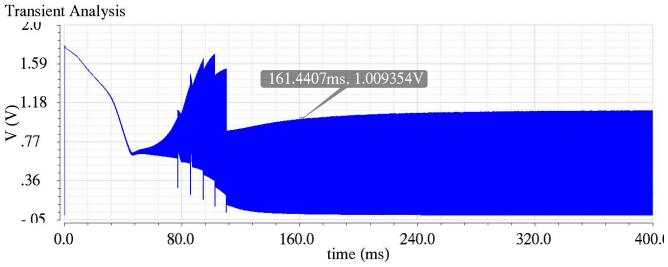

Fig. 17: Voltage buildup with digital control

VI. Conclusions

In this paper, a novel approach to improve the startup time of the crystal is proposed. The theory provides necessary insight to synthesize the optimum solution with respect to frequency stability, power consumption and crystal drive limit. The overall startup method and factors affecting the startup time are discussed with relevant equations. Analysis and simulations show the relation between Gm-stage current and negative resistance. Fully integrated circuit shows the practicability of the proposed method of startup. The simulation and analysis show that the proposed method results in much better startup behavior in comparison with conventional startup circuit and without startup circuit.

References

[1] Mike Mitchell. Implementing a real-time clock on the msp430. 2001.

[2] Shane A Blanchard. Quick start crystal oscillator circuit. In *University/Government/Industry Microelectronics Symposium, 2003. Proceedings of the 15th Biennial*, pages 78–81. IEEE, 2003.

[3] Shunta Iguchi, Hiroshi Fuketa, Takayasu Sakurai, and Makoto Takamiya. Variation-tolerant quick-start-up cmos crystal oscillator with chirp injection and negative resistance booster. *IEEE Journal of Solid-State Circuits*, 51(2):496–508, 2016.

[4] Ken Ueno, Tetsuya Hirose, Tetsuya Asai, and Yoshihito Amemiya. A 300 nw, 15 ppm/c, 20 ppm/v cmos voltage reference circuit consisting of subthreshold mosfets. *IEEE Journal of solid-state circuits*, 44(7):2047–2054, 2009.

[5] Qichao Zha, Tiejun Lu, Yu Zong, Jianhui Zhang, and Shaoxian Qu. Design of cmos crystal oscillator with low power consumption. *International Journal of Information and Electronics Engineering*, 3(6):630, 2013.

[6] Aatmesh Shrivastava, Divya Akella Kamakshi, and Benton H Calhoun. A 1.5 nw, 32.768 khz xtal oscillator operational from a 0.3 v supply. *IEEE Journal of Solid-State Circuits*, 51(3):686–696, 2016.

[7] Daniel Aebischer, Henri J Oguey, and Vincent R Von Kaenel. A 2.1-mhz crystal oscillator time base with a current consumption under 500 na. *IEEE Journal of Solid-State Circuits*, 32(7):999–1005, 1997.

[8] Eric A Vittoz, Marc GR Degrauwe, and Serge Bitz. High-performance crystal oscillator circuits: theory and application. *IEEE Journal of Solid-State Circuits*, 23(3):774–783, 1988.

[9] Anthony M Scalpi. Crystal oscillator design and negative resistance. Sep 2006.

[10] Theron Jones. Design a crystal oscillator to match your application. 2012.

[11] Phillip E Allen and Douglas R Holberg. *CMOS analog circuit design*. Oxford Univ. Press, 2002.