Impact of Process Variation Induced Transistor Mismatch on Sense Amplifier Performance

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Abstract

Sense amplifier is a very critical peripheral circuit in memories as its performance strongly affects both memory access time, and overall memory power dissipation. As the device dimensions scale below 100nm, the process variations are increasing and are impacting the circuit design significantly. The circuit yield loss caused by the process and device parameter variation has been more pronounced than before [1]. In this paper, effects of process variation induced transistor mismatch on sense amplifier performance are studied. A comparative study of the effect of mismatch on delay and yield for different sense amplifier configurations at 90nm technology is presented.

1. INTRODUCTION

Technology scaling has enabled us to integrate large memory blocks with logic circuits on a single chip. However, performance of the on chip memory limits the speed and performance of the overall system. The key limiting factor is the increasing bitline capacitance, which results in increased time to develop differential bitline voltage. For fast and power efficient memory designs, both this time and signal swing on the bitlines need to be minimized. A sense amplifier is used to generate full rail output voltage using minimum bitline differential voltage/current.

As CMOS IC fabrication technology becomes more and more advanced, the control of process variation and manufacturing uncertainty becomes more and more critical. The sense amplifier performance degradation due to process variations and resulting yield loss is more pronounced than before. It is important for the designer to be able to understand mismatch effects, since sensing should be done as fast as possible, subject to sensitivity constraints imposed by the parameter variations inherent in fabrication process [2]. For low power applications it is always desirable to have low bitline differential voltage. However, the bitline differential voltage has direct impact on yield of the sense amplifier [3].

This paper studies the effect of length mismatch and threshold voltage mismatch on sense amplifier designs at 90nm CMOS technology. Variations in sensing delay and yield with transistor mismatch are compared in three latch-type sense amplifiers and a current mode sense amplifier. Section 2 gives a brief introduction to process variations. Section 3 briefly describes the sense amplifiers used in this study. Section 4 explains experimental setup for mismatch analysis. Section 5 documents the simulation results and conclusions are presented in section 6.

2. PROCESS VARIATIONS

IC manufacturing variations can be placed in two categories: random variations and systematic variations. Random variations are inherent fluctuations in process parameters, such as random dopant fluctuations, oxide growth rates from die-to-die, wafer-to-wafer and lot-to-lot. On the other hand, systematic variations depend on the layout pattern and are therefore predictable. We focus on random variations which cannot be compensated, are difficult to minimize, and pose serious challenge in deep sub-micron (DSM) designs.

MOS transistor dimensions and the threshold voltage are among the key parameters that control CMOS transistor's drive current. MOS circuits become extremely sensitive to length and threshold voltage as we tend to use minimum length transistors and reduced supply voltage. The variation in substrate doping concentration and gate oxide thickness can be accounted for variation in threshold voltage. Charge centers near the oxide-substrate interface, fixed oxide charge and surface state densities - are likely to be the dominant mismatch sources for carrier mobility. Random variation in deposition, etching, annealing temperature and chemical mechanical planarization etc. contribute to channel length variation. Dependence of transistor current is increasingly non-linear to channel length. A 10% transistor gate length variation can translate to as much as a variation of -15% to +25% in gate delay [4]. Therefore parameter variations introduce asymmetry in the sense amplifiers, which in turn reduces the yield and performance.

A. Mismatch models

Transistor mismatch effects vary considerably between different regions (weak inversion, linear, saturation etc.) of operation. Various mismatch models are studied in the past and the drain current model is found to be less complex and fairly accurate for mismatch analysis (see [5] and the references there in). The current mismatch model for linear and saturation regions of operation are given by equations 1 and 2 below [5],

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Linear Region:

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta\beta}{\beta} - \frac{\Delta V_T(V_{SB})}{V_{GS} - V_T(V_{SB}) - (1/2)V_{DS}} - \frac{\Delta\theta_{eff}(V_{GS} - V_T(V_{SB}))}{1 + \theta_{eff}(V_{GS} - V_T(V_{SB}))} + \frac{\Delta V_{DS}}{V_{DS}} + \frac{\Delta V_{GS}}{V_{GS} - V_T(V_{SB}) - (1/2)V_{DS}} \quad (1)$$

Saturation Region:

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta\beta}{\beta} - \frac{2\Delta V_T(V_{SB})}{V_{GS} - V_T(V_{SB})} - \frac{\Delta\theta_{eff}(V_{GS} - V_T(V_{SB}))}{1 + \theta_{eff}(V_{GS} - V_T(V_{SB}))} + \frac{2\Delta V_{GS}}{V_{GS} - V_T(V_{SB})} + \frac{\lambda\Delta V_{DS}}{1 + \lambda V_{DS}} \quad (2)$$

where θ_{eff} is empirical effective mobility reduction factor and is a function of β and source and drain resistances. Other parameters in equation 1 and 2 have usual meanings. From the above equations it can be seen that the variation in drain current is a strong function of variations in β, V_T, θ_{eff} and drain-to-source voltages. In the present work, we have considered only the effect of variations in V_T and L on the performance of four types of sense amplifiers.

3. SENSE AMPLIFIER CIRCUITS

This section briefly illustrates the working of the sense amplifiers used in this study.

A. Latch-Type Sense Amplifiers:

Figures 1, 2 and 3 show three different latch-type sense amplifiers [2], [6], [9], [11]. All the circuits use cross-coupled inverter latch. The inverters are initialized in the transient region before the sense amplifier is activated, by precharging and equalizing the sense amplifier output nodes. These sense amplifiers remain turned-off (*SAEN* at zero) until a sufficient voltage differential has been developed between the bitlines. When *SAEN* goes high the cross-coupled inverter pair moves to a stable operation point based on the bitline voltages. Due to positive feedback and high gain these sense amplifiers quickly produce the output. However, that also makes them very sensitive to parameter variations.

B. Clamped Bitline Sense Amplifier (CBLSA):

This is a current mode type sense amplifier, which amplifies a small differential current between the bitlines into a full rail-to-rail voltage. Its low input impedance makes it suitable for larger memories.

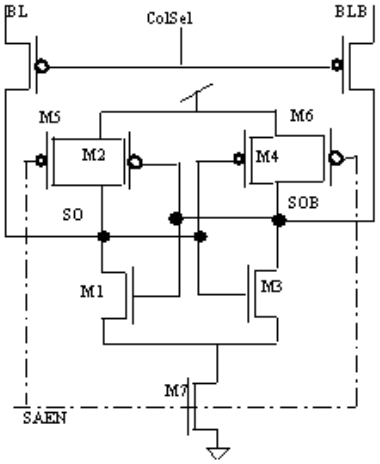

Fig. 1: Latch type sense amplifier 1

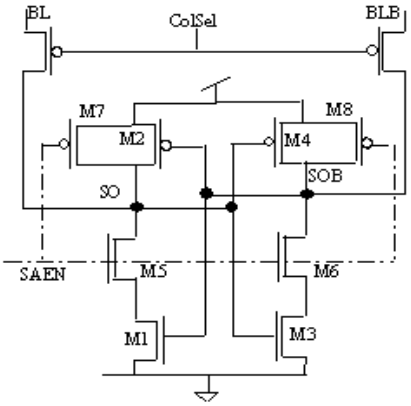

Fig. 2: Latch type sense amplifier 2

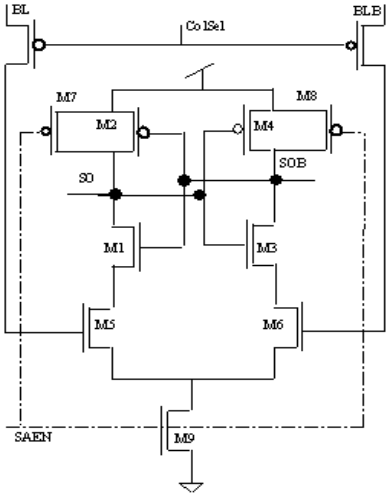

Fig. 3: Latch type sense amplifier 3

Figure 4 shows circuit schematic of CBLSA. We have modified the basic CBLSA of [7], [8] by adding transistor M8. It is found that the addition of M8 speeds up the decision process and reduces the sensing delay by roughly 10%.

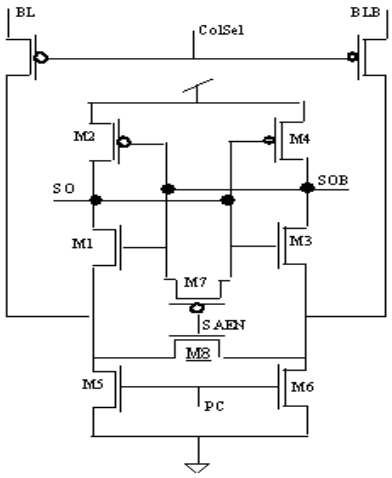

Fig. 4: Clamped bitline sense amplifier (CBLSA)

Sense amplifier delay variation with bitline differential voltage is shown in figure 5 for the four types of sense amplifiers. From the graph, we see that the sensing delay decreases with increase in differential voltage. CBLSA is found to be fastest among the four types of sense amplifiers. However, the rate of decrease of delay with increase in differential voltage is highest in Latch-type1 sense amplifier and lowest in Latch-type3 sense amplifier.

4. EXPERIMENTAL SETUP

The sense amplifier is said to be perfectly balanced or symmetric when all the transistor parameters on the left-hand side are equal to parameters on the right-hand side. It is said to be vertically matched when the W/L's of NMOS and PMOS have been ratioed so that the sense amplifier has equal pull-up and pull-down capability [2]. For mismatch analysis we consider only the variation in channel length and threshold voltage of the transistors. Our analysis assumes that a particular parameter x (where x is either L, W or V_T of the device), is varied by decreasing the value of that parameter for the NMOS transistors in the left hand side of the sense amplifier by Δx and increasing it by the same amount for corresponding right hand side transistors. We assume perfect matching in PMOS transistors while performing mismatch analysis of NMOS transistors and vice-versa. In all sense amplifiers total width of all the transistors is kept nearly same for fair comparison. Simulations are carried out for 90nm CMOS technology, using Berkeley Predictive Technology Model (BPTM) [10] and considering nominal values of NMOS and PMOS transistor threshold voltages as 0.26V (V_{tn}) and -0.303V (V_{tp}) respectively. A nominal output load capacitance of 5fF is assumed at sense amplifier output nodes. The circuits are tested to read both logic low and logic high from consecutive memory locations. Channel length of all the critical NMOS transistors (M1 and M3 in Latch-Type1 and M1, M3, M5 and M6 in the remaining circuits) is taken as 150nm. However, for rest of the transistors in the circuit the length is taken as 100nm. A 200fF bitline capacitance is assumed for all the simulations. Power supply voltage is assumed to be at 1V.

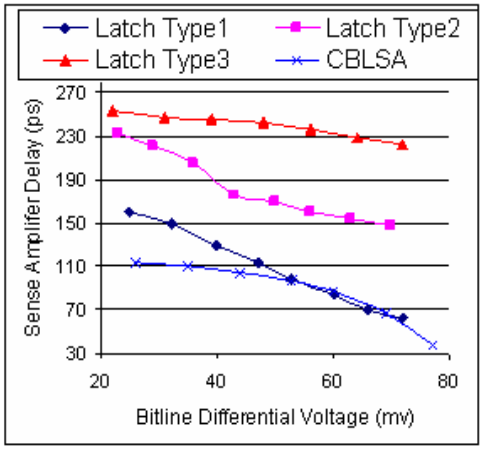

Fig. 5: Sense amplifier delay vs bitline differential voltage

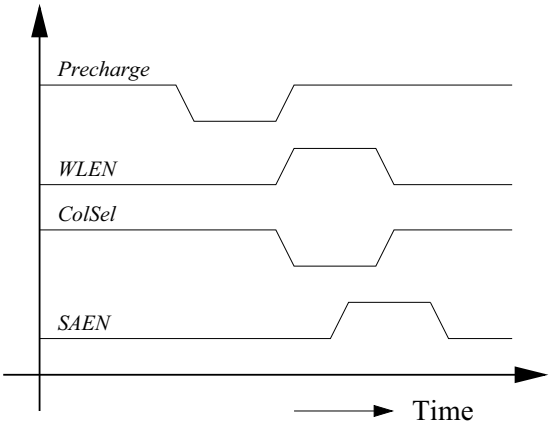

Fig. 6: Sense amplifier timing scheme

The timing scheme used in all the sense amplifiers is shown in figure 6. The wordline enable (*WLEN*) and column select (*ColSel*) are activated for a short duration during the sensing operation. Both the signals are deactivated after sufficient differential voltage/current is developed between the bitlines. This has the effect of isolating bitline capacitances from the sense amplifier. This kind of timing scheme helps in reducing signal swing on bitlines, thereby reducing power dissipation.

5. SIMULATION RESULTS

Extensive simulations are carried out to check the effect of mismatch in V_{tn} and channel length. For all mismatch analysis time interval between *WLEN* and sense amplifier enable (*SAEN*) is kept constant at 110ps in all the four circuits under consideration. The sense amplifier delay was measured as the time taken for the sense amplifier's output to reach 90% of the full-rail voltage after the *SAEN* signal goes high.

A. Mismatch Analysis

a) Mismatch in NMOS Parameters: For the circuit shown in figure 1, V_{tn} of M1 is decreased and that of M3 is increased by same amount. For circuits shown in figures 2, 3 and 4, the V_{tp} of M1 and M5 is decreased while that of M3 and M6 is increased. Similar analysis is carried out to study channel length mismatch in NMOS transistors. For all the simulations we assume that the SRAM cell content is logic high, since this gives the worst case results for the above setup.

The results of delay versus NMOS threshold voltage mismatch are shown in figure 7. It is found that, Latch-Type1 sense amplifier fails to read correctly when the percentage of V_{tn} mismatch on either side is greater than 8, and the Latch-Type2 and Latch-Type3 fail at 7% and 6% respectively. However CBLSA is relatively more sensitive to mismatch in NMOS threshold voltage which fails at 5%. Similar trend is observed with NMOS length mismatch. However, if minimum length (i.e. 100nm) NMOS transistors are used, CBLSA is found to become extremely sensitive to mismatch in channel length. Simulation results for NMOS length mismatch are shown in figure 8.

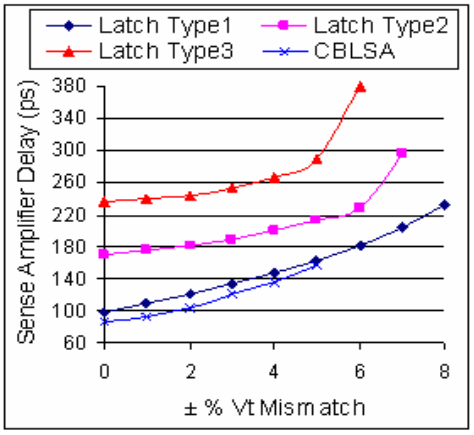

Fig. 7: Sense amplifier delay vs NMOS V_t mismatch

From figure 8 we find that sensing delay increases with the mismatch. However, the delay decreases when a logic low is read with the same setup. Exactly reverse phenomenon can be expected, if the parameters of the NMOS transistors in the left hand side are increased while those in the right hand side are decreased.

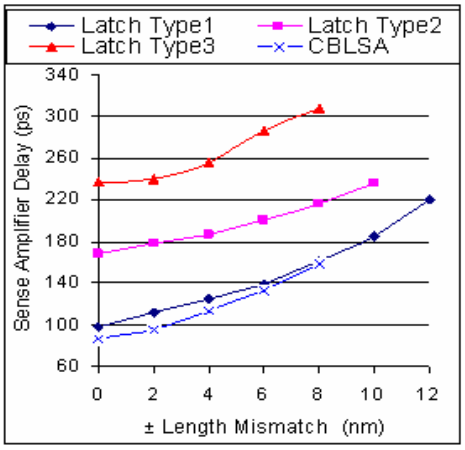

Fig. 8: Sense amplifier delay vs NMOS channel length mismatch

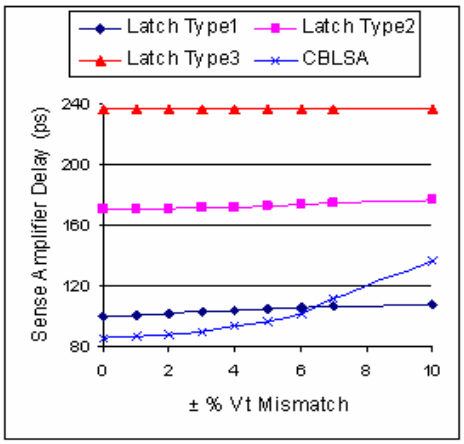

Fig. 9: Sense amplifier delay vs PMOS V_t mismatch

b) Mismatch in PMOS Parameters: Parameter mismatch of PMOS transistors does not drastically affect performance of the sense amplifier. The reason being, when the sense amplifier is activated NMOS transistors immediately start operating in saturation region, however PMOS transistors operate either in cut-off or conduct in deep triode region. Mismatch analysis is carried out by decreasing V_{tp} of M2 and increasing V_{tp} of M4 by the same amount. Similar variations in channel length are imposed to understand the effect of length mismatch. The readings are taken when the SRAM cell content is logic low, as this gives worst case results. Simulation results for threshold voltage mismatch and length mismatch are shown in figure 9 and 10 respectively. However, the sense amplifier delay decreases when logic high is read from the memory. Simulation results show that except

CBLSA, all latch type sense amplifiers are less sensitive to variation in PMOS parameters.

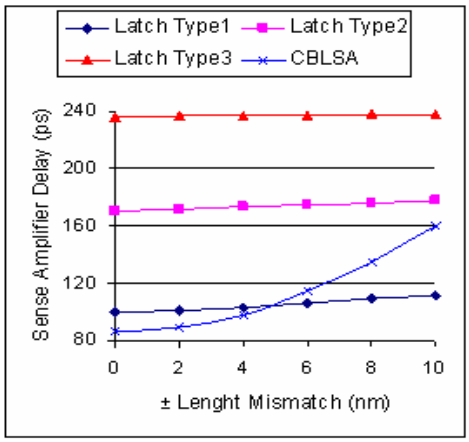

Fig. 10: Sense amplifier delay vs PMOS channel length mismatch

B. Yield Analysis

For successful read operation, the sense amplifier should be activated only after development of sufficiently large bitline differential voltage or current. However, to decrease the overall sensing delay, it is desirable to activate the sense amplifier as early as possible. Sense amplifier may fail to read correctly due to its asymmetry, which is a result of manufacturing process variations. Yield analysis is carried out using Monte-Carlo simulations, and varying bitline differential voltage (current in the case of CBLSA). Threshold voltage and channel length of all the NMOS transistors (M1 and M3 in Latch-Type1, M1, M3, M5, and M6 in the remaining circuits) is randomly varied simultaneously to reflect practical scenario. For NMOS threshold voltage Gaussian distribution is assumed with a standard deviation of 12mv and a mean value of 260mv. Similarly Gaussian distribution is assumed with a standard deviation of 4nm and a mean value of 150nm, for NMOS channel lengths. All Monte-Carlo simulations incorporate 6σ variation, where σ is the standard deviation of the parameter. The yield analysis results are shown in figure 11 with each marker representing the yield measurement for a sample size of 1000. Yield is calculated using the following simple equation.

$$Yield = \frac{number\ of\ correct\ decisions}{number\ of\ samples} \qquad (3)$$

In the case of CBLSA, yield analysis is carried out by changing bitline differential voltages. However, corresponding currents are measured (shown in table 1) and the yield is plotted as a function of bitline differential voltage for the purpose of comparison with latch-type sense amplifiers. Simulation plot in figure 11 shows that Latch-type2 sense amplifier has a marginally higher yield compared to all other types of sense amplifiers. Yield can be increased by decreasing the gain of the sense amplifier. However, the penalty for decrease in gain is increased sensing delay.

TABLE 1: CBLSA BITLINE DIFFERENTIAL VOLTAGE AND CORRESPONDING CURRENT

Differential Voltage (mv)	Differential Current (μA)
16	13
26	15
35	16
44	17
53	19
60	20
69	21.5
77	23

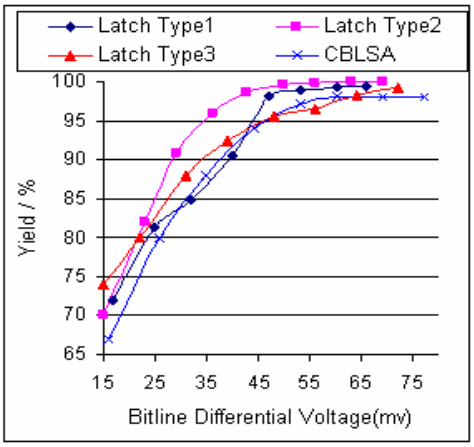

Fig. 11: Yield vs bitline differential voltage

6. CONCLUSIONS

Impact of process variation induced transistor mismatch on four different sense amplifier configurations is presented. It is found that as the mismatch increases sensing delay also increases, eventually leading to failure of the sense amplifier. Performance of the sense amplifier is worst affected by mismatch in NMOS transistor threshold voltage and channel length whereas performance degradation due to PMOS parameter variations is found to be marginal. Clamped bitline sense amplifier is found to give best performance in terms of speed, although when compared to latch type sense amplifiers it is marginally more sensitive to parameter variations. From the yield analysis it is found that mismatch reduces the yield in all the four cases. Latch-Type2 sense amplifier is found to give the best yield.

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