Impedance Matching for the Reduction of Via Induced Signal Reflection in On-Chip High Speed Interconnect Lines

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***Abstract*—Advancements in VLSI technology has made it possible to have more than eight metal layers connecting millions of closely placed devices in a single IC chip. Different interconnect layers run across the chip and the necessary connections across the layers are made through vias. The impedance discontinuity at the junction of the via and the interconnect line creates signal reflections and contributes to the loss of the signal. This paper proposes a method for the reduction of via induced signal reflection in multi layer high speed on-chip interconnect structures. At the junction of the interconnect and the via, impedance mismatch is reduced by the inclusion of an appropriate capacitive load. In this paper, we show the reduction in signal reflection upto a frequency of 9 GHz using the proposed model for the dimensions of 65 nm technology node in the case of two interconnect layers connected through a single via.**

I. Introduction

As the signals transmitted through the interconnects in modern Very Large Scale Integrated (VLSI) circuits reached above 2 Giga bits per second (Gbps), signal integrity plays an important role in successful data transmissions. Recent Integrated Circuit (IC) chips have more than eight metal layers and 100 million transistors [1]. Vias are extensively used to connect the signal traces (interconnect lines) residing on different layers.

Vias size are relatively small compared to the length of the interconnect lines and behaves almost like an ideal connector at low frequencies due to small electrical length. Due to this, vias are either completely ignored in the analysis or simulated with a lumped inductance or with a lumped capacitance and calculated with approximate equations. When the signals transmitted through the interconnects reached above 1 GHz, vias started to behave as distributed structures.

The impedance difference between the vias and the signal traces introduces signal reflections at GHz frequencies. Vias create considerable voltage breakdown and signal integrity problems such as signal attenuation, crosstalk, switching noise etc [2]. There have been various studies on the properties and types of vias ([3]-[5]). The capacitance and inductance of a through-hole via has been analyzed using the quasi-static approach ([3]-[7]) or from full wave simulations ([8]-[10]). Multi via interconnect structures have been analyzed by decomposing the geometry into exterior and interior structures [11]. In addition to these, several papers were published on the efficient modeling of multiple vias ([12]-[13]) in high speed interconnect circuits.

Signal reflection reduction techniques in high speed interconnects with vias for multi layer Printed Circuit Board (PCB) structures are discussed in several papers. In [14], it is demonstrated that an appropriate shape of the transmission line near the via can reduce the reflections in interconnect lines. A coaxial type via hole structure is proposed in [15] that reduces the amount of reflection noise on high speed signals in multilayer interconnect structures. The design technique of employing an artificial neural network for constructing reflection less via structures is proposed and validated in [16]. The impact of via parameters like diameter, height and stub effect on signal reflections are analyzed and the reflections are reduced to minimum with optimized via dimensions [17].

In all these papers, signal reflection reduction methods are aimed towards PCBs and based on the via structures and optimization of the via parameters. Via equivalent circuits are represented by lumped *LC* circuits. As the technology node decreases, via resistance increases significantly (0.3 Ω in 0.7 μm to 8 Ω in 90 nm)[18]. Further, the impedance discontinuity at the junction of the interconnect line and the via creates signal reflections. This causes some amount of loss in the signal transmitted.

In this paper, we propose a method to reduce the signal reflection in high speed on-chip multi layer interconnect structures in an IC chip. The via is represented by lumped *RLC* model in the form of **T** network. Reflections are reduced by impedance matching through the addition of the suitable capacitance value at the junction of the interconnect line and the via. Expression to calculate the value of the load capacitance to be included at the junction of the via and the interconnect line is formed. Using the proposed model, the effect on the signal reflections are analyzed using S parameters in the case of the two interconnect layers connected through a via.

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The rest of this paper is organized as follows. Introduction to the via structure is given in section II. Section III gives the expressions to find the value of the characteristic impedance of the interconnect line and the value of the matching capacitance to be added for minimum signal reflection. The model for the signal reflection reduction between two interconnect layers connected through a via and its analysis is given in section IV. The conclusions are given in section V.

II. Via Structure

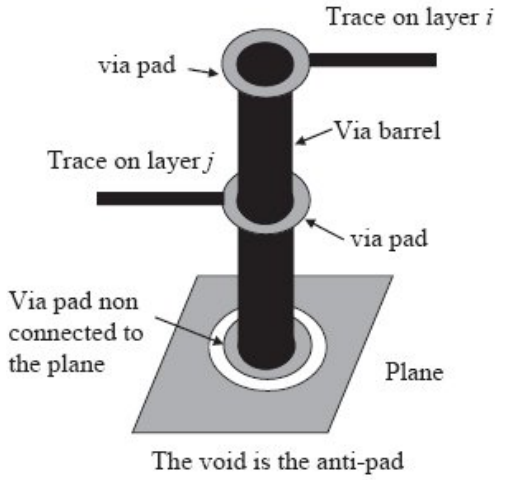

Fig. 1. Simple Via Structure

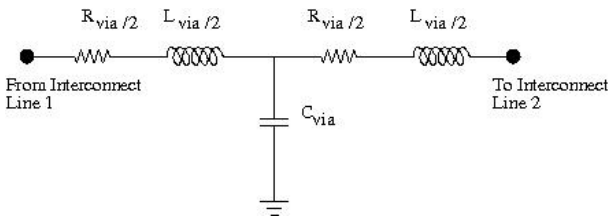

Fig. 2. Lumped RLC equivalent via model

A via is defined as an electrical connection between signal traces on different layers in a multi layer structure. A simple via is shown in Fig. 1. Via is a small conductive cylindrical hole drilled from one layer to another layer that is used to make electrical connections between the traces of various layers of the interconnect structure in an IC. It consists of the barrel, the pad and the anti pad. The barrel is a conductive material that fills the hole to allow an electrical connection between the layers, the pad is used to connect the barrel to the component or trace and the anti pad is a clearance hole between the pad and the metal on a layer to which no connection is required [19].

Via resistance (R_{via}), inductance (L_{via}) and capacitance (C_{via}) are modeled as a function of physical dimensions and material characteristics of the via [20]. A lumped *RLC* model represented in the form of **T** network as the equivalent of a via is shown in Fig. 2. Voltage drop between the interconnected nodes of the two metal layers is caused by R_{via}, L_{via} and the capacitive component C_{via} seen between the via and the ground.

The expressions to estimate the resistance, inductance and capacitance values of the via equivalent circuit is given in 1, 2 and 3 [20].

$$R_{via} = \frac{\rho h_{via}}{\pi r_{via}^2} \tag{1}$$

$$L_{via} = \frac{\mu_0}{4\pi}[h_{via} ln(\frac{2h_{via} + \sqrt{r_{via}^2 + (2h_{via})^2}}{r_{via}}) + (r_{via} - \sqrt{r_{via}^2 + (2h_{via})^2})] \tag{2}$$

$$C_{via} = \frac{2\pi\epsilon_r\epsilon_0 h_{via}}{ln((r_{via} + t)/r_{via})} \tag{3}$$

where ρ is the resistivity of the conducting material, r_{via}, h_{via}, and t represents the radius, length and dielectric thickness of the via respectively, ϵ_r is the relative permittivity of the material, ϵ_0 is the permittivity of the free space (8.852×10^{-12} F/m) and μ_0 is the permeability of free space ($4\pi\times10^{-7}$ H/m).

III. Expression to find the value of Capacitance for Impedance Matching

When an electromagnetic wave propagates from one media to another media (in our case, interconnect line to via) with differing characteristic impedances, two things will happen: (i) a portion of the wave is reflected away from the impedance discontinuity back toward the source and (ii) a portion of the wave is transmitted through the via. The simultaneous existence of both the transmitted and reflected waves is a direct result of the boundary conditions that must be satisfied when solving Maxwell's equations at the interface between the two regions [19].

When the plane wave is propagating in the transverse electromagnetic (TEM) mode, the difference of the incident and reflected waves must equal to the transmitted wave. i.e.

$$v_t = v_i - v_r \tag{4}$$

$$\frac{i_t}{Z_{via}} = \frac{i_i}{Z_0} - \frac{i_r}{Z_0} \tag{5}$$

where v_i, v_r, v_t, i_i, i_r and i_t are the incident, reflected and transmitted voltage and current waves respectively. Z_0 is the characteristic impedance of the transmission line and Z_{via} is the impedance of the via equivalent circuit.

Since the incident waves are known, Eq. 4 and 5 are solved simultaneously for the transmitted and reflected portions of the wave. The expressions for v_t and v_r are expressed as

$$v_t = v_i \frac{2Z_{via}}{Z_{via} + Z_0} \tag{6}$$

$$v_r = v_i \frac{Z_{via} - Z_0}{Z_{via} + Z_0} \tag{7}$$

The reflection coefficient (Γ) is a measure of how much of the signal is reflected back by the intersection between the two impedance regions and the transmission coefficient (ξ) tells how much of the wave is transmitted. From Eq. 6 and 7, we have

$$\Gamma = \frac{v_r}{v_i} = \frac{Z_{via} - Z_0}{Z_{via} + Z_0} \tag{8}$$

$$\xi = \frac{v_t}{v_i} = \frac{2Z_{via}}{Z_{via} + Z_0} \tag{9}$$

By implementing the interconnect lines as microstrip lines, the characteristic impedance of the finite thickness microstrip line [21] is given in Eq. 10.

$$Z_0 = \sqrt{\frac{\epsilon_0 \mu_0}{\varepsilon_{eff}}} \frac{1}{C_a} \tag{10}$$

where

$$C_a = \begin{cases} \dfrac{2\pi\varepsilon_0}{ln(8h/w_e + w_e/4h)} & , \dfrac{w_e}{h} \leq 1 \\ \varepsilon_0[\frac{w_e}{h} + 1.393 + 0.667ln(\frac{w_e}{h} + 1.444)] & , \dfrac{w_e}{h} > 1 \end{cases}$$

$$w_e = \begin{cases} w + 0.398t(1 + ln\dfrac{4\pi w}{t}) & , \dfrac{w}{h} \leq \dfrac{1}{2\pi} \\ w + 0.398t(1 + ln\dfrac{2h}{t}) & , \dfrac{w}{h} > \dfrac{1}{2\pi} \end{cases}$$

$$\zeta = \begin{cases} 0.02(\epsilon_r - 1)(1 - \dfrac{w}{h})^2 & , \dfrac{w}{h} < 1 \\ 0 & , \dfrac{w}{h} > 1 \end{cases}$$

$$\epsilon_{eff} = [\frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}(1 + 12\frac{h}{w_e})^{-1/2} + \zeta - 0.217(\zeta - 1)\frac{t}{\sqrt{w_e h}}]$$

where w and t are width and thickness of the conductor. Substrate thickness is represented by h. The terms e_{eff} and w_e in Eq. 10 accounts for the effective dielectric constant and extra capacitance caused by the finite thickness of the signal conductor.

The input impedance Z_{in} seen from the right terminal of the first interconnect layer (point B in Fig. 8) is computed by replacing the via in Fig. 8 by its equivalent circuit given in Fig. 2. Thus Z_{in} is given by

$$Z_{in} = (\frac{R_{via} + j\omega L_{via}}{2}) + [\frac{1}{j\omega C_{via}} \parallel (\frac{R_{via} + j\omega L_{via}}{2} + Z_{02} + (\frac{1}{j\omega C_L} \parallel Z_{t2}))] \tag{11}$$

where Z_{02} is the characteristic impedance of the second interconnect layer, Z_{t1} Z_{t2} are the terminating resistance at the input and output side used for S parameter analysis and C_L is the load capacitance.

The signal reflection is minimum when the characteristic impedance of the microstrip line matches with the via impedance. A matching can be achieved by connecting an appropriate matching capacitance (C_m) between point B and ground as shown in Fig. 10. The new input impedance seen at point B in Fig. 10 is

$$Z_{match} = (\frac{1}{j\omega C_m} \parallel Z_{in}) \tag{12}$$

Substituting the expression for Z_{in} in Eq. 12 and simplifying, the expression for C_m is given by

$$C_m = \frac{1}{jw}\left[\frac{1}{Z_{match}} - \frac{1}{x + \dfrac{(a + jb)}{(c + jd + 1)}}\right] \tag{13}$$

where

$$x = \frac{R_{via} + j\omega L_{via}}{2}$$
$$a = R_{via} - \omega^2 L_{via} C_{via} Z_{t2} + 2Z_{02} + 2Z_{t2}$$
$$b = R_{via} C_L Z_{t2} + L_{via} + 2Z_{02} C_L Z_{t2}$$
$$c = -\omega^2 C_{via}(R_{via} C_L Z_{t2} + L_{via} + 2Z_{02} C_L Z_{t2})$$
$$d = \omega C_{via}(R_{via} - \omega^2 L_{via} C_L Z_{t2} + 2Z_{02} + 2Z_{t2})$$

The value of C_m is adjusted for maximum impedance matching and minimum signal reflection.

IV. Simulation Results

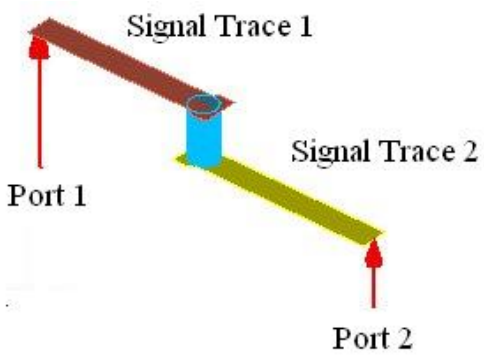

Fig. 3. 3D view of the two interconnect layers connecting through via

Figure 3 shows the 3D view of the two interconnect layers connected through a via. Modeling and simulations of the interconnect structures with via are carried out using Advanced Digital System (ADS) software. In this work, we have used interconnect parameters of 65 *nm* technology node [22].

Interconnect layer 1 and layer 2 are connected through via. We have considered the following via dimensions: via diameter of 0.4 μm, pad diameter of 0.65 μm, via height of 10 μm and dielectric thickness 10 nm. Interconnects are connected between transmitter and receiver. The receiver section is modeled as load capacitance (C_L). Interconnect line length and C_L are considered as 0.5 mm and 0.25 pF respectively.

Lumped *RLC* model represented in the form of **T** network is shown in Fig. 2. Table I shows via parameters calculated using Eq. 1 to 3 for the specified via dimensions. Fig. 4 shows the input signal reflection (parameter S_{11} at point A) of the structure in Fig. 8 along with the via equivalent model of

TABLE I
CALCULATED PARAMETERS USING EQUATIONS

Parameters	Value	Unit
R_{via}	3.5	Ω
L_{via}	26.09	pH
C_{via}	113.98	fF
Z_{01}	76	Ω
Z_{02}	88	Ω
C_m	344.74	fF
(for Z_{01}^*=Z_{match})		

Z_{01}^*: Characteristic impedance of the first interconnect line

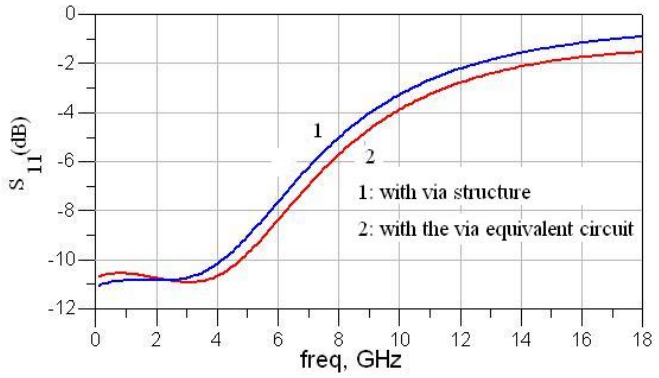

Fig. 4. Signal reflection in the interconnect layers connected through via equivalent circuit and via structure

Fig. 2. We find that both the responses are closely matching. Hence the model shown in Fig. 2 can be used as the equivalent of the via.

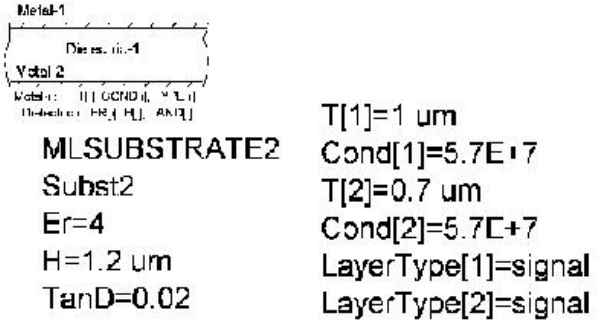

Fig. 5. ADS setup for the simulation of 2 layer structure

The ADS setup for creating two layer structure is given in Fig. 5. In Fig. 5, the values of the relative dielectric constant of the substrate (ϵ_r), height of substrate (H), dielectric loss tangent (TanD), metal thickness (T[n]), conductivity (Cond[n]), type of the metal layer (LayerType[n]) and name (LayerName[n]) are listed.

The ADS setup for via connection is given in Fig. 6. Via pad (MLVIAPAD) connects interconnect layer to a via hole

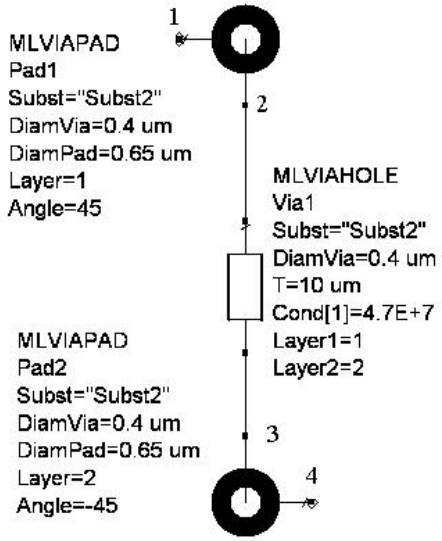

Fig. 6. ADS setup for via

(MLVIAHOLE). Pin 1 of Pad1 is connected to interconnect layer 1 and pin 2 is connected to Via1. The other end of Via1 is connected to pin 3 of Pad2 and pin4 is connected to interconnect layer 2.

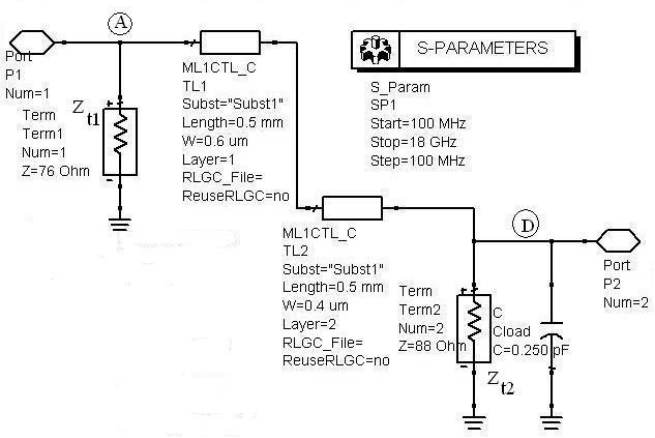

Fig. 7. Structure of the two interconnect layers connected without via

Signal reflections between two interconnect layers connected without and with via are measured from the arrangements shown in Fig. 7 and 8 respectively. Figure 9 shows the signal reflection measured at point A in Fig. 7 and 8. From Fig. 9, it can be seen that there is a significant increase in the signal reflection at lower frequency (upto 8 GHz) in the structure employing via in comparison to the structure without a via. This is due to the impedance mismatch between the interconnect layer and the via.

To mitigate the signal reflection at the junction of the via and the interconnect, we insert a capacitance between point B and ground as shown in Fig. 10. Figure 11 shows the signal reflections at the input side (point A in Fig. 10) for different

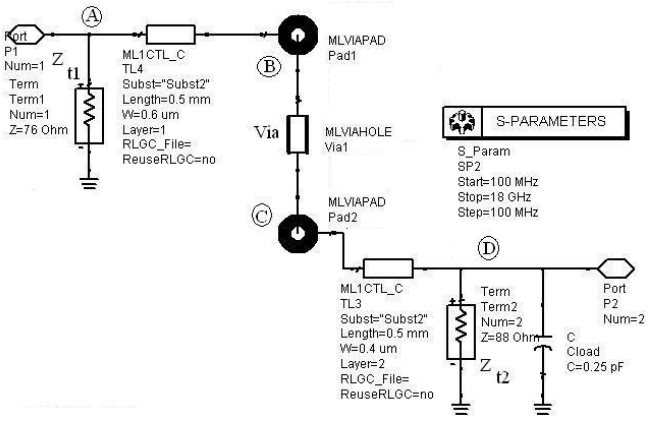

Fig. 8. Structure of the two interconnect layers connected through a via

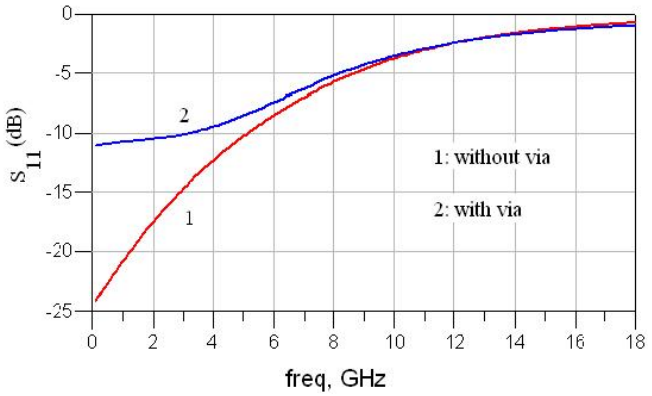

Fig. 9. Simulation result of signal reflection in the arrangement of without and with via

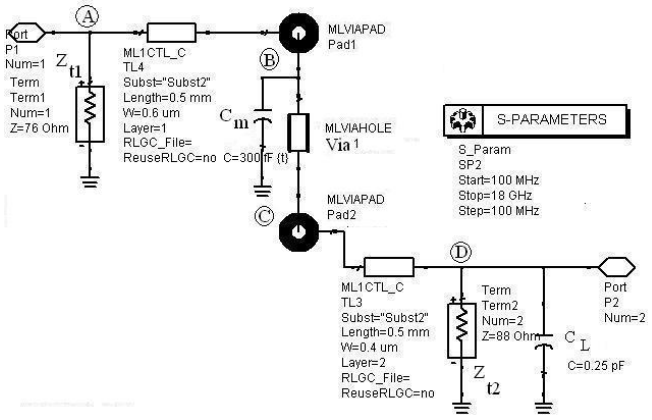

Fig. 10. Arrangement used to measure the signal reflection in two interconnect layers connected through a via

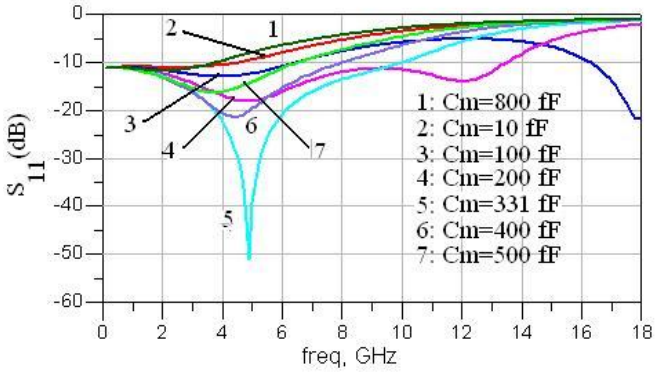

Fig. 11. Simulation result of signal reflection for different matching capacitance values

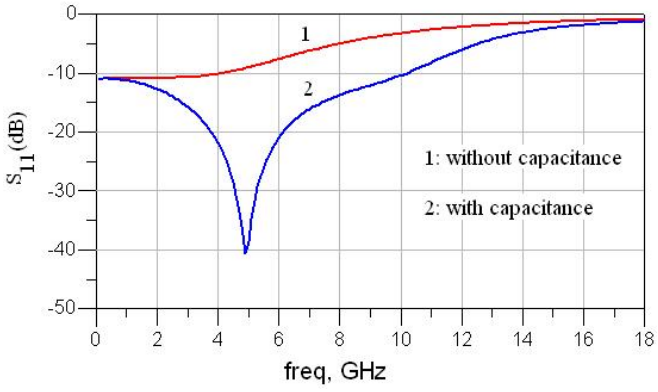

Fig. 12. Simulation result of signal reflection with and without capacitance

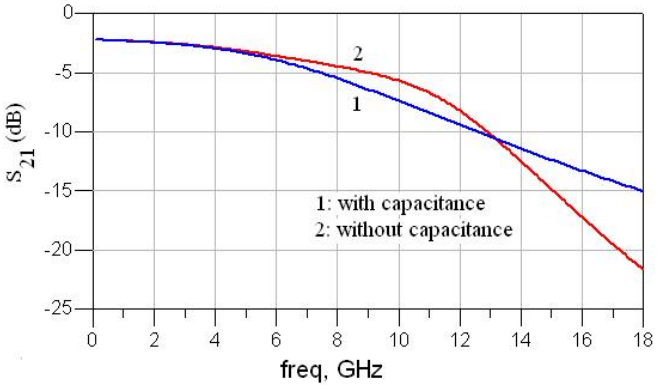

Fig. 13. Simulation result of transmission loss without and with capacitance

matching capacitance (C_m) values.

It is observed from Eq. 13 that the minimum signal reflection is dependent on the matching terminating resistances (Z_{t1} and Z_{t2}) and the load capacitance C_L. In this work, we are interested to have minimum signal reflection in the range of 1-10 GHz. By keeping the minimum signal reflection point at 5 GHz with Z_{t1}=76Ω and Z_{t2}=88Ω, the theoretical value (Eq. 13) of C_m is found to be 344.74 fF (Table I). From the simulations, the matching capacitance value is found to be 331 fF at 5 GHz (Fig. 11).

Figure 12 and 13 shows the signal reflection (S_{11}) and transmission loss (S_{21}) at point A for without and with capacitance at point B in Fig. 10. From Fig. 12, it can be seen that there is a clear advantage in using a matching capacitance to reduce signal reflections.

Using the proposed method, signal reflections can be re-

duced in multi layer structures. In multi layer structure, signal lines are surrounded by ground/power lines for the minimization of crosstalk. Hence the matching capacitances can be easily connected between the ground plane and the junction of the interconnect layer and the via. The matching capacitances (C_m) can be realized using n-MOS devices. Since the value of C_m is moderate, the area consumed by these capacitors is not very significant.

V. Conclusion

Via induced signal reflections at high frequencies in an interconnect structure causes performance degradation in high speed circuits. In this work, an analysis of signal reflections in the frequency range of 1 GHz to 10 GHz is carried out for two layer interconnect structure with vias as connecting elements between different layers. The via equivalent model is represented by lumped *RLC* circuit and simulation results show that responses obtained from via equivalent circuit and with via structure are closely matching. A matching load capacitance is used to reduce the signal reflection arise due to the impedance mismatch between the junction of the interconnect and the via. The matching capacitance value is analytically computed using the formed expression and is found to be closely matching with the simulation results.

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