IET Circuits, Devices & Systems

Research Article

IET Journals
The Institution of Engineering and Technology

11.39 fJ/conversion-step 780 kS/s 8 bit switched capacitor-based area and energy-efficient successive approximation register ADC in 90 nm complementary metal–oxide–semiconductor

ISSN 1751-858X
Received on 20th January 2017
Revised 3rd September 2017
Accepted on 22nd November 2017
E-First on 15th January 2018
doi: 10.1049/iet-cds.2017.0029
www.ietdl.org

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Abstract: In this study, a design technique for low-energy consumption and area-efficient successive approximation register analogue-to-digital converter (ADC) is presented. Digital-to-analogue conversion equivalent voltage is acquired utilising passive sharing of charge between two unit capacitors and integration of the shared charge onto an input sample-and-hold capacitor, via a switched capacitor integrator circuit. The architecture is less parasitic sensitive and low noise, yielding an area and energy-efficient ADC. To demonstrate the efficacy of the proposed technique, a ±350 mV 8 bit 0.78 MS/s ADC is designed in a 90 nm complementary metal–oxide–semiconductor process. The ADC core has a small area footprint of 0.00145 mm^2 and has a figure-of-merit of 11.39 fJ/conv-step.

1 Introduction

Biomedical implants and wireless sensor nodes are constrained to dissipate low power and occupy low chip area [1]. Successive approximation register (SAR) analogue-to-digital converters (ADCs) are widely preferred for digitisation due to low-power consumption. The SAR ADCs with traditional binary weighted capacitor array (BWCA)-based approach, listed in [2, 3], show low-power consumption. The area and power performances are, however, limited by capacitor mismatch of the array.

For the matching requirement, the unit capacitor and hence the capacitor array size becomes large. Capacitors are custom designed in [4] to achieve small size unit capacitors with good matching performance. While doing so the power consumption due to the capacitor array is reduced, whereas the area occupied by the capacitor array remains unaltered. Dynamic element matching technique [5] reduces capacitor mismatch effect, but incurs additional hardware and switching losses. Increased metal interconnect parasitics at lower technology nodes offer routing challenges. Hence BWCA-based SAR ADCs are area inefficient.

On the other hand, non-BWCA-based SAR ADCs constituting large-sized unit capacitors show good matching performance. These ADCs adopt passive sharing of charge between capacitors to generate digital-to-analogue conversion (DAC) voltage. Voltage buffers track the DAC equivalent in [6] rendering the design power inefficient. Charge holding unit capacitors are serially connected in [7] to achieve DAC equivalent, but accuracy is lost due to switch and capacitor bottom plate parasitics. Switch parasitics again degrade linearity despite the usage of a vast number of unit capacitors and conversion clock cycles in [8]. In general, the performances of these ADCs are limited by parasitics. Switched capacitor (SC) integrator-based SAR ADCs [9, 10] make use of few unit capacitors. These ADCs operate in three phases, taking 50% additional conversion time in comparison with the conventional SAR ADC. Even though mismatch performance is good, other serious issues to be addressed are thermal noise and voltage-dependent parasitics. In this paper, we propose a novel SC integrator architecture using unit-sized capacitors. The proposed architecture is less parasitic sensitive when compared with other non-BWCA-based SAR ADCs. The architecture shows good capacitor matching and also low noise, enabling area and energy-efficient ADC design.

2 Proposed SC integrator SAR ADC

2.1 Concept

Consider two unit capacitors, C_1 and C_2, as shown in Fig. 1*a*. Assume that the capacitors are initially discharged. Phase ϕs charges C_1 to full-scale reference voltage V_{ref}. $\phi 1$, $\phi 2$ and $\phi 3$ are non-overlapping clock phases. During $\phi 1$, charge in C_1 is passively shared with C_2. The voltage across each of these capacitors after charge sharing is equal to $V_{ref}/2$. During the phase $\phi 2$, C_2 discharges to *gnd*. The cycle is repeated to yield binary fractions of V_{ref} across C_1. Alternatively, with $\phi 3$, C_2 may also discharge to *gnd* (virtual) using an SC integrator, as illustrated in Fig. 1*b*. The capacitor C_{int} will, therefore, become capable of integrating binary fractions of V_{ref}. Suppose C_{int} is unit sized and had initially sampled the input voltage V_{in}, the output voltage V_o after N clock cycles will be

$$V_o = V_{in} - \sum_{i=1}^{N} B_{N-i}\frac{V_{ref}}{2^i} \tag{1}$$

Here, we denote B_{N-i} as a binary decision to use integrator circuit to discharge C_2 at an ith clock cycle.

The above method realises an ADC using SC integration technique. However, in a realistic circuit, some serious issues affect the conversion accuracy. First, the switches in the architecture [implemented using complementary metal–oxide–semiconductor (CMOS) transmission gate] inevitably have source-to-bulk and drain-to-bulk depletion layer parasitics. The parasitics are voltage dependent and hence affects the charge sharing accuracy between two unit capacitors. Second, thermal noise at the integrator output increases linearly with the clock cycle. Let Q_1, q_{p1} and $c_{p1}(v)$, respectively, be the charge, parasitic charge and parasitic associated with C_1. Similarly, Q_2, q_{p2} and $c_{p2}(v)$ are associated with C_2. The resultant voltage v due to sharing of charge between capacitors C_1 and C_2 is given by (2)

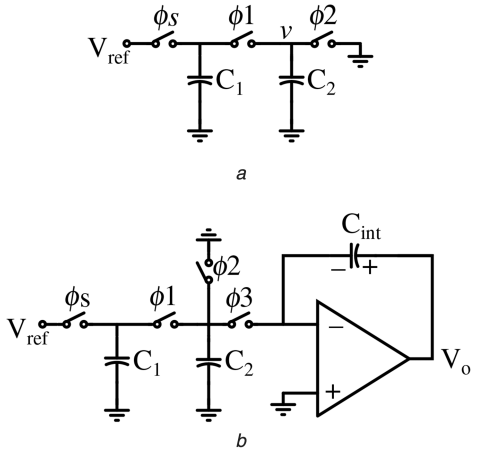

Fig. 1 *Illustration of concept*
(a) Passive charge sharing between unit capacitors, ***(b)*** SC integration

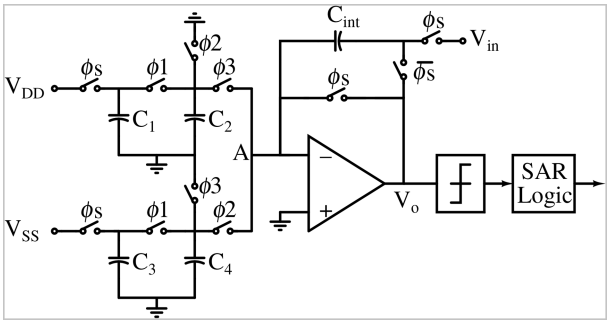

Fig. 2 *Proposed SAR ADC*

$$v = \frac{Q_1 + Q_2 + q_{p1} + q_{p2}}{C_1 + C_2 + c_{p1}(v) + c_{p2}(v)} \tag{2}$$

If C_1 was to be initially charged to V_{ref} and C_2 discharged to *gnd*, the maximum change in v will be $V_{ref}/2$. The parasitics and the change in v influence the charge sharing accuracy.

To reduce error, first, we suggest making use of two identical passive charge sharing circuits. The unit capacitors of one such circuit are initially charged to positive rail supply voltage V_{DD}, while the other with negative rail supply voltage V_{SS}. Supply voltages shall be $V_{DD} = -V_{SS} = (V_{ref}/2)$. During every clock cycle, charge from a unit capacitor of either of the two charge sharing circuits will be allowed to integrate into C_{int}. The maximum change in v is now limited to $V_{ref}/4$. This enhances the charge sharing accuracy by two-fold (assuming the rate of change in voltage-dependent parasitic with node voltage is a constant). Second, we double the size of the integrator capacitor, due to which the thermal noise power at the output of the integrator is reduced by a factor of 4 (discussed in Section 3.1). The strategy of having two passive charge sharing circuits and reduction of integrator gain by two, leads to total capacitor area reduction.

2.2 Circuit description

Fig. 2 shows the proposed SC integrator-based SAR ADC. Unit capacitors C_1 and C_2 form a passive charge sharing capacitor pair. Unit capacitors C_3 and C_4 form the other capacitor pair. The capacitor C_{int} is serving both as sample-and-hold and integrator capacitor. The comparator output is fed to control logic. The switches are operated in reference to the clock. A dual power supply voltage source is used, with the common terminal voltage at *gnd*. If voltages V_{DD} and V_{SS} differ in their magnitude, the architecture shall be modified, wherein capacitors C_3 and C_4 will bottom plate sample the V_{DD}.

2.3 Operation

Nominally, capacitors $C_1 = C_2 = C_3 = C_4 = C$ and $C_{int} = 2C$. Supply voltage $V_{DD} = -V_{SS} = V_{ref}/2$. Terminal A in Fig. 2 corresponds to virtual ground. All clock phases are non-overlapping. Each clock cycle constitutes a charge integration and a charge sharing phase. Following describes the step-by-step operation:

i. *Sampling (first cycle of integration phase):* Phases ϕs and $\phi 1$ raise. Capacitor C_{int} samples V_{in}. Meantime, C_1 and C_2 sample V_{DD} and C_3 and C_4 sample V_{SS} (see Fig. 3*a*). The output voltage V_o is at virtual *gnd* during sampling. On completion of the sampling process, ϕs goes low and thus $V_o = V_{in}$.
ii. *Passive charge sharing and comparison:* With $\phi 1$ remaining high, C_1 and C_2 share charge. So do C_3 and C_4 (see Fig. 3*b*). The sharing makes no difference during the first cycle as the capacitors have equal charge. V_o is compared against *gnd* to fetch the most significant bit (MSB).
iii. *Charge integration:* If the MSB is logic '0', phase $\phi 2$ raises (see Fig. 3*c*). C_4 will transfer charge to C_{int} and C_2 discharges to *gnd*. Else, phase $\phi 3$ raises. C_2 will move charge to C_{int} and C_4 discharges to *gnd*. C_1 and C_3 hold onto their charge. The new output voltage will be

$$V_o = V_{in} + (-1)^{MSB} V_{ref}/4 \tag{3}$$

iv. The remaining bits are similarly determined by the following steps 2–3.

Fig. 3*d* shows the desired clock phases.

3 Analysis

3.1 Noise estimation

For simplicity, a portion of a network (in Fig. 2) having C_1, C_2 and C_{int} is considered. The switches are the source of thermal noise due to finite ON state resistance. The switch is modelled as a resistor R_{on} in series with a noise source v_{nr}. Noise model during charge sharing process is shown in Fig. 4*a*. Sharing of charge adds thermal noise onto the capacitors. v_{nc1} and v_{nc2}, respectively, represent such noise with C_1 and C_2. The mean square (MS) noise voltage across all the capacitors initially is equal to kT/C, suggesting $\overline{v^2}_{nc1}[1] = kT/C$. Since C_2 always discharges to either *gnd* or virtual ground before the commencement of charge sharing, v_{nc2} for any clock cycle will be kT/C. The noise acquired after sharing during nth cycle is given by

$$\overline{v^2}_{nc1}[n+1] = \overline{v^2}_{nc2}[n+1] = \frac{1}{2}\left(\overline{v^2}_{nc1}[n] + \frac{2kT}{C}\right) \tag{4}$$

The noise acquired by C_2 toward the end of charge sharing phase is introduced in integration phase and vice versa. Noise model during integration phase is shown in Fig. 4*b*. The acquired noise by C_2, along with the integrating switch noise and operational transconductance amplifier (OTA) noise, is added onto C_{int}. Source v_{nOTA} represents the input-referred thermal noise of the OTA. The output resistance R_L of the OTA is assumed to be infinite. The noise source v_{nr}, placed at integrator output node, is due to switching during input sample-and-hold process. The integrating switch noise and OTA noise are given by (5) and (6) [11]

$$\overline{v^2}_{nSW} = \frac{kT/C}{1 + 1/x} \tag{5}$$

$$\overline{v^2}_{nOTA} = \frac{kT\Gamma/C}{1 + x} \tag{6}$$

The parameter $x = 2g_m R_{on}$ and Γ is commonly known as Ogawa's/excess noise factor (device noise alone). g_m represents the OTA

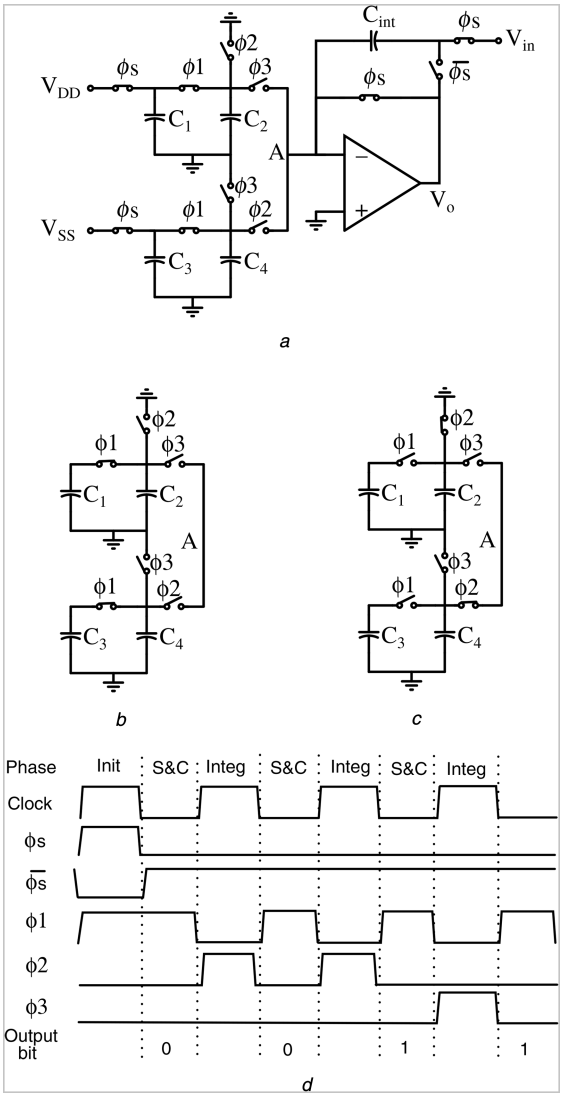

Fig. 3 *Illustration of the proposed architecture. Circuit configuration during*
(a) Initialisation/sampling phase (ϕs), ***(b)*** Passive charge sharing and comparison phase ($\phi 1$), ***(c)*** Charge integration phase, say, for MSB result of '0' ($\phi 2$), ***(d)*** Desired clock phases (phases Init, S&C and Integ in the waveform diagram are, respectively, referred to as initialisation, sharing and comparison and integration)

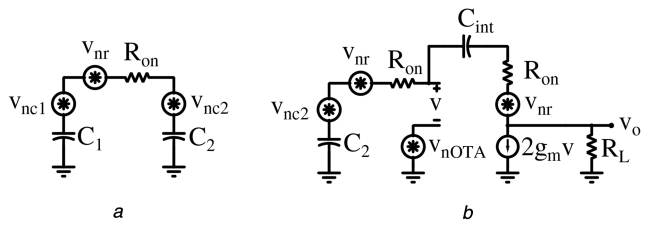

Fig. 4 *Noise analysis model of the ADC during*
(a) Charge sharing, ***(b)*** Charge integration

Table 1 Noise computation for the proposed ADC

Clock	$\overline{v^2}_{nc2}$, kT/C	$\overline{v^2}_{n}$, kT/C
1	1	1
2	1.5	1.625
3	1.75	2.3125
4	1.875	3.03125
5	1.9375	3.765625
6	1.96875	4.5078125
7	1.984375	5.25390625
8	1.9921875	6.001953125

transconductance. Since integrator gain is halved, the noise added at integrator output during every cycle is

$$\overline{v^2}_{n,o}[n] = \frac{1}{4}\left(\overline{v^2}_{nc2}[n] + \overline{v^2}_{nSW} + \overline{v^2}_{nOTA}\right) \tag{7}$$

The total MS noise at output including input sampling noise toward the end of Nth clock cycle is

$$\overline{v^2}_{n} = \sum_{n=2}^{N} \overline{v^2}_{n,o}[n] + \frac{kT}{C} \tag{8}$$

With $x \gg 1$, the OTA noise could be neglected, and Table 1 shows computed MS noise values. Equating obtained thermal noise to quantisation noise, the minimum total capacitance required for different ADC resolutions is plotted in Fig. 5. A plot is shown, wherein the BWCA-based SAR ADC is limited by the mismatch. Equation (9) from [12] estimates the total capacitance requirement

$$C_{BWCA} = 2^N 18(2^N - 1)K_\sigma^2 K_C \tag{9}$$

where K_σ is the mismatch coefficient and K_C is the capacitor density, whose respective values considered are 1% μm and 2 fF/μm^2. The plot also shows total capacitance estimate for a split BWCA with two identical arrays. Equation (9) is modified and presented in (10). The estimate shows a slight reduction in total capacitance, as K_σ reduces with large-sized capacitors. K_σ is taken to be 0.8% μm

$$C_{split\,BWCA} = 2^{((N/2)+1)} 18(2^{((N/2)-1)})2^N K_\sigma^2 K_C \tag{10}$$

A similar noise estimation is done for the proposed architecture in [10] and its plot of total capacitance requirement is also shown in this figure. Since integrator gain is unity and possibly two integrations per bit, the accumulated thermal noise is large in their case. All the plots are normalised to a voltage range of 1 V. It is evident that the proposed architecture of SAR ADC has least total capacitance requirement. As a comparison, for resolution of 10 bits, the total capacitance value of proposed ADC is 0.785 pF against 2.4 pF of split BWCA SAR and 3.7 pF of the rest.

3.2 Capacitor mismatch

For a worst possible capacitor mismatch, assume C_2 and C_4 have normalised capacitance values of $1 + \alpha$ and C_1 and C_3 have $1 - \alpha$. Furthermore, C_{int} is assumed to $2[1 \pm (\alpha/\sqrt{2})]$ and we shall pick the term having a negative symbol in this analysis $\alpha \ll 1$. Let q be the desired initial charge in the unit capacitors. Table 2 shows the charge held by unit capacitors of charge sharing circuits. The higher-order terms of α are ignored. Integrating the DAC equivalent charge, the integrator output voltage V_o is given by (11). Applying Taylor series, (11) is approximated as (12). Toward the end of conversion, the integrator output voltage should ideally converge to *gnd*. However, the non-zero value arises due to the mismatch. Denoting the error as ε, we get (13). The summation of first two terms on right-hand side of (13) will be zero. The remaining term is then given by (14) (see (11))

$$V_o \simeq V_{in} - q\sum_{k=1}^{N-1} \frac{1}{2^k}\left(B_{N-k}(1-(k-2)\alpha) - \overline{B}_{N-k}(1-(k-2)\alpha)\right)\left(1+\frac{\alpha}{\sqrt{2}}\right) \tag{12}$$

$$\varepsilon \simeq V_{in} - q\sum_{k=1}^{N-1} \frac{1}{2^k}(B_{N-k} - \overline{B}_{N-k}) + q\alpha\sum_{k=1}^{N-1} \frac{1}{2^k}\left[(B_{N-k} - \overline{B}_{N-k})(k-2) - \left(\frac{B_{N-k} - \overline{B}_{N-k}}{\sqrt{2}}\right)\right] \tag{13}$$

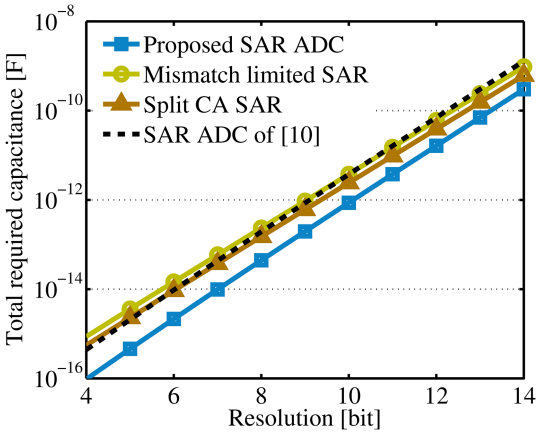

Fig. 5 *Total capacitance requirement in various SAR ADC architectures*

$$|\varepsilon| \simeq q\alpha \sum_{k=1}^{N-1} \frac{1}{2^k}\left[(B_{N-k} - \overline{B}_{N-k})(k-2) - \left(\frac{B_{N-k} - \overline{B}_{N-k}}{\sqrt{2}}\right)\right] \quad (14)$$

$$|\varepsilon_{max}| \simeq q\alpha\left[\frac{(1+(1/\sqrt{2}))}{2^1} + \frac{(0+(1/\sqrt{2}))}{2^2} + \frac{(1-(1/\sqrt{2}))}{2^3} + \cdots + \frac{(N-3-(1/\sqrt{2}))}{2^{N-2}}\right] \quad (15)$$

On observing (14), the voltage ε is maximum at places of one and three quarters of output codes. Let us choose the code to be 0011..1. Note, this selection of code is conditionally valid and depends on the assumption made earlier in this analysis. The expression for maximum ε for the preferred output code is achieved by expanding (14). The obtained equation is (15). Summing the arithmetico-geometric series within

$$|\varepsilon_{max}| \simeq q\alpha\left[1 + \frac{1}{2\sqrt{2}} - \left(\frac{1}{2}\right)^{N-1}\left(N - 1 - \frac{1}{\sqrt{2}}\right)\right] \quad (16)$$

For large values of N, the term $(1/2)^{N-1}(N-1-(1/\sqrt{2}))$ converges to zero. On substitution of normalised charge q as $V_{ref}/2$ and α as σ_u/C_u, (16) could be denoted as

$$\frac{|\varepsilon_{max}|}{V_{ref}} \simeq 0.676\frac{\sigma_u}{C_u} \quad (17)$$

Equation (17) represents the relation between the conversion accuracy and the capacitance mismatch. With modern chip fabrication technologies being able to provide well-matched capacitors, the obtained result assures good conversion accuracy. For an obtained unit capacitor size (30 fF) in the design, the standard deviation of unit capacitance is around 0.1%. Considering that the ADC delivers 8 bit accuracy, the conversion error introduced due to worst capacitor matching is within the range of 0.2 least significant bit (LSB).

3.3 Bandwidth

The ADC yields 1 bit every clock cycle. The SC integrator performance influences the ADC throughput and is given as NF_S bits per second. Considering that the integrator has no pole-zero doublets below the unity-gain bandwidth (UGB) and the slew duration is small, the settling time duration t_s to satisfy N effective number of bits (ENoB) is

Table 2 Charge held by unit capacitors during charge sharing phase

Clock	Charge held by	
	C_1 (C_3)	C_2 (C_4)
1	$q(1-\alpha)$	$q(1+\alpha)$
2	$q\left(\frac{1-2\alpha}{2}\right)$	$q\left(\frac{1}{2}\right)$
3	$q\left(\frac{1-3\alpha}{4}\right)$	$q\left(\frac{1-\alpha}{4}\right)$
4	$q\left(\frac{1-4\alpha}{8}\right)$	$q\left(\frac{1-2\alpha}{8}\right)$
.	.	.
.	.	.
N	$q\left(\frac{1-N\alpha}{2^{N-1}}\right)$	$q\left(\frac{1-(N-2)\alpha}{2^{N-1}}\right)$

$$t_s = N\ln(2N)\frac{1}{\text{UGB}\,.\,\beta} \quad (18)$$

where β is the feedback ratio, equal to 2/3 in this architecture. For a 50% duty cycle clock, the ADC throughput will be

$$\text{throughput} = \frac{\text{UGB}}{3\ln(2N)} \quad (19)$$

From (19), it is clear that the ADC can deliver higher throughput if unity-gain frequency of the integrator is high. Also, the open-loop gain of the amplifier can influence the steady-state error of the integrator. The gain error is expressed as

$$|\text{gain error}| = \frac{C/2C_{int}+1}{A_V} \quad (20)$$

C is the unit capacitance and A_V is the open-loop gain.

4 Implementation

4.1 OTA

The presence of an OTA in any ADC is a drawback. However, an OTA designed robustly in subthreshold region consumes less power and area. Fig. 6*a* shows designed OTA. The input stage is a self-biased differential amplifier [13] with transconductance pairs $M1_{a,b}$ and $M2_{a,b}$. The output stage is a cascode amplifier. Simple Miller Resistor-Capacitor compensation stabilises the circuit. The OTA offers required DC gain and bandwidth at low voltage. Bodies of all transistors are tied to *gnd* to reduce threshold voltage.

The power consumption of the OTA, under the data conversion environment, is expressed as (21). A detailed derivation is presented in [14]

$$P = 4N_N N_C kTV_{ov}\ln\left(\frac{2}{3}DR^2\right)\frac{DR^2}{V_{ref}}f_{clk} \quad (21)$$

where V_{ov} is the gate overdrive voltage, N_N and N_C, respectively, are excess noise and excess capacitance factors at the integrator output. The reduced unit capacitor size in the proposed ADC lowers the value of N_C and, therefore, low power.

The DC gain and the phase margin of the OTA are 82.12 dB and 70.61°, respectively, at a typical process, voltage and temperature. The UGB is close to 17 MHz. An auto-zeroing technique [15] is incorporated to remove the input-referred offset voltage and $1/f$ noise.

$$V_o = V_{in} - q\left[\left(B_{N-1}(1+\alpha) + \frac{B_{N-2}}{2} + \frac{B_{N-3}}{4}(1-\alpha) + \cdots + \frac{B_1}{2^{N-2}}(1-(N-3)\alpha)\right) - \left(\overline{B}_{N-1}(1+\alpha) + \frac{\overline{B}_{N-2}}{2} + \frac{\overline{B}_{N-3}}{4}(1-\alpha) + \cdots + \frac{\overline{B}_1}{2^{N-2}}(1-(N-3)\alpha)\right)\right]\frac{1}{2(1-(\alpha/\sqrt{2}))} \quad (11)$$

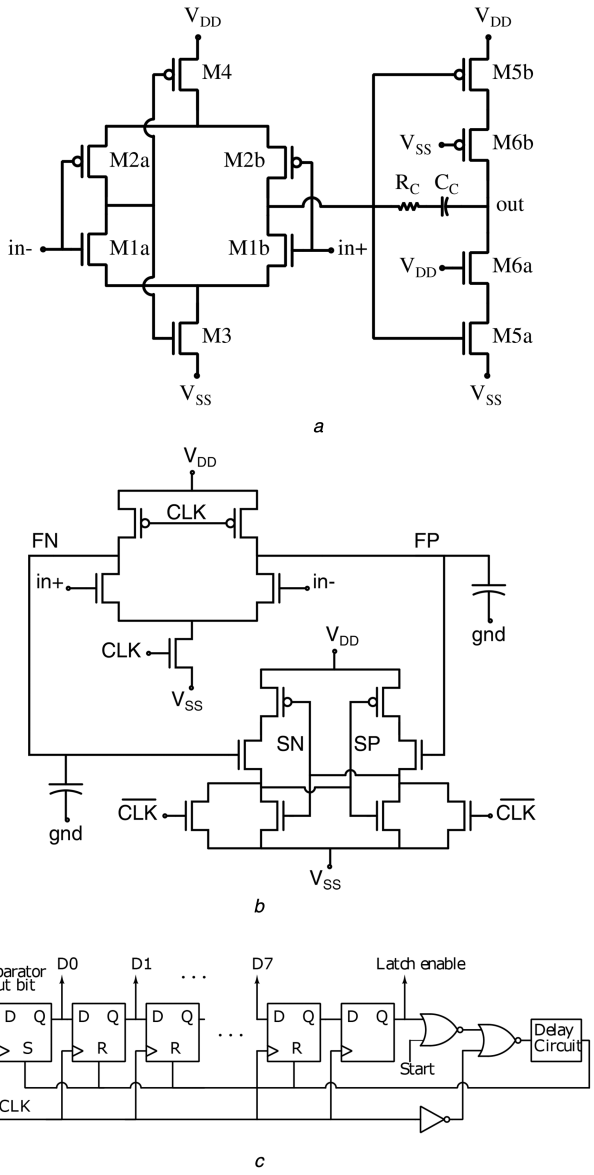

Fig. 6 *Diagram of the*
(a) OTA circuit, ***(b)*** Comparator circuit, ***(c)*** Control logic block

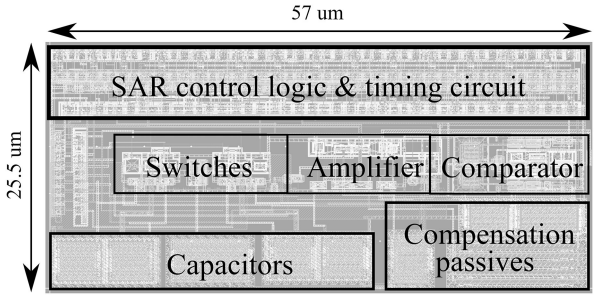

Fig. 7 *Layout of the ADC*

4.2 Switches and capacitors

Owing to bottom plate sampling technique, C_{int} acquires no signal-dependent charge error while sampling V_{in}. Similar impedance is seen at either end of a charge sharing switch. In the case of a charge integration switch, the impedances differ, but remain constant throughout the operation of the ADC. Therefore, this allows the complementary MOS transistor switch to be sized accordingly to overcome channel charge injection error. Besides, complementary MOS transistors lower the variation of voltage-dependent parasitics at charge sharing nodes. Switches with a small geometry size are preferred to keep parasitic to a minimum. Switches have N-channel MOS of size 120 nm × 90 nm and P-channel MOS of size 150 nm × 90 nm. Dummy transistors are placed, wherever necessary, to have an equal amount of parasitic at all the charge sharing nodes. In the given technology, metal–oxide–metal capacitors offer good matching characteristics. The capacitor C_{int} is 60 fF in size and the capacitors C_{1-4} are of 30 fF.

4.3 Comparator

The comparator specifications are relaxed due to charge sharing process being independent of the comparison result. A double-tail dynamic latched comparator [16], shown in Fig. 6*b* serves the purpose. Discharge capacitor size is chosen to be 15 fF each. This large size of capacitor improves matching and reduces comparator kickback. The voltage at the inputs of the comparator settles down to *gnd* toward the end of conversion. The devices in the comparator circuit are matched to reduce the offset voltage. The comparator consumes very less power due to relaxed gain and bandwidth requirement.

4.4 Control logic

$N+2$ number of D flip-flops are used to form a circular shift register. The block diagram is shown in Fig. 6*c*. The register also receives the data bit from the output of the comparator and right shifts the data bits forming serial to parallel conversion. On reaching the end of conversion, the digital equivalent of the analogue input is fetched to external circuitry and the flip-flop contents are reset as desired. Although the switches appear to be more in number, fewer combinational logic circuit elements are required.

5 Simulation results

The ADC is designed for 8 bits using 90 nm CMOS process of United Microelectronics Corporation. The ADC operates with analogue input voltage spanning full-scale rail-to-rail supply voltage of ±350 mV. An auxiliary supply voltage of 600 mV is used for increasing gate overdrive of switches. The layout of the ADC is shown in Fig. 7 and the area occupied is 0.00145 mm^2 (57 µm × 25.5 µm). Post-layout extraction generates a netlist for simulation requirements. The total ADC power consumption is 931 nW at a sampling frequency of 780 kHz, out of which the OTA accounts for 39.7%.

5.1 Linearity test of the ADC

The static performance of the ADC is shown in Fig. 8*a*. Absolute values of both the static non-linearities are limited below 1 LSB. The big integral nonlinearity (INL) error at the mid-code is mainly due to node parasitics. Spectral simulation is shown in Fig. 8*b*. Signal-to-noise ratio (SNR) is found to be 45.63 dB for the typical process corner. Close to a value of 1.8 dB loss from an ideal signal-to-quantisation-NR is due to design decision of having total thermal noise equal to half the quantisation error. For the sake of low-power consumption, the OTA transconductance is chosen low. The result is a significant input-referred thermal noise of the OTA. Thus, the SNR degradation of around 3.5 dB is due in large part to the OTA noise. Total distortion component is close to 1 dB, largely attributed to switching non-idealities. The achieved SN-and-distortion ratio (SNDR) of the ADC is 44.45 dB, and the spurious-free dynamic range is 61 dB.

To verify the ADC performance across process variations and capacitor mismatch, Monte Carlo runs of 200 numbers are carried out. Figs. 8*c* and *d* show the statistical distributions. The mean and 3σ differential nonlinearity (DNL) errors are 0.87 and 0.54 LSB, respectively. In the case of INL, the respective error values are 1.37 and 1.59 LSB. The mean and 3σ SNR are 42.16 and 1.7 dB, respectively. An additional 2.33 dB loss, when compared with typical process corner simulation, is largely due to channel charge injection variation experienced at different process corners.

Fig. 9 shows the plot of SNDR and total power consumption of the ADC against the sampling frequency. The SNDR reduces at lower sampling frequencies due to increased charge leakage by the

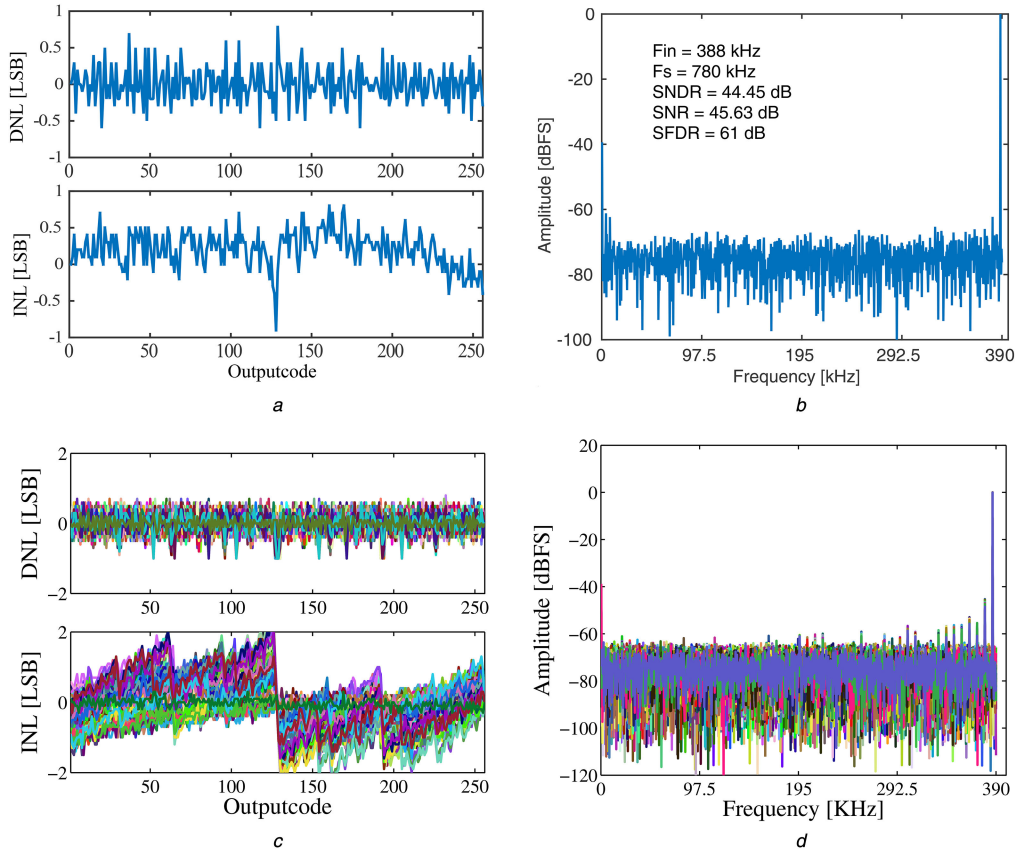

Fig. 8 *Linearity performance of the ADC*

(a) Differential and integral non-linearity curves of the ADC, ***(b)*** FFT spectrum of the ADC, ***(c)*** Statistical distributions of DNL and INL errors, ***(d)*** Statistical distribution FFT spectrum and SNR distribution

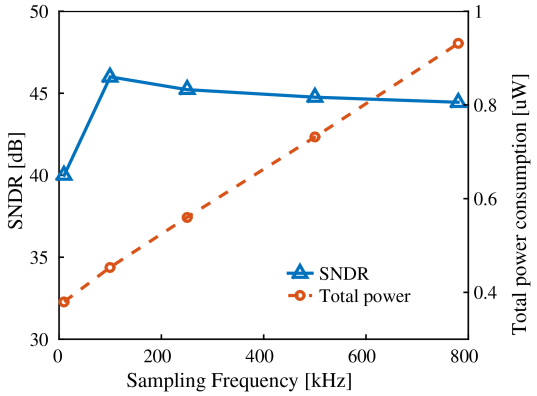

Fig. 9 *Plot of SNDR and total power consumption of the ADC versus sampling frequency*

unit capacitors. The change in frequency is linearly related to change in power consumption. For higher frequencies, switching power dominates the total power consumption.

5.2 Comparison and discussion

The ADC is compared with other state-of-the-art SAR ADC designs in Table 3. Area efficiency (AE) merit is computed as in [20]. The proposed ADC shows good area performance and at the same time competitive with energy efficiency. The AE is 13.85 μm^2/code and the figure-of-merit (FoM) of the ADC at 780 kS/s is 11.39 fJ/conv-step. The ADC has a clear stand out in performance when compared with its non-binary WCA-based SAR ADC counterparts, though only fewer designs are available for comparison. Both the non-binary designs are mainly affected due to parasitic, and therefore consume large power. The ADC is also compared against BWCA-based ADCs. Long *et al.* [18] employ statistical estimation method to evaluate LSB (however, requires a large number of clock cycles) while [17] implements subranging SAR ADC with energy-efficient algorithm at lower technology node. Energy-efficient V_{CM}-based switching schemes are utilised in [12, 19]. The area occupied is large due to implementation in a relatively old process. Unlike other SAR ADC designs, the unit capacitor array holds a small portion of the ADC layout (see Fig. 7). Therefore, the area of the ADC would increase only slightly if higher resolution is desirable. Noise is traded for power, and the achieved linearity is typical as in any other SAR ADC designs. ENoB is close to 1.3 bit less than theoretical. The large part of power consumption of the proposed ADC is proportional to the number of conversion clocks, which indeed is resolution dependent. In the case of traditional, the DAC power consumption (primary contributor for ADC power consumption) is nearly same for all resolutions if MSB capacitors and supply voltage remain unchanged [21].

6 Conclusion

The proposed architecture is robust amidst parasitic capacitances and offers low noise. The result is a small capacitance load on the OTA, allowing both power and noise specification of the employed

Table 3 ADC performance comparison

	[6][a]	[8][b]	[17][b]	[18][b]	[12][b]	[19][b]	This work[a]
supply, V	0.8	0.7	0.45	0.7	0.6	0.5	±0.35
process, nm	130	90	40	65	180	180	90
DAC type	non-binary	non-binary	binary	binary	binary	binary	non-binary
F_S (MS/s)	0.025	0.1	0.2	0.1	0.02	0.01	0.78
power, W	0.35 µ	700 n	84 n	645 n	38 n	68 n	931 n
ENoB, bit	7.81	4.5	8.95	10.5	9.4	9.3	6.71
area, mm^2	—	0.0135	0.0065	0.03	0.1634	0.144	0.00145
FoM, fJ/step	62	310	0.85	4.5	2.8	10.8	11.39
AE, μm^2/code	—	596.6	13.14	20.72	241.9	228.4	13.85

[a]Simulated results.

[b]Fabricated results.

OTA to be relaxed. The unit capacitors in the design show good capacitance matching. The design thus promises a low-power consumption and a small area of the chip. The performance is competitive with the benchmark designs, even though the proposed ADC includes a higher percentage of the analogue blocks.

7 References

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